

Pulse-width Modulated DC-DC Power Converters

Marian K. Kazimierczuk

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Wright State University
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To my family

Contents

Preface xix
About the Author xxi
List of Symbols xxiii

1 Introduction 1

1.1 Classification of Power Supplies 1
1.2 Basic Functions of Voltage Regulators 3
1.3 Power Relationships in DC–DC Converters 5
1.4 DC Transfer Functions of DC–DC Converters 5
1.5 Static Characteristics of DC Voltage Regulators 6
1.6 Dynamic Characteristics of DC Voltage Regulators 9
1.7 Linear Voltage Regulators 12
1.7.1 Series Voltage Regulator 13
1.7.2 Shunt Voltage Regulator 14
1.8 Topologies of PWM DC–DC Converters 17
1.9 Relationships among Current, Voltage, Energy, and Power 18
1.10 Electromagnetic Compatibility 19
1.11 Summary 20
1.12 References 20
1.13 Review Questions 21
1.14 Problems 22

2 Buck PWM DC–DC Converter 23

2.1 Introduction 23
2.2 DC Analysis of PWM Buck Converter for CCM 23
2.2.1 Circuit Description 23
2.2.2 Assumptions 27
2.2.3 Time Interval $0 < t \leq DT$ 27
2.2.4 Time Interval $DT < t \leq T$ 28
2.2.5 Device Stresses for CCM 29
2.2.6 DC Voltage Transfer Function for CCM 29

2.2.7 Boundary between CCM and DCM 30
2.2.8 Ripple Voltage in Buck Converter for CCM 32
2.2.9 Switching Losses with Linear MOSFET Output Capacitance 37
2.2.10 Switching Losses with Nonlinear MOSFET Output Capacitance 39
2.2.11 Power Losses and Efficiency of Buck Converter for CCM 42
2.2.12 DC Voltage Transfer Function of Lossy Converter for CCM 46
2.2.13 MOSFET Gate-drive Power 47
2.2.14 Design of Buck Converter for CCM 48
2.3 DC Analysis of PWM Buck Converter for DCM 51
2.3.1 Time Interval $0 < t \leq DT$ 54
2.3.2 Time Interval $DT < t \leq (D + D_1)T$ 56
2.3.3 Time Interval $(D + D_1)T < t \leq T$ 57
2.3.4 Device Stresses for DCM 57
2.3.5 DC Voltage Transfer Function for DCM 57
2.3.6 Maximum Inductance for DCM 59
2.3.7 Power Losses and Efficiency of Buck Converter for DCM 61
2.3.8 Design of Buck Converter for DCM 63
2.4 Buck Converter with Input Filter 69
2.5 Buck Converter with Synchronous Rectifier 69
2.6 Buck Converter with Positive Common Rail 72
2.7 Tapped-inductor Buck Converters 74
2.7.1 Tapped-inductor Common-diode Buck Converter 74
2.7.2 Tapped-inductor Common-transistor Buck Converter 76
2.7.3 Watkins–Johnson Converter 76
2.8 Multiphase Buck Converter 77
2.9 Summary 79
2.10 References 81
2.11 Review Questions 81
2.12 Problems 82

3 Boost PWM DC–DC Converter 85

3.1 Introduction 85
3.2 DC Analysis of PWM Boost Converter for CCM 85
3.2.1 Circuit Description 85
3.2.2 Assumptions 88
3.2.3 Time Interval $0 < t \leq DT$ 88
3.2.4 Time Interval $DT < t \leq T$ 89
3.2.5 DC Voltage Transfer Function for CCM 90
3.2.6 Boundary between CCM and DCM 91
3.2.7 Ripple Voltage in Boost Converter for CCM 93
3.2.8 Power Losses and Efficiency of Boost Converter for CCM 95
3.2.9 DC Voltage Transfer Function of Lossy Boost Converter for CCM 97
3.2.10 Design of Boost Converter for CCM 99
3.3 DC Analysis of PWM Boost Converter for DCM 103
3.3.1 Time Interval $0 < t \leq DT$ 105

3.3.2 Time Interval $DT < t \leq (D + D_1)T$ 106
3.3.3 Time Interval $(D + D_1)T < t \leq T$ 108
3.3.4 Device Stresses for DCM 108
3.3.5 DC Voltage Transfer Function for DCM 108
3.3.6 Maximum Inductance for DCM 112
3.3.7 Power Losses and Efficiency of Boost Converter for DCM 112
3.3.8 Design of Boost Converter for DCM 115
3.4 Bidirectional Buck and Boost Converters 122
3.5 Tapped-inductor Boost Converters 124
3.5.1 Tapped-inductor Common-diode Boost Converter 126
3.5.2 Tapped-inductor Common-load Boost Converter 126
3.6 Duality 127
3.7 Power Factor Correction 129
3.7.1 Power Factor 129
3.7.2 Boost Power Factor Corrector 132
3.8 Summary 134
3.9 References 135
3.10 Review Questions 136
3.11 Problems 136

4 Buck-boost PWM DC–DC Converter 139

4.1 Introduction 139
4.2 DC Analysis of PWM Buck-boost Converter for CCM 139
4.2.1 Circuit Description 139
4.2.2 Assumptions 140
4.2.3 Time Interval $0 < t \leq DT$ 142
4.2.4 Time Interval $DT < t \leq T$ 142
4.2.5 DC Voltage Transfer Function for CCM 143
4.2.6 Device Stresses for CCM 144
4.2.7 Boundary between CCM and DCM 145
4.2.8 Ripple Voltage in Buck-boost Converter for CCM 146
4.2.9 Power Losses and Efficiency of the Buck-boost Converter for CCM 149
4.2.10 DC Voltage Transfer Function of Lossy Buck-boost Converter for CCM 151
4.2.11 Design of Buck-boost Converter for CCM 153
4.3 DC Analysis of PWM Buck-boost Converter for DCM 159
4.3.1 Time Interval $0 < t \leq DT$ 160
4.3.2 Time Interval $DT < t \leq (D + D_1)T$ 162
4.3.3 Time Interval $(D + D_1)T < t \leq T$ 162
4.3.4 Device Stresses of the Buck-boost Converter in DCM 162
4.3.5 DC Voltage Transfer Function of the Buck-boost Converter for DCM 163
4.3.6 Maximum Inductance for DCM 166
4.3.7 Power Losses and Efficiency of the Buck-boost Converter in DCM 166
4.3.8 Design of Buck-boost Converter for DCM 168
4.4 Bidirectional Buck-boost Converter 174
4.5 Synthesis of Buck-boost Converter 175

4.6 Synthesis of Boost-buck (Ćuk) Converter 177
4.7 Noninverting Buck-boost Converters 178
4.7.1 Cascaded Noninverting Buck-boost Converters 178
4.7.2 Four-transistor Noninverting Buck-boost Converters 179
4.8 Tapped-inductor Buck-boost Converters 181
4.8.1 Tapped-inductor Common-diode Buck-boost Converter 181
4.8.2 Tapped-inductor Common-transistor Buck-boost Converter 182
4.8.3 Tapped-inductor Common-load Buck-boost Converter 183
4.8.4 Tapped-inductor Common-source Buck-boost Converter 184
4.9 Summary 185
4.10 References 186
4.11 Review Questions 187
4.12 Problems 187

5 Flyback PWM DC–DC Converter 189

5.1 Introduction 189
5.2 Transformers 190
5.3 DC Analysis of PWM Flyback Converter for CCM 191
5.3.1 Derivation of PWM Flyback Converter 191
5.3.2 Circuit Description 192
5.3.3 Assumptions 193
5.3.4 Time Interval $0 < t \leq DT$ 195
5.3.5 Time Interval $DT < t \leq T$ 196
5.3.6 DC Voltage Transfer Function for CCM 197
5.3.7 Boundary between CCM and DCM 198
5.3.8 Ripple Voltage in Flyback Converter for CCM 199
5.3.9 Power Losses and Efficiency of Flyback Converter for CCM 201
5.3.10 DC Voltage Transfer Function of Lossy Converter for CCM 204
5.3.11 Design of Flyback Converter for CCM 205
5.4 DC Analysis of PWM Flyback Converter for DCM 211
5.4.1 Time Interval $0 < t \leq DT$ 212
5.4.2 Time Interval $DT < t \leq (D + D_1)T$ 213
5.4.3 Time Interval $(D + D_1)T < t \leq T$ 214
5.4.4 DC Voltage Transfer Function for DCM 214
5.4.5 Maximum Magnetizing Inductance for DCM 218
5.4.6 Ripple Voltage in Flyback Converter for DCM 218
5.4.7 Power Losses and Efficiency of Flyback Converter for DCM 219
5.4.8 Design of Flyback Converter for DCM 222
5.5 Multiple-output Flyback Converter 228
5.6 Bidirectional Flyback Converter 229
5.7 Ringing in Flyback Converter 229
5.8 Flyback Converter with Active Clamping 232
5.9 Two-transistor Flyback Converter 233
5.10 Summary 234
5.11 References 235

5.12 Review Questions 236
5.13 Problems 236

6 Forward PWM DC–DC Converter 239

6.1 Introduction 239
6.2 DC Analysis of PWM Forward Converter for CCM 239
6.2.1 Derivation of Forward PWM Converter 239
6.2.2 Time Interval $0 < t \leq DT$ 241
6.2.3 Time Interval $DT < t \leq DT + t_m$ 243
6.2.4 Time Interval $DT + t_m < t \leq T$ 245
6.2.5 Maximum Duty Cycle 246
6.2.6 Device Stresses 246
6.2.7 DC Voltage Transfer Function for CCM 247
6.2.8 Boundary between CCM and DCM 248
6.2.9 Ripple Voltage in Forward Converter for CCM 248
6.2.10 Power Losses and Efficiency of Forward Converter for CCM 250
6.2.11 DC Voltage Transfer Function of Lossy Converter for CCM 253
6.2.12 Design of Forward Converter for CCM 254
6.3 DC Analysis of PWM Forward Converter for DCM 261
6.3.1 Time Interval $0 < t \leq DT$ 261
6.3.2 Time Interval $DT < t \leq DT + t_m$ 264
6.3.3 Time Interval $DT + t_m < t \leq (D + D_1)T$ 265
6.3.4 Time Interval $(D + D_1)T < t \leq T$ 265
6.3.5 DC Voltage Transfer Function for DCM 266
6.3.6 Maximum Inductance for DCM 270
6.3.7 Power Losses and Efficiency of Forward Converter for DCM 270
6.3.8 Design of Forward Converter for DCM 273
6.4 Multiple-output Forward Converter 280
6.5 Forward Converter with Synchronous Rectifier 281
6.6 Forward Converters with Active Clamping 281
6.7 Two-switch Forward Converter 283
6.8 Summary 283
6.9 References 284
6.10 Review Questions 285
6.11 Problems 286

7 Half-bridge PWM DC–DC Converter 289

7.1 Introduction 289
7.2 DC Analysis of PWM Half-bridge Converter for CCM 289
7.2.1 Circuit Description 289
7.2.2 Assumptions 291
7.2.3 Time Interval $0 < t \leq DT$ 292
7.2.4 Time Interval $DT < t \leq T/2$ 295
7.2.5 Time Interval $T/2 < t \leq T/2 + DT$ 296
7.2.6 Time Interval $T/2 + DT < t \leq T$ 297

7.2.7 Device Stresses 297
7.2.8 DC Voltage Transfer Function of Lossless Half-bridge Converter for CCM 298
7.2.9 Boundary between CCM and DCM 299
7.2.10 Ripple Voltage in Half-bridge Converter for CCM 299
7.2.11 Power Losses and Efficiency of Half-bridge Converter for CCM 301
7.2.12 DC Voltage Transfer Function of Lossy Converter for CCM 304
7.2.13 Design of Half-bridge Converter for CCM 305
7.3 DC Analysis of PWM Half-bridge Converter for DCM 312
7.3.1 Time Interval $0 < t \leq DT$ 312
7.3.2 Time Interval $DT < t \leq (D + D_1)T$ 314
7.3.3 Time Interval $(D + D_1)T < t \leq T/2$ 315
7.3.4 DC Voltage Transfer Function for DCM 316
7.3.5 Maximum Inductance for DCM 320
7.4 Summary 320
7.5 References 321
7.6 Review Questions 322
7.7 Problems 323

8 Full-bridge PWM DC–DC Converter 325

8.1 Introduction 325
8.2 DC Analysis of PWM Full-bridge Converter for CCM 325
8.2.1 Circuit Description 325
8.2.2 Assumptions 327
8.2.3 Time Interval $0 < t \leq DT$ 327
8.2.4 Time Interval $DT < t \leq T/2$ 329
8.2.5 Time Interval $T/2 < t \leq T/2 + DT$ 331
8.2.6 Time Interval $T/2 + DT < t \leq T$ 332
8.2.7 Device Stresses 332
8.2.8 DC Voltage Transfer Function of Lossless Full-wave Converter for CCM 332
8.2.9 Boundary between CCM and DCM 333
8.2.10 Ripple Voltage in Full-bridge Converter for CCM 335
8.2.11 Power Losses and Efficiency of Full-bridge Converter for CCM 336
8.2.12 DC Voltage Transfer Function of Lossy Converter for CCM 339
8.2.13 Design of Full-bridge Converter for CCM 340
8.3 DC Analysis of PWM Full-bridge Converter for DCM 344
8.3.1 Time Interval $0 < t \leq DT$ 344
8.3.2 Time Interval $DT < t \leq (D + D_1)T$ 349
8.3.3 Time Interval $(D + D_1)T < t \leq T/2$ 350
8.3.4 DC Voltage Transfer Function for DCM 350
8.3.5 Maximum Inductance for DCM 355
8.4 Phase-controlled Full-bridge Converter 357
8.5 Summary 358
8.6 References 358

8.7 Review Questions 359
8.8 Problems 360

9 Push-pull PWM DC–DC Converter 363

9.1 Introduction 363
9.2 DC Analysis of PWM Push-pull Converter for CCM 363
9.2.1 Circuit Description 363
9.2.2 Assumptions 365
9.2.3 Time Interval $0 < t \leq DT$ 365
9.2.4 Time Interval $DT < t \leq T/2$ 368
9.2.5 Time Interval $T/2 < t \leq T/2 + DT$ 368
9.2.6 Time Interval $T/2 + DT < t \leq T$ 369
9.2.7 Device Stresses 370
9.2.8 DC Voltage Transfer Function of Lossless Full-wave Converter for CCM 370
9.2.9 Boundary between CCM and DCM 371
9.2.10 Ripple Voltage in Push-pull Converter for CCM 372
9.2.11 Power Losses and Efficiency of Push-pull Converter for CCM 374
9.2.12 DC Voltage Transfer Function of Lossy Converter for CCM 377
9.2.13 Design of Push-pull Converter for CCM 378
9.3 DC Analysis of PWM Push-pull Converter for DCM 384
9.3.1 Time Interval $0 < t \leq DT$ 384
9.3.2 Time Interval $DT < t \leq (D + D_1)T$ 386
9.3.3 Time Interval $(D + D_1)T < t \leq T/2$ 388
9.3.4 DC Voltage Transfer Function for DCM 388
9.3.5 Maximum Inductance for DCM 392
9.4 Comparison of PWM DC–DC Converters 394
9.5 Summary 394
9.6 References 394
9.7 Review Questions 395
9.8 Problems 396

10 Small-signal Models of PWM Converters for CCM and DCM 397

10.1 Introduction 397
10.2 Assumptions 398
10.3 Averaged Model of Ideal Switching Network for CCM 398
10.4 Averaged Values of Switched Resistances 403
10.5 Model Reduction 405
10.6 Large-signal Averaged Model for CCM 407
10.7 DC and Small–signal Circuit Linear Models of Switching Network for CCM 411
10.8 Family of PWM Converter Models for CCM 418
10.9 PWM Small-signal Switch Model for CCM 419
10.10 Modeling of the Ideal Switching Network for DCM 421
10.10.1 Relationships among DC Components for DCM 421

10.10.2 Small-signal Model of Ideal Switching Network for DCM 425
10.11 Averaged Parasitic Resistances for DCM 428
10.12 Small-signal Models of PWM Converters for DCM 430
10.13 Summary 431
10.14 References 433
10.15 Review Questions 435
10.16 Problems 436

11 Open-loop Small-signal Characteristics of Boost Converter for CCM 437

11.1 Introduction 437
11.2 DC Characteristics 437
11.3 Open-loop Control-to-output Transfer Function 440
11.4 Delay in Open-loop Control-to-output Transfer Function 448
11.5 Open-loop Audio Susceptibility 450
11.6 Open-loop Input Impedance 453
11.7 Open-loop Output Impedance 455
11.8 Open-loop Step Responses 458
11.8.1 Open-loop Response of Output Voltage to Step Change in Input Voltage 458
11.8.2 Open-loop Response of Output Voltage to Step Change in Duty Cycle 461
11.8.3 Open-loop Response of Output Voltage to Step Change in Load Current 462
11.9 Summary 464
11.10 References 465
11.11 Review Questions 465
11.12 Problems 466

12 Voltage-mode Control of Boost Converter 469

12.1 Introduction 469
12.2 Circuit of Boost Converter with Voltage-mode Control 469
12.3 Pulse-width Modulator 471
12.4 Transfer Function of Modulator, Boost Converter Power Stage, and Feedback Network 474
12.5 Error Amplifier 478
12.6 Integral-single-lead Controller 480
12.7 Integral-double-lead Controller 485
12.7.1 Analysis of Integral-double-lead Controller 485
12.7.2 Design of Integral-double-lead Controller 488
12.8 Loop Gain 492
12.9 Closed-loop Control-to-output Voltage Transfer Function 493
12.10 Closed-loop Audio Susceptibility 495
12.11 Closed-loop Input Impedance 496
12.12 Closed-loop Output Impedance 500
12.13 Closed-loop Step Responses 502
12.13.1 Closed-loop Response to Step Change in Input Voltage 502

12.13.2 Closed-loop Response to Step Change in Reference Voltage 503
12.13.3 Closed-loop Response to Step Change in Load Current 505
12.14 Closed-loop DC Transfer Functions 506
12.15 Summary 507
12.16 References 508
12.17 Review Questions 508
12.18 Problems 509

13 Current-mode Control 511

13.1 Introduction 511
13.2 Principle of Operation of PWM Converters with Peak-current-mode Control 512
13.3 Relationship between Duty Cycle and Inductor-current Slopes 516
13.4 Instability of Closed-current Loop 518
13.5 Slope Compensation 521
13.6 Sample-and-hold Effect on Current Loop 526
13.6.1 Natural Response of Inductor Current to Small Perturbation in Closed-current Loop 526
13.6.2 Forced Response of Inductor Current to Step Change in Control Voltage in Closed-current Loop 528
13.6.3 Transfer Function of Closed-current Loop in z-Domain 530
13.7 Current Loop in s-Domain 531
13.7.1 Control Voltage-to-inductor Current Transfer Function 531
13.7.2 Error Voltage-to-duty Cycle Transfer Function 534
13.7.3 Loop Gain of Current Loop 537
13.7.4 Closed-loop Transfer Function of Current Loop 543
13.7.5 Alternative Representation of Current Loop 546
13.7.6 Current Loop with Disturbances 546
13.7.7 Modified Approximation of Current Loop 547
13.8 Voltage Loop of PWM Converters with Current-mode Control 550
13.8.1 Closed-voltage Loop Transfer Function 552
13.8.2 Closed-loop Audio Susceptibility 552
13.8.3 Closed-loop Output Impedance 553
13.9 Feedforward Gains in PWM Converters with Current-mode Control without Slope Compensation 554
13.10 Feedforward Gains in PWM Converters with Current-mode Control and Slope Compensation 557
13.11 Closed-loop Transfer Functions with Feedforward Gains 559
13.12 Slope Compensation by Adding a Ramp to Inductor Current 560
13.13 Relationships for Constant-frequency Current-mode On-time Control 561
13.14 Summary 561
13.15 References 562
13.16 Review Questions 565
13.17 Problems 565
13.18 Appendix: Sample-and-hold Modeling 566
13.18.1 Sampler 566

14 Current-mode Control of Boost Converter 571

14.1 Introduction 571
14.2 Open-loop Small-signal Transfer Functions 571
14.2.1 Open-loop Duty Cycle-to-inductor Current Transfer Function 571
14.2.2 Open-loop Input Voltage-to-inductor Current Transfer Function 578
14.2.3 Open-loop Inductor-to-output Current Transfer Function 581
14.3 Open-loop Step Responses of Inductor Current 585
14.3.1 Open-loop Response of Inductor Current to Step Change in Input Voltage 585
14.3.2 Open-loop Response of Inductor Current to Step Change in Duty Cycle 588
14.3.3 Open-loop Response of Inductor Current to Step Change in Load Current 590
14.4 Closed-current-loop Transfer Functions 592
14.4.1 Input Voltage-to-duty Cycle Transfer Function 599
14.4.2 Load Current-to-duty Cycle Transfer Function 604
14.4.3 Output Impedance of Closed-current Loop 604
14.5 Closed-voltage-loop Transfer Functions 608
14.5.1 Control Voltage-to-feedback Voltage Function 608
14.5.2 Loop Gain of Voltage Loop 611
14.5.3 Closed-loop Gain of Voltage Loop 614
14.5.4 Closed-loop Audio Susceptibility with Integral Controller 616
14.5.5 Closed-loop Output Impedance with Integral Controller 619
14.6 Closed-loop Step Responses 620
14.6.1 Closed-loop Response of Output Voltage to Step Change in Input Voltage 620
14.6.2 Closed-loop Response of Output Voltage to Step Change in Load Current 620
14.6.3 Closed-loop Response of Output Voltage to Step Change in Reference Voltage 622
14.7 Closed-loop DC Transfer Functions 623
14.8 Summary 624
14.9 References 624
14.10 Review Questions 625
14.11 Problems 626

15 Silicon and Silicon Carbide Power Diodes 627

15.1 Introduction 627
15.2 Electronic Power Switches 627
15.3 Intrinsic Semiconductors 628
15.4 Extrinsic Semiconductors 630
15.5 Silicon and Silicon Carbide 631
15.6 Physical Structure of Junction Diodes 632
15.7 Static $I-V$ Diode Characteristic 634
15.8 Breakdown Voltage of Junction Diodes 637

15.8.1 Width of Depletion Region 638
15.8.2 Electric Field Distribution 639
15.8.3 Avalanche Breakdown Voltage 642
15.8.4 Punch-through Breakdown Voltage 642
15.8.5 Edge Terminations 644
15.9 Capacitances of Junction Diodes 645
15.9.1 Junction Capacitance 646
15.9.2 Diffusion Capacitance 648
15.10 Reverse Recovery of pn Junction Diodes 650
15.10.1 Qualitative Description 650
15.10.2 Reverse Recovery in Resistive Circuits 651
15.10.3 Charge-continuity Equation 654
15.10.4 Reverse Recovery in Inductive Circuits 657
15.11 Schottky Diodes 659
15.11.1 Static $I-V$ Characteristic of Schottky Diodes 661
15.11.2 Junction Capacitance of Schottky Diodes 662
15.11.3 Switching Characteristics of Schottky Diodes 663
15.12 SPICE Model of Diodes 666
15.13 Summary 667
15.14 References 669
15.15 Review Questions 670
15.16 Problems 670

16 Silicon and Silicon Carbide Power MOSFETs 673

16.1 Introduction 673
16.2 Physical Structure of Power MOSFETs 673
16.3 Principle of Operation of Power MOSFETs 677
16.3.1 Cutoff Region 677
16.3.2 Formation of Channel 677
16.3.3 Linear Region 678
16.3.4 Saturation Region 678
16.3.5 Antiparallel Diode 679
16.3.6 Integrated MOSFETs 679
16.4 Derivation of Power MOSFET Characteristics 679
16.4.1 Ohmic Region 679
16.4.2 Pinch-off Region 683
16.4.3 Channel-length Modulation 683
16.5 Power MOSFET Characteristics 684
16.6 Mobility of Charge Carriers 686
16.6.1 Effect of Doping Concentration on Mobility 687
16.6.2 Effect of Temperature on Mobility 689
16.6.3 Effect of Electric Field on Mobility 692
16.7 Short-channel Effects 697
16.8 Aspect Ratio of Power MOSFETs 698
16.9 Breakdown Voltage of Power MOSFETs 699
16.10 Gate Oxide Breakdown Voltage of Power MOSFETs 701
16.11 Resistance of Drift Region 701
16.12 Figures-of-merit 704
16.13 On-resistance of Power MOSFETs 705

16.13.1 Channel Resistance 705
16.13.2 Accumulation Region Resistance 707
16.13.3 Neck Region Resistance 707
16.13.4 Drift Region Resistance 708
16.14 Capacitances of Power MOSFETs 710
16.14.1 Gate-to-source Capacitance 710
16.14.2 Drain-to-source Capacitance 712
16.14.3 Gate-to-drain Capacitance 712
16.15 Switching Waveforms 723
16.16 SPICE Model of Power MOSFETs 724
16.17 Insulated Gate Bipolar Transistors 726
16.18 Heat Sinks 728
16.19 Summary 730
16.20 References 732
16.21 Review Questions 732
16.22 Problems 733

17 Soft-switching DC–DC Converters 735

17.1 Introduction 735
17.2 Zero-voltage-switching DC–DC Converters 736
17.3 Buck ZVS Quasi-resonant DC–DC Converter 736
17.3.1 Waveforms 736
17.3.2 DC Voltage Transfer Function 741
17.3.3 Voltage and Current Stresses 742
17.4 Boost ZVS Quasi-resonant DC–DC Converter 745
17.4.1 Waveforms 745
17.4.2 DC Voltage Transfer Function 748
17.4.3 Current and Voltage Stresses 749
17.4.4 Generalization 751
17.5 Zero-current-switching DC–DC Converters 751
17.6 Boost ZCS Quasi-resonant DC–DC Converter 753
17.6.1 Waveforms 753
17.6.2 Voltage Transfer Function 756
17.6.3 Current and Voltage Stresses 757
17.6.4 Generalization 759
17.7 Multiresonant Converters 759
17.8 Summary 761
17.9 References 762
17.10 Review Questions 763
17.11 Problems 764

Appendix A Introduction to SPICE 765

Appendix B Introduction to MATLAB 769

Answers to Problems 773

Index 779

Preface

This book is about switching-mode dc–dc power converters with pulse-width modulation (PWM) control. It is intended as a power electronics textbook at the senior and graduate levels for students majoring in electrical engineering, as well as a reference for practicing engineers in the area of power electronics. The purpose of the book is to provide the foundations for the study of semiconductor power devices, topologies of PWM switching-mode dc–dc power converters, modeling, dynamics, and controls of PWM converters.

The first part of the book covers topologies of transformerless and isolated PWM converters, such as buck, boost, buck-boost, flyback, forward, half-bridge, full-bridge, and push-pull converters. The second part covers small-signal circuit models of PWM converters, transfer functions of PWM converter power stages, voltage-mode control, and current-mode control of PWM converters. The third part presents semiconductor devices, such as silicon and silicon carbide power diodes, power MOSFETs, and IGBTs. The fourth and final part is devoted to soft-switching dc–dc PWM power converters.

The textbook assumes that the student is familiar with general circuit analysis techniques and electronic circuits. Complete solutions for all problems are included in the *Solutions Manual*, which is available from the publisher for those instructors who adopt the book for their courses.

I am pleased to express my gratitude to Nisha Das for MATLAB figures, proofreading, suggestions, and critical evaluation of the manuscript.

Throughout the entire course of this project, the support provided by John Wiley & Sons, Ltd was excellent. I wish to express my sincere thanks to Simone Taylor, Publisher, Laura Bell, Publishing Assistant, and Nicky Skinner, Project Editor, and Erica Peters, Content Editor. It has been a real pleasure working with them. Last but not least, I wish to thank my family for their support.

The author would welcome and greatly appreciate readers' suggestions and corrections for improvements of the technical content as well as the presentation style.

Marian K. Kazimierczuk

About the Author

Marian K. Kazimierczuk is Professor of Electrical Engineering at Wright State University, Dayton, Ohio, USA. He is the author of five books, over 130 journal papers, over 150 conference papers, and seven patents. He is a Fellow of the IEEE. He received the Outstanding Teaching Award from the American Society for Engineering Education in 2008. His research interests are in power electronics, including PWM dc–dc power converters, resonant dc–dc power converters, modeling and controls, RF power amplifiers and oscillators, semiconductor power devices, magnetic devices, and renewable energy sources.

List of Symbols

A	Transfer function of forward path in negative feedback system
A_i	Inductor-to-load current transfer function
A_J	Cross-sectional area of junction
C	Filter capacitance
C_b	Blocking capacitance
C_c	Coupling capacitance
C_{ds}	Drain-to-source capacitance of MOSFET
C_{gd}	Gate-to-drain capacitance of MOSFET
C_{gs}	Gate-to-source capacitance of MOSFET
C_{iss}	MOSFET input capacitance at $V_{DS} = 0$, $C_{iss} = C_{gs} + C_{gd}$
C_{min}	Minimum value of filter capacitance C
C_{oss}	MOSFET output capacitance at $V_{GD} = 0$, $C_{oss} = C_{gs} + C_{ds}$
C_o	Transistor output capacitance
C_{ox}	Oxide capacitance per unit area
C_{rss}	MOSFET transfer capacitance, $C_{rss} = C_{gd}$
d	AC component of on-duty cycle of switch
d_m	Amplitude of small-signal component of on-duty cycle of switch
d_T	Total on-duty cycle of switch
D	DC component of on-duty cycle of switch
f_p	Frequency of pole of transfer function
f_s	Switching frequency
f_0	Corner frequency
f_z	Frequency of zero of transfer function
H_{sh}	Transfer function of sampler and zero-order hold
i_i	AC component of input current
i_o	AC component of load current
i_D	Diode current
i_C	Current through filter capacitor C
i_L	Current through inductor L
i_O	Total load current
i_S	Switch current
I_{pk}	Magnitude of cross-conduction current
I_{rms}	RMS value of current i

I_{Crms}	RMS value of capacitor current i_C
I_D	Average diode current
I_{DM}	Peak diode current
I_{Drms}	RMS value of diode current
I_I	DC input current of converter
I_L	Average current through inductor L
I_{LB}	Average current through inductor L at the CCM/DCM boundary
I_O	DC output current of converter
I_{Omax}	Maximum value of dc load current I_O
I_{Omin}	Minimum value of dc load current I_O
I_{OB}	DC output current at the CCM/DCM boundary
I_{SM}	Peak switch current
I_{Srms}	RMS value of i_S
k	Boltzmann constant
K_i	Input feedforward gain
K_o	Output feedforward gain
L	Inductance, channel length
L_m	Magnetizing inductance of transformer
L_{max}	Maximum inductance L for DCM operation
L_{min}	Minimum inductance L for CCM operation
LNR	Line regulation
LOR	Load regulation
M_v	Open-loop input-to-output voltage function of converter
M_{vcl}	Closed-loop input-to-output voltage function of converter
M_{vi}	Open-loop input voltage-to-inductor current transfer function
M_{vo}	Open-loop input-to-output voltage function of converter at $f = 0$
$M_{I\,DC}$	DC current transfer function of converter
$M_{V\,DC}$	DC voltage transfer function of converter
n	Transformer turns ratio
n_i	Intrinsic carrier concentration
N_p	Number of turns of the primary winding
N_s	Number of turns of the secondary winding
N_A	Concentration of acceptors
N_D	Concentration of donors
P_{rC}	Conduction loss in filter capacitor ESR
PM	Phase margin
P_{ton}	Turn-on switching losses
P_D	Total diode conduction loss
P_{FET}	Overall power dissipation in MOSFET (excluding gate-drive power)
P_I	DC input power of converter
P_G	Gate-drive power
P_{LS}	Overall power dissipation of converter
P_O	DC output power of converter
P_{RF}	Conduction loss in diode forward resistance R_F
P_{VF}	Conduction loss in diode offset voltage V_F
PF	Power factor
Q	Quality factor
Q_g	Gate charge
Q_F	Forward stored charge
Q_{rr}	Reverse recovery charge

r_C	ESR of filter capacitor
r_{DS}	On-resistance of MOSFET
R_{DR}	Resistance of drift region
R_F	Diode forward resistance
R_L	DC load resistance
R_{LB}	DC load resistance at CCM/DCM boundary
R_{Lmax}	Maximum value of load resistance R_L
R_{Lmin}	Minimum value of load resistance R_L
S	Specific resistance of drift region
S_{max}	Maximum percentage overshoot
SR	Slew rate of op-amps
t_f	Fall time
t_r	Rise time
t_{rr}	Reverse recovery time
T	Switching period, loop gain
T_c	Voltage transfer function of controller
T_i	Loop gain of current loop
T_{cl}	Closed-loop control-to-output transfer function
T_m	Transfer function of pulse-width modulator
T_p	Open-loop control-to-output transfer function
T_{pi}	Open-loop duty cycle-to-inductor current transfer function
T_{po}	Open-loop control-to-output transfer function at $f = 0$
T_A	Ambient temperature
T_J	Junction temperature
THD	Total harmonic distortion
v_c	AC component of control voltage
v_e	AC component of error voltage
v_f	AC component of feedback voltage
v_i	AC component of converter input voltage
v_o	AC component of converter output voltage
v_{sat}	Saturation velocity of carriers
v_r	AC component of reference voltage
v_{rc}	Voltage across ESR of filter capacitor
v_{DS}	Drain-to-source voltage of MOSFET
v_L	Voltage across inductance L
v_o	AC component of output voltage
v_C	Total control voltage
v_C	Total error voltage
v_F	Total feedback voltage
v_O	Total output voltage
V_{bi}	Built-in potential
V_{cm}	Amplitude of small-signal component of control voltage
V_C	DC component of control voltage
V_{Cpp}	Peak-to-peak ripple voltage of the filter capacitance
V_E	DC component of error voltage
V_t	Gate-to-source threshold voltage
V_{BD}	Breakdown voltage
V_{BR}	Reverse blocking (breakdown) voltage
V_{DS}	Drain-to-source dc voltage of MOSFET
V_{DSS}	Drain-to-source breakdown voltage of MOSFETs

V_{DM}	Reverse peak voltage of diode
V_F	Diode offset voltage, dc component of feedback voltage
V_{GD}	Gate-to-drain voltage of MOSFET
V_{GSpp}	Peak-to-peak gate-to-source voltage
V_I	DC component of input voltage of converter
V_O	DC output voltage of converter
V_r	Peak-to-peak value of output ripple voltage
V_{rcpp}	Peak-to-peak ripple voltage across ESR
V_R	DC reference voltage
V_{SM}	Peak switch voltage
V_{Tm}	Peak ramp voltage of pulse-width modulator
W	Channel width
W_C	Energy stored in capacitor
W_L	Energy stored in inductor
Z_i	Open-loop input impedance of converter
Z_{icl}	Closed-loop input impedance of converter
Z_o	Open-loop output impedance of converter
Z_{ocl}	Closed-loop output impedance of converter
Δi_L	Peak-to-peak of inductor ripple current
β	Transfer function of feedback network
η	Efficiency of converter
θ	Thermal resistance
μ	Carrier mobility
μ_h	Mobility of holes
μ_n	Mobility of electrons
ξ	Damping ratio
ρ	Resistivity
σ	Conductivity, damping factor
τ	Minority carrier lifetime, time constant
ϕ	Phase of transfer function, magnetic flux
ψ	Initial phase
ω	Angular frequency
ω_c	Unity-gain angular crossover frequency
ω_d	Damped angular resonant frequency
ω_p	Angular frequency of simple pole
ω_z	Angular frequency of simple zero
ω_0	Corner angular frequency

1

Introduction

1.1 Classification of Power Supplies

Power supply technology is an enabling technology that allows us to build and operate electronic circuits and systems [1]–[24]. All active electronic circuits, both digital and analog, require power supplies. Many electronic systems require several dc supply voltages. Power supplies are widely used in computers, telecommunications, instrumentation equipment, aerospace, medical, and defense electronics. A dc supply voltage is usually derived from a battery or an ac utility line using a transformer, rectifier, and filter. The resultant raw dc voltage is not constant enough and contains a high ac ripple that is not appropriate for most applications. *Voltage regulators* are used to make the dc voltage more constant and to attenuate the ac ripple.

A power supply is a constant voltage source with a maximum current capability. There are two general classes of power supplies: *regulated* and *unregulated*. The output voltage of a regulated power supply is automatically maintained within a narrow range, 1–2 % of the desired nominal value, in spite of line voltage, load current, and temperature variations. Regulated dc power supplies are called *dc voltage regulators*. There are also *dc current regulators*, such as battery chargers.

Figure 1.1 shows a classification of regulated power supply technologies. Two of the most popular categories of voltage regulators are *linear regulators* and *switching-mode power supplies*. There are two basic linear regulator topologies: the series voltage regulator and the shunt voltage regulator. The switching-mode voltage regulators are divided into three categories: pulse-width modulated (PWM) dc–dc converters, resonant dc–dc converters, and switched-capacitor (also called charge-pump) voltage regulators. In linear voltage regulators, transistors are operated in the active region as dependent current sources with relatively high voltage drops at high currents, dissipating a large amount of power and resulting in low efficiency. Linear regulators are heavy and large, but they exhibit low noise level and are suitable for audio applications.

In switching-mode converters, transistors are operated as switches, which inherently dissipate much less power than transistors operated as dependent current sources. The voltage

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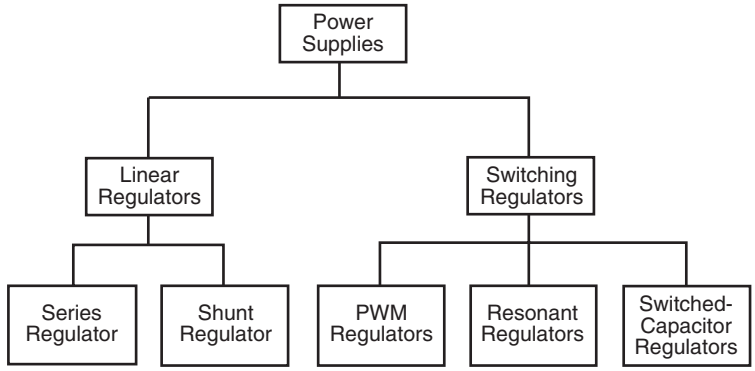


Figure 1.1 Classification of power supply technologies.

drop across the transistors is very low when they conduct high current and the transistors conduct a nearly zero current when the voltage drop across them is high. Therefore, the conduction losses are low and the efficiency of switching-mode converters is high, usually above 80–90 %. However, switching losses reduce the efficiency at high frequencies. Switching losses increase proportionally to switching frequency. Linear and switched-capacitor regulator circuits (except for large capacitors) can be fully integrated and are used in low-power and low-voltage applications, usually below several watts and 50 V. PWM and resonant regulators are used at high power and voltage levels. They are small in size, light in weight, and have high conversion efficiency.

Figure 1.2 shows block diagrams of two typical ac–dc power supplies that convert the widely available ac power to dc power. The power supply of Figure 1.2(a) contains a dc linear voltage regulator, whereas the power supply of Figure 1.2(b) contains a switching-mode voltage regulator. The power supply shown in Figure 1.2(a) consists of a low-frequency step-down power line transformer, a front-end rectifier, a low-pass filter, a linear voltage regulator, and a load. The nominal voltage of the ac utility power line is 110 Vrms in the USA and 220 Vrms in Europe. However, the actual line voltage varies within a range of about ±20 % of the nominal voltage. The frequency of the ac line voltage is very

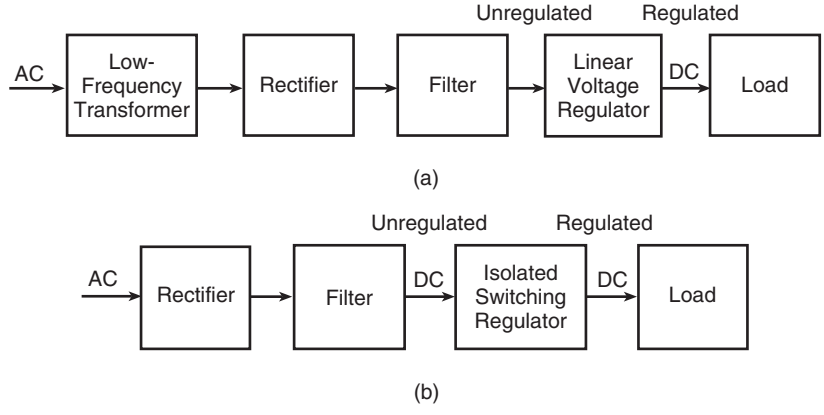


Figure 1.2 Block diagrams of ac–dc power supplies. (a) With a linear regulator. (b) With a switching-mode voltage regulator.

low (50 Hz in Europe, 60 Hz in USA, 400 Hz in aircraft applications, and 20 kHz in space applications). The line transformer provides dc isolation from the ac power line and reduces a relatively high line voltage to a lower voltage (ranging usually from 5 to 28 Vrms). Since the frequency of the ac line voltage is very low, the line transformer is heavy and bulky. The output voltage of the front-end rectifier/filter is unregulated and it varies because the peak voltage of the ac line varies. Therefore, a voltage regulator is required between the rectifier/filter and the load. There still exists a need for *universal power supplies* that can accept any utility line voltage in the world, ranging from 85 to 264 Vrms.

The power supply shown in Figure 1.2(b) consists of a front-end rectifier, a low-pass filter, an isolated dc–dc switching-mode voltage regulator, and a load. It is run directly from the ac line. The ac voltage is rectified directly from the ac power line, which does not require a bulky low-frequency line transformer. Hence, such a circuit is called an *off-line power supply* (plug into the wall). The switching-mode voltage regulator contains a high-frequency transformer to obtain dc isolation for the entire power supply. Since the switching frequency is much higher than that of the ac line frequency, the size and weight of a high-frequency transformer as well as inductors and capacitors is reduced. The switching frequency usually ranges from 25 to 500 kHz. To avoid audio noise, the switching frequency should be above 20 kHz. A PWM switching-mode voltage regulator generates a high-frequency rectangular voltage wave, which is rectified and filtered. The duty cycle (or the pulse width) of the rectangular wave is varied to control the dc output voltage. Therefore, these voltage regulators are called PWM dc–dc converters.

Power converters are required to convert one form of electric energy to another. A dc–dc converter is a power supply that converts a dc input voltage into a desired regulated dc output voltage. The dc input may be an unregulated or regulated voltage. Often, the input of a dc–dc converter is a battery or a rectified ac line voltage. A voltage regulator should provide a constant voltage to the load, even if line voltage, load current, and temperature vary. Unlike in linear voltage regulators, the output voltage in PWM dc–dc converters may be either lower or higher than the input voltage, resulting in *step-down* or *step-up* converters. In a step-down converter, the output voltage is lower than the input voltage. In a step-up converter, the output voltage is higher than the input voltage. Some converters may act as both step-down and step-up converters. The output voltage source may be of the same polarity (noninverting) or opposite polarity (inverting) to that of the polarity of the input voltage. The dc–dc converters may have *common negative* or *common positive* input and output terminals. Converters may have a *single output* or *multiple outputs*. In addition, there are *fixed* and *adjustable* output voltage power supplies. Fixed output voltage supplies (e.g., 1.8 V) are used for power electronic circuits that require a specific supply voltage. Power supplies with adjustable output voltage (e.g., from 0 to 30 V) are convenient for laboratory tests. In some applications, *programmable* power supplies with digitally selected output voltages are required. Power supplies may be *nonisolated* or *isolated*. Transformers can be used to obtain dc isolation between the input and output and between the different outputs. Common requirements of most power supplies are: high efficiency, high power density, high reliability, and low cost.

1.2 Basic Functions of Voltage Regulators

The simplest voltage regulator is a Zener diode regulator, shown in Figure 1.3. It is a shunt regulator. However, the performance of the Zener diode regulator is not satisfactory for most applications. Therefore, negative feedback techniques are usually used in voltage regulators to improve the performance. A block diagram of a voltage regulator with negative

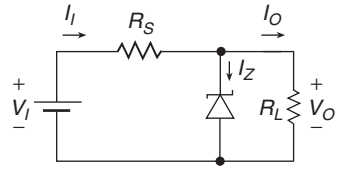


Figure 1.3 Zener diode voltage regulator.

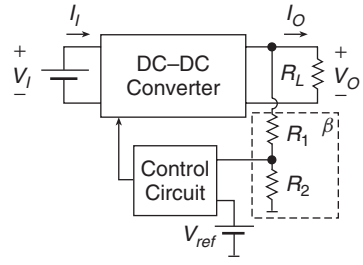


Figure 1.4 Block diagram of a voltage regulator with negative feedback.

feedback is shown in Figure 1.4. It consists of a power stage (a dc–dc converter), a feedback network, a reference voltage V_{ref}, and a control circuit (also called an error amplifier). The feedback network monitors the output voltage and reduces the error signal. The control circuit compares the feedback voltage with the reference voltage, generates an error voltage, amplifies it, and adjusts the transistor base current to keep the output voltage V_O constant.

The load current I_O may vary over a very wide range: $I_{Omin} \leq I_O \leq I_{Omax}$. Consequently, the load resistance $R_L = V_O/I_O$ also varies over a wide range: $R_{Lmin} \leq R_L \leq R_{Lmax}$, where $R_{Lmin} = V_O/I_{Omax}$ and $R_{Lmax} = V_O/I_{Omin}$. Most regulated power supplies have a short-circuit or current-overload protection circuit, which limits the output current to a safe level to protect the power supply and/or the load. The input voltage of a voltage regulator is usually unregulated and can vary over a wide range: $V_{Imin} \leq V_I \leq V_{Imax}$. For example, the dc input voltage in telecommunications power supplies is $36 \leq V_I \leq 72\,\text{V}$ with a nominal input voltage $V_{Inom} = 48\,\text{V}$. The input voltage source may be a battery, a rectified single-phase or three-phase ac line voltage. The output voltage of a battery decreases when the battery is discharged. The peak voltage of a utility line varies as much as 10–20 %, causing the rectified dc voltage to vary. The operating temperature of semiconductor and passive devices may also change from T_{min} to T_{max}, affecting the performance of power supplies.

The basic functions of a dc–dc converter are as follows:

- to provide conversion of a dc input voltage V_I to the desired dc output voltage within a tolerance range (e.g., $V_O = 1.2\,\text{V} \pm 1\,\%$);
- to regulate the output voltage V_O against variations in the input voltage V_I, the load current I_O (or the load resistance R_L), and the temperature;
- to reduce the output ripple voltage below the specified level;
- to ensure fast response to rapid changes in the input voltage and load current (or load resistance);
- to provide dc isolation;

- to provide multiple outputs;
- to minimize the electromagnetic interference (EMI) below levels specified by EMI standards.

1.3 Power Relationships in DC–DC Converters

The input current i_I of many switching-mode dc–dc converters is pulsating. The dc component of the converter input current is given by

$$I_I = \frac{1}{T}\int_0^T i_I\, dt. \tag{1.1}$$

Hence, the dc input power of a dc–dc converter is

$$P_I = \frac{1}{T}\int_0^T V_I i_I\, dt = V_I \frac{1}{T}\int_0^T i_I\, dt = V_I I_I. \tag{1.2}$$

The ac components of the output voltage and current are assumed to be very small and can be neglected. Therefore, dc output power of a dc–dc converter is

$$P_O = V_O I_O \tag{1.3}$$

and the power loss in the converter is

$$P_{LS} = P_I - P_O. \tag{1.4}$$

The efficiency of the dc–dc converter is

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} \tag{1.5}$$

from which

$$\frac{P_{LS}}{P_O} = \left(\frac{1}{\eta} - 1\right). \tag{1.6}$$

The normalized power loss P_{LS}/P_O decreases as the converter efficiency increases. For example, for $\eta = 25\,\%$, $P_{LS}/P_O = 300\,\%$, but for $\eta = 95\,\%$, $P_{LS}/P_O = 5.26\,\%$.

1.4 DC Transfer Functions of DC–DC Converters

The dc voltage transfer function (also called the dc voltage conversion ratio or the dc voltage gain) of a dc–dc converter is

$$M_{V\,DC} = \frac{V_O}{V_I} \tag{1.7}$$

and the dc current transfer function of a dc–dc converter is

$$M_{I\,DC} = \frac{I_O}{I_I}. \tag{1.8}$$

Hence, the efficiency of a dc–dc converter is

$$\eta = \frac{P_O}{P_I} = \frac{I_O V_O}{I_I V_I} = M_{I\,DC} M_{V\,DC}. \tag{1.9}$$

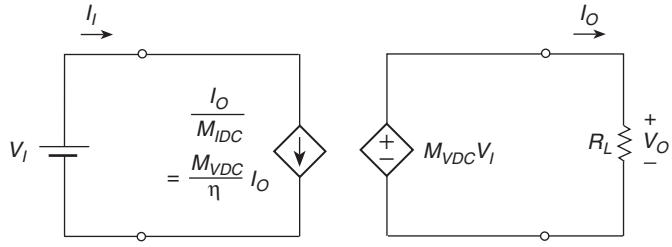


Figure 1.5 A dc model of a dc–dc converter.

From (1.7), (1.8), and (1.9),

$$V_O = M_{V\,DC} V_I \tag{1.10}$$

and

$$I_I = \frac{I_O}{M_{I\,DC}} = \frac{M_{V\,DC}}{\eta} I_O. \tag{1.11}$$

These equations can be represented by the dc circuit model of a dc–dc converter shown in Figure 1.5.

1.5 Static Characteristics of DC Voltage Regulators

Static characteristics of voltage regulators are described by three parameters: line regulation, load regulation, and thermal regulation. The output voltage V_O of most voltage regulators increases as the input voltage V_I increases, as shown in Figure 1.6. Therefore, one figure-of-merit of voltage regulators for steady-state operation is *line regulation*, which is a measure of the regulator's ability to maintain the predescribed nominal output voltage V_{Onom} under slowly varying input voltage conditions.

The *line regulation* is the ratio of the output voltage change ΔV_O to a corresponding change in the input voltage

$$LNR = \left(\frac{\Delta V_O}{\Delta V_I}\right)\Bigg|_{I_O=Const \text{ and } T_A=Const} \left(\frac{\text{mV}}{\text{V}}\right). \tag{1.12}$$

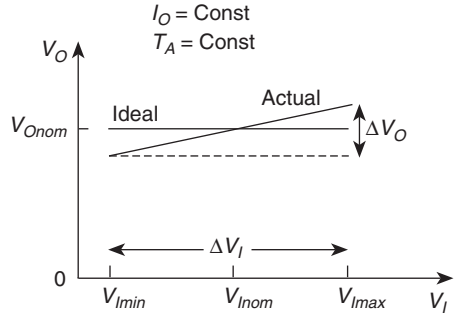


Figure 1.6 Output voltage V_O versus input voltage V_I for voltage regulators, illustrating line regulation.

For example, for an LM140 linear voltage regulator, $\Delta V_O = 10\,\text{mV}$ at $I_O = 0.5\,\text{A}$, $T_A = 25\,^\circ\text{C}$, and $7.5\,\text{V} \leq V_I \leq 20\,\text{V}$. Hence, $LNR = 10/(20 - 7.5) = 0.8\,\text{mV/V}$.

The *percentage line regulation* is defined as the ratio of the percentage change in the output voltage to a corresponding change in the input voltage,

$$PLNR = \left.\frac{\dfrac{\Delta V_O}{V_{Onom}} \times 100\,\%}{\Delta V_I}\right|_{I_O=Const \text{ and } T_A=Const} \left(\frac{\%}{\text{V}}\right), \tag{1.13}$$

where T_A is the ambient temperature. Ideally, the line regulation should be zero, in which case the output voltage is independent of the input voltage. For example, for an LM317 linear voltage regulator, the typical value of the line regulation is $PLNR = 0.01\,\%/\text{V}$ at $I_O = 20\,\text{mA}$, $T_A = 25\,^\circ\text{C}$, and $3\,\text{V} \leq V_I - V_O \leq 40\,\text{V}$.

The output voltage V_O of voltage regulators decreases as the load current I_O increases due to a varying load resistance, as shown in Figure 1.7. Hence, the second figure-of-merit of voltage regulators for steady-state operation is *load regulation*, which is a measure of the regulator's ability to maintain a constant output voltage V_{Onom} under slowly varying load conditions over a certain range of load current, usually from zero load current to a maximum load current I_{Omax}.

The *load regulation* is given by

$$LOR = \left.\frac{\Delta V_O}{\Delta I_O}\right|_{V_I=Const \text{ and } T_A=Const} \left(\frac{\text{mV}}{\text{A}}\right). \tag{1.14}$$

The *percentage load regulation* for voltage regulators that have no minimum load requirement is defined as

$$PLOR = \left.\frac{V_{O(NL)} - V_{O(FL)}}{V_{O(FL)}} \times 100\,\%\right|_{V_I=Const \text{ and } T_A=Const} (\%), \tag{1.15}$$

where $V_{O(NL)}$ is the no-load (open-circuit) output voltage and $V_{O(FL)}$ is the full-load output voltage, which corresponds to a maximum load current I_{Omax}. In some voltage regulators, such as PWM converters operated in the continuous conduction mode, the minimum load current I_{Omin} is not zero. The output voltage at the minimum load current is $V_{O(minL)}$. In this case, the load regulation is defined as

$$PLOR = \left.\frac{V_{O(minL)} - V_{O(FL)}}{V_{O(FL)}} \times 100\,\%\right|_{V_I=Const \text{ and } T_A=Const} (\%). \tag{1.16}$$

For an ideal voltage regulator, the load regulation is zero. For example, for an LM117 linear voltage regulator, $PLOR_2 = 0.3\,\%$ for $5\,\text{mA} \leq I_O \leq 100\,\text{mA}$ and $T_A = 25\,^\circ\text{C}$.

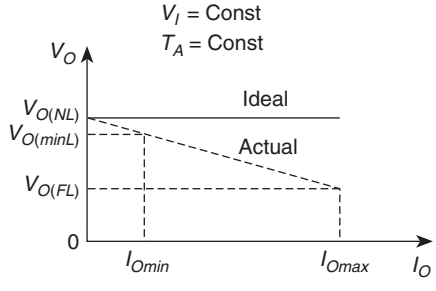


Figure 1.7 Output voltage V_O versus output current I_O for voltage regulators, illustrating load regulation.

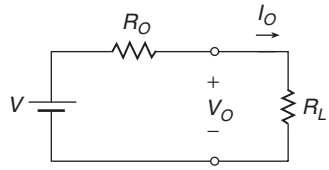


Figure 1.8 DC model of voltage source with an output resistance.

The line regulation and the load regulation can be combined into a *line/load regulation*

$$LLR = \left.\frac{\dfrac{\Delta V_O}{V_{Onom}} \times 100\,\%}{\Delta I_O}\right|_{V_I=Const \text{ and } T_A=Const} \left(\frac{\%}{\text{A}}\right). \tag{1.17}$$

Sometimes power supply manufacturers specify the equivalent dc output resistance R_o. A dc model of a real voltage source consists of an ideal voltage source V and an output resistance R_o, as shown in Figure 1.8. The output voltage is given by

$$V_O = V - R_o I_O, \tag{1.18}$$

from which

$$\Delta V_O = -R_o \Delta I_O. \tag{1.19}$$

Hence, the *incremental* or *dynamic output resistance* is defined as the ratio of change in the output voltage to the corresponding change in the load current

$$R_o = -\frac{\Delta V_O}{\Delta I_O} = -LOR. \tag{1.20}$$

When $I_{Omin} = 0$, the dc output resistance is given by

$$R_o = \frac{V_{O(NL)} - V_{O(FL)}}{I_{Omax}}. \tag{1.21}$$

The output resistance of a voltage regulator should be as low as possible so that a change in the output current ΔI_O will result only in a small change in the output voltage $\Delta V_O = -R_o \Delta I_O$. Ideally, R_o should be zero, resulting in an output voltage that is independent of the load current. At high frequencies (or for fast changes in the load current), the output resistance has a complex output impedance. From Figure 1.8, the output voltage at the full load resistance $R_{FL} = R_{Lmin}$ is

$$V_{O(FL)} = V_{O(NL)} \frac{R_{FL}}{R_o + R_{FL}}. \tag{1.22}$$

Hence, the percentage load regulation can be expressed as

$$PLOR = \frac{V_{O(NL)} - V_{O(FL)}}{V_{O(NL)}} \times 100\,\% = \frac{V_{O(FL)}\left(\dfrac{R_o + R_{FL}}{R_{FL}}\right) - V_{O(FL)}}{V_{O(FL)}} \times 100\,\%$$

$$= \frac{R_o}{R_{FL}} \times 100\,\%. \tag{1.23}$$

A very low output resistance can be obtained by using negative feedback with shunt connection of the power stage and the feedback network at the output. The relationship between the open-loop output resistance R_o and the closed-loop output resistance R_{of} is

$$R_{of} = \frac{R_o}{1 + \beta A} \tag{1.24}$$

where A is the dc (or low-frequency) voltage gain of the forward path and β is the transfer function of the feedback network.

A third figure-of-merit of voltage regulators is the *thermal regulation* defined as

$$THR = \left.\frac{\dfrac{\Delta V_O}{V_{Onom}} \times 100\,\%}{\Delta P_D}\right|_{I_O=Const \text{ and } V_I=Const} \left(\frac{\%}{\text{W}}\right) \tag{1.25}$$

where ΔP_D is the change in power dissipation. For example, for an LM317 linear voltage regulator, $THR = 0.04\,\%/\text{W}$.

The *static* or *dc input resistance* of a dc voltage regulator at a given operating point Q is

$$R_{in(DC)} = \frac{V_I}{I_I}. \tag{1.26}$$

Since

$$P_O = \frac{V_O^2}{R_L} \tag{1.27}$$

and

$$P_I = \frac{V_I^2}{R_{in(DC)}}, \tag{1.28}$$

the converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{\dfrac{V_O^2}{R_L}}{\dfrac{V_I^2}{R_{in(DC)}}} = \left(\frac{V_O}{V_I}\right)^2 \frac{R_{in(DC)}}{R_L} = M_{V\,DC}^2 \frac{R_{in(DC)}}{R_L}. \tag{1.29}$$

Hence, one obtains the dc input resistance of dc voltage regulators as a function of load resistance R_L and the dc–dc voltage transfer function

$$R_{in(DC)} = \frac{\eta R_L}{M_{V\,DC}^2}. \tag{1.30}$$

1.6 Dynamic Characteristics of DC Voltage Regulators

Voltage regulators should minimize the amount of ripple voltage at the output. The parameter that describes this feature is called the *ripple rejection ratio*, defined as

$$RRR = \frac{V_{ri}}{V_r}, \tag{1.31}$$

where V_r is the output ripple resulting from an input ripple V_{ri}. For example, for an LM317 linear voltage regulator, $RRR = 80\,\text{dB} = 10^4$ at $f = 120\,\text{Hz}$. If the input ripple $V_{ri} = 1\,\text{V}$, then the output ripple is $V_r = V_{ri}/RRR = 1/10^4 = 0.1\,\text{mV}$.

Dynamic transient performance of voltage regulators is described by *line transient response* and *load transient response*. In general, transient response is the shape of a signal as it moves between two steady-state points.Figure 1.9 shows a circuit for testing line transient response of voltage regulators. A test is made at a fixed load current I_O, usually 50 % of its rated full-load current I_{Omax}. The input voltage v_I contains step changes of magnitude Δv_I superimposed on its dc component V_I, as shown in Figure 1.10(a). As a result, the output voltage v_O contains transients just after the step changes in the input voltage, as

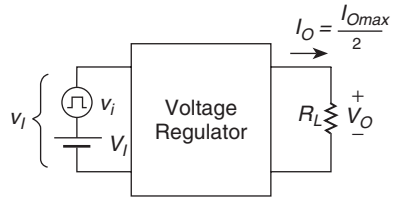


Figure 1.9 Circuit for testing the line transient response of voltage regulators.

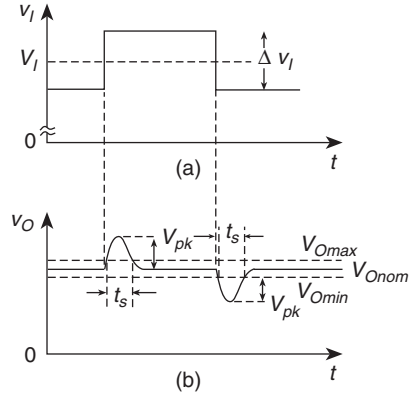


Figure 1.10 Waveforms illustrating line transient response of voltage regulators. (a) Waveform of the input voltage v_I. (b) Waveform of the output voltage v_O.

shown in Figure 1.10(b). When the input voltage v_I abruptly increases, the output voltage v_O also increases initially and then returns to a steady-state value. On the other hand, when the input voltage v_I abruptly decreases, the output voltage also decreases initially and then returns to a steady-state value. The abrupt change in the input voltage may cause an oscillatory (or underdamped) response characterized by overshoot and undershoot through the limits of a static regulation band. The response may be overdamped or critically damped. A closed-loop step response should be nonoscillatory. An oscillatory step response of a closed-loop circuit indicates that the margins of stability are too low or the circuit is unstable. The settling time t_s and the transient component V_{pk} should be below the specified levels.

Figure 1.11 shows a circuit for testing a load transient response. The input voltage V_I is held constant, usually at the nominal value V_{Inom}. Step changes in the load current are obtained using an active load that acts like a current sink. Its waveform is a square wave

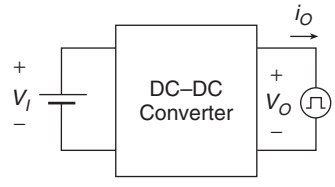


Figure 1.11 Circuit for testing the load transient response using an active current sink.

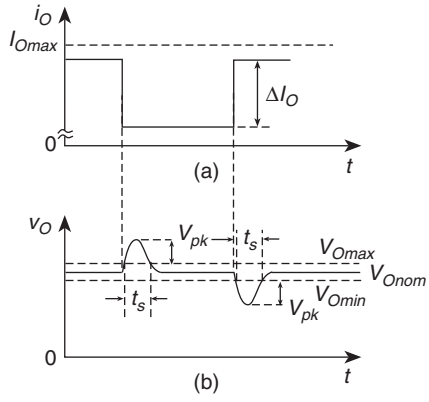


Figure 1.12 Waveforms illustrating load transient response of voltage regulators. (a) Waveform of the load current i_O. (b) Waveform of the output voltage v_O.

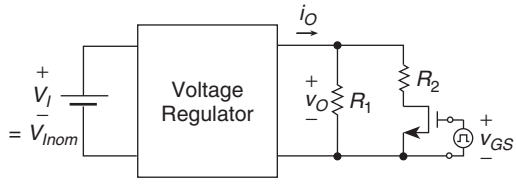


Figure 1.13 Circuit for testing the load transient response with a switched load resistance from R_1 to $R_1||R_2$ using a Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET).

with a dc offset, as shown in Figure 1.12(a). The step changes in the load current cause a transient response in the converter output voltage. When the load current is abruptly decreased, the output voltage initially increases and then returns to its steady-state value. The two parameters of output voltage are the peak transient voltage V_{pk} and the settling time t_s. The settling time t_s should be less than 200–500 ms and V_{pk} should be below a specified value. Usually, nonoscillatory response is expected in closed-loop power supplies to ensure sufficient stability margins.

Another circuit for testing the load transient response is shown in Figure 1.13. The input voltage V_I is held constant, usually at the nominal value V_{Inom}. A step change in the load current may be obtained by switching the load resistance R_L. A resistor R_1 is connected in parallel with a series combination of a resistor R_2 and a fast switch (e.g., a power MOSFET). If the switch is OFF, the load resistance is high, equal to $R_{L1} = R_1$, and the steady-state load current is low, equal to $I_{O1} = V_O/R_{L1}$. If the switch is ON, the load resistance is low, equal to $R_{L2} = R_1R_2/(R_1 + R_2)$, and the steady-state load current is high, equal to $I_{O2} = V_O/R_{L2}$. Therefore, when the load resistance is switched from R_{L1} to R_{L2} and vice versa, the load current i_O experiences step changes in magnitude ΔI_O superimposed on the dc load current I_O (e.g., from $0.1I_{Omax}$ to $0.9I_{Omax}$). This causes the output voltage to change just after the step change in the load current, as shown in Figure 1.12(b). When the load current i_O abruptly increases, the output voltage v_O initially decreases and then returns to a steady-state value and vice versa. In general, the response may be underdamped (or oscillatory), critically damped, or overdamped, but a nonoscillatory response is normally required.

Many voltage regulators are operated with a constant load resistance R_L (or a constant load current I_O) for relatively long time intervals. In addition, these regulators have a

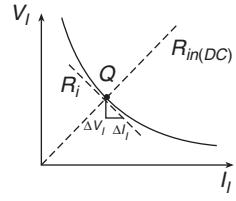


Figure 1.14 Voltage–current characteristic of a constant power source.

negative feedback controller, which maintains a constant output voltage V_O. Therefore, the dc output power $P_O = V_O^2/R_L$ is also constant. Such operating conditions are called constant power load. If the output power P_O and the efficiency η are constant, the input power $P_I = P_O/\eta = V_I I_I$ is also constant. The dc input voltage of a dc voltage regulator can be expressed by

$$V_I = \frac{P_I}{I_I} = \frac{P_O}{\eta I_I}. \tag{1.32}$$

Figure 1.14 shows a plot of the input voltage V_I as a function of the dc input current I_I at a constant output power P_O. If the input voltage V_I is increased, the input current $I_I = P_I/V_I$ decreases under constant power load conditions. Therefore, the slope of the I_I–V_I characteristic is negative at any operating point Q. The *dynamic input resistance* (also called the *ac* or *incremental input resistance*) of the voltage regulator with a constant input power P_I for slow changes of the input voltage and current at a given operating point Q (i.e., for low frequencies) is given by

$$R_i = \frac{d(V_I)}{dI_I} = \frac{d}{dI_I}\left(\frac{P_I}{I_I}\right) = -\frac{P_I}{I_I^2} = -\frac{V_I}{I_I} = -R_{in(DC)}. \tag{1.33}$$

Note that for a constant input power, the dynamic input resistance is just the negative of the static input resistance. The dynamic input resistance of a voltage regulator with a constant output power P_O and a constant efficiency η is

$$R_i = \frac{d(V_I)}{dI_I} = \frac{d}{dI_I}\left(\frac{P_O}{\eta I_I}\right) = \frac{P_O}{\eta}\frac{d}{dI_I}\left(\frac{1}{I_I}\right) = -\frac{P_O}{\eta I_I^2} = -\frac{R_L I_O^2}{\eta I_I^2}. \tag{1.34}$$

From (1.9), one obtains

$$\frac{I_O}{I_I} = \eta\frac{V_I}{V_O} = \frac{\eta}{\dfrac{V_O}{V_I}} = \frac{\eta}{M_{V\,DC}}. \tag{1.35}$$

Substitution of (1.35) into (1.34) produces

$$R_i = -\frac{\eta R_L}{M_{V\,DC}^2}. \tag{1.36}$$

It can be seen that the dynamic input resistance of a dc voltage regulator with a constant power load is negative and directly proportional to the load resistance R_L.

1.7 Linear Voltage Regulators

There are two basic topologies of linear voltage regulators: the series voltage regulator and the shunt voltage regulator. These topologies are shown in Figure 1.15. A band-gap

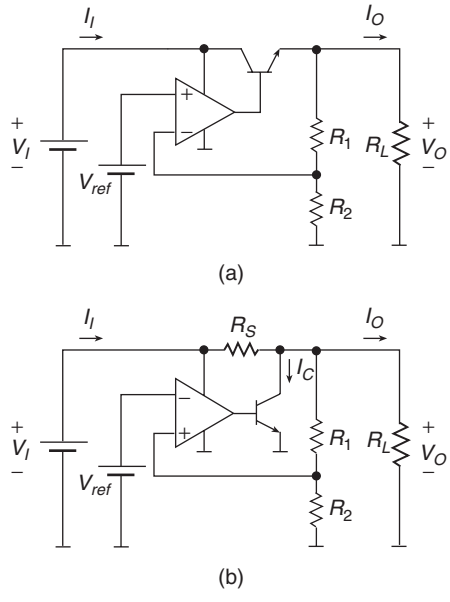


Figure 1.15 Basic circuits of linear voltage regulators. (a) Series voltage regulator. (b) Shunt voltage regulator.

reference voltage source V_{ref} is applied to the noninverting input of the op-amp. The input voltage of the op-amp is the difference between the noninverting input voltage V^+ and the inverting input voltage V^- given by $V_{i(op\text{-}amp)} = V^+ - V^-$. Since the input voltage of an op-amp with negative feedback is almost zero, the voltage across the resistor R_2 is controlled by the reference voltage source V_{ref}. Thus,

$$V_{R2} = V_O \frac{R_2}{R_1 + R_2} \approx V_{ref}. \tag{1.37}$$

Rearrangement of this equation gives the output voltage for both linear voltage regulators

$$V_O \approx V_{ref}\left(\frac{R_1}{R_2} + 1\right). \tag{1.38}$$

The range of the output current of linear voltage regulators is from 0 to a maximum value I_{Omax}, usually determined by a current limiting circuit.

1.7.1 Series Voltage Regulator

The series voltage regulator is shown in Figure 1.15(a). It employs a *pass transistor* whose collector-to-emitter voltage V_{CE} is controlled to compensate for varying the input voltage. Referring to Figure 1.15(a),

$$V_I = V_{CE} + V_O. \tag{1.39}$$

Since V_O is constant,

$$\Delta V_I = \Delta V_{CE}. \tag{1.40}$$

Thus, a change in the input voltage will result in the same change in the voltage drop across the pass transistor. The pass transistor behaves like a variable resistor R_v. The series

voltage regulator can be represented as a voltage divider composed of the variable resistor R_v and the load resistor R_L. When the output voltage V_O decreases, the variable resistance also decreases, causing the output voltage across the load resistance to increase, and *vice versa*. The voltage drop across R_v can be expressed as

$$V_{CE} = V_I - V_O = R_v I_O. \tag{1.41}$$

At a fixed load current I_O, a change in the input voltage is given by

$$\Delta V_{CE} = \Delta V_I = \Delta R_v I_O. \tag{1.42}$$

When the input voltage is changed by ΔV_I, the resistance is changed by $\Delta R_v = \Delta V_I / I_O$.

The efficiency of a series voltage regulator can be derived by observing that $I_O \approx I_I$

$$\eta = \frac{P_O}{P_I} = \frac{I_O V_O}{I_I V_I} \approx \frac{V_O}{V_I} = M_{V\,DC}. \tag{1.43}$$

It can be seen that the efficiency of a series voltage regulator is equal to the dc voltage transfer function $M_{V\,DC}$. If the input voltage V_I is much higher than the output voltage V_O, the efficiency is very low. For example, if $V_I = 20\,\text{V}$ and $V_O = 5\,\text{V}$, then $\eta = 5/20 = 25\,\%$. This is a very low efficiency. However, if $V_I = 8\,\text{V}$ and $V_O = 5\,\text{V}$, then $\eta = 5/8 = 62.5\,\%$. The power loss in the pass transistor is expressed by

$$P_{LS} \approx I_O(V_I - V_O). \tag{1.44}$$

Thus, the power loss increases with increasing load current I_O and the voltage drop across the pass transistor $\Delta V = V_I - V_O$.

The series voltage regulator will work properly as long as V_I does not drop too low, which causes the op-amp to saturate. The op-amp must be in the linear region to function properly as a control circuit. The minimum voltage difference between the unregulated input voltage and the regulated output voltage $V_{DO} = V_{Imin} - V_O$ at which the circuit ceases to regulate against further reduction in the input voltage is called the *drop-out voltage*. For most series voltage regulators, this voltage is about 2 V, but in some voltage regulators V_{DO} can be as low as 0.1 V. Voltage regulators with a low drop-out (LDO) voltage are called LDO regulators. In these regulators, a pnp or an n-channel power MOSFET (NMOS) transistor is used as a pass component, as shown in Figure 1.16.

1.7.2 Shunt Voltage Regulator

The shunt voltage regulator is shown in Figure 1.15(b). It employs a shunt transistor, in which the current is controlled to compensate for the change in the input voltage or the load current. The output voltage is held constant by varying the collector current I_C of

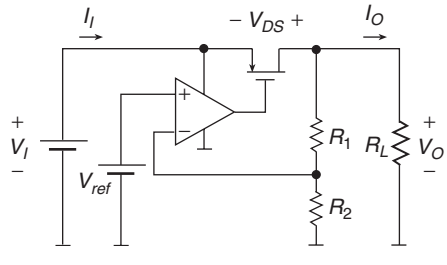


Figure 1.16 Typical low drop-out voltage regulator topology.

the shunt transistor. The shunt transistor acts like a variable resistor. When the output voltage V_O decreases, the op-amp output voltage also decreases, the shunt transistor conducts less heavily, and the variable resistance increases. Thus, less current is diverted from the load, causing an increase in the load current and the output voltage. Using Kirchhoff's current law,

$$I_I = I_C + I_O. \tag{1.45}$$

When the load current I_O is changed at a fixed input voltage V_I, the input current $I_I = (V_I - V_O)/R_s$ is constant and therefore

$$\Delta I_C = -\Delta I_O. \tag{1.46}$$

Equation (1.45) can be rewritten as

$$\frac{V_I - V_O}{R_s} = I_C + I_O. \tag{1.47}$$

When the input voltage changes at a fixed load current I_O,

$$\frac{\Delta V_I}{R_s} = \Delta I_C, \tag{1.48}$$

from which

$$\Delta V_I = R_s \Delta I_C = \Delta V_{Rs}. \tag{1.49}$$

Thus, the output voltage V_O is held constant by varying the voltage drop across the series resistor R_s, which in turn is controlled by varying the collector current I_C of the shunt transistor.

The shunt regulator is inherently short-circuit-proof. The output current under short-circuit conditions is given by

$$I_{O(sc)} = \frac{V_I}{R_s}. \tag{1.50}$$

The power loss in resistor R_s is

$$P_{Rs} = (V_I - V_O)I_I = (V_I - V_O)(I_O + I_C). \tag{1.51}$$

The power loss in the shunt transistor is

$$P_Q = V_O I_C = V_O(I_I - I_O), \tag{1.52}$$

and the efficiency is defined as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{V_O}{V_I} \frac{I_O}{I_O + I_C}. \tag{1.53}$$

Thus, the shunt voltage regulator is less efficient than the series voltage regulator due to the power loss in both series resistor R_s and shunt transistor. However, the line transient response of the shunt regulator is better than that of the series regulator. The shunt voltage regulator must be protected against input overvoltage conditions.

The major characteristics of linear voltage regulators are as follows:

- simple circuit;
- very small size and low weight;
- cost-effective;
- low noise level;

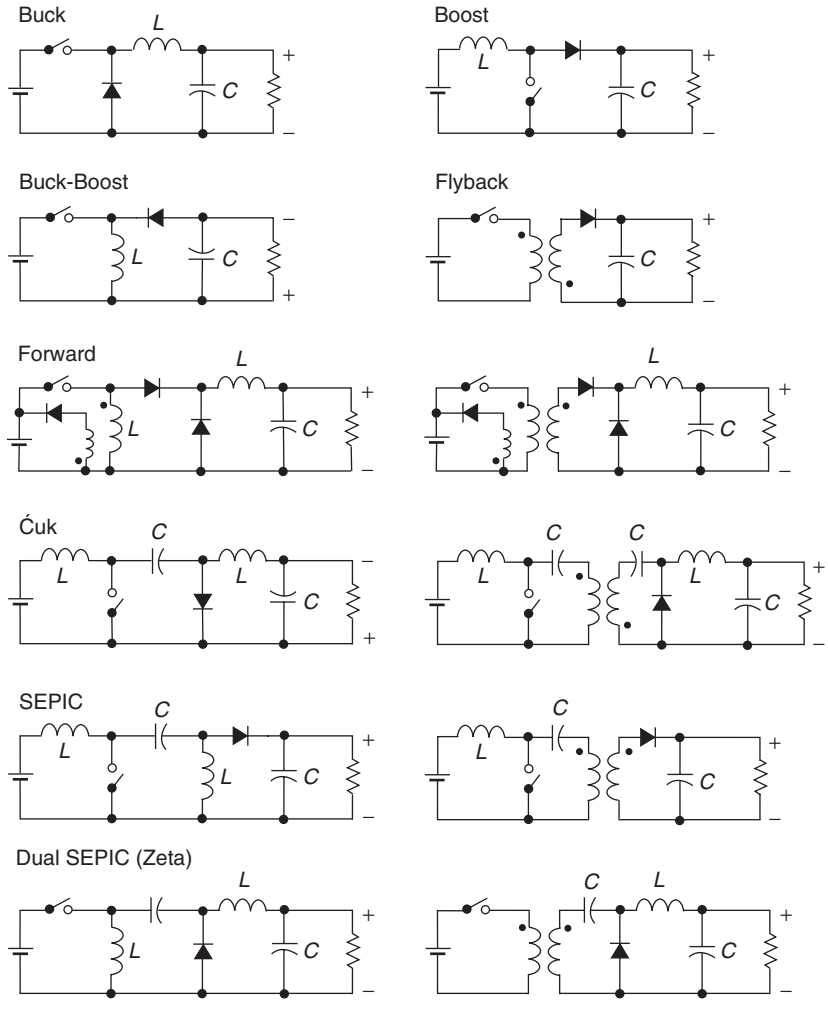


Figure 1.17 Single-ended PWM dc–dc nonisolated and isolated converters.

- wide bandwidth and fast step response;
- low input and output voltages, usually below 40 V;
- low output current, usually below 3 A;
- low output power, usually below 25 W;
- low efficiency (especially for $V_I \gg V_O$), usually between 20 % and 60 %;
- only step-down linear voltage regulators are possible;
- only noninverting linear voltage regulators are possible;
- large low-frequency (50 or 60 Hz) transformers are required in ac–dc power supplies with linear voltage regulators.

1.8 Topologies of PWM DC–DC Converters

Switched-mode technology employs a wide variety of topologies. Figure 1.17 shows a family of single-ended PWM dc–dc converters: the buck, boost, buck-boost, flyback, forward, Ćuk (boost-buck), SEPIC (single-ended primary input converter), and dual SEPIC [7] (also called zeta or inverse SEPIC) converters. The flyback converter is a transformer version of the buck-boost converter, and the forward converter is a transformer version of the buck converter. The flyback and dual SEPIC converters are identical on the primary side of the transformer. Likewise, the Ćuk and SEPIC converters are identical on the primary side of the transformer. The flyback and SEPIC converters are identical on the secondary side of the

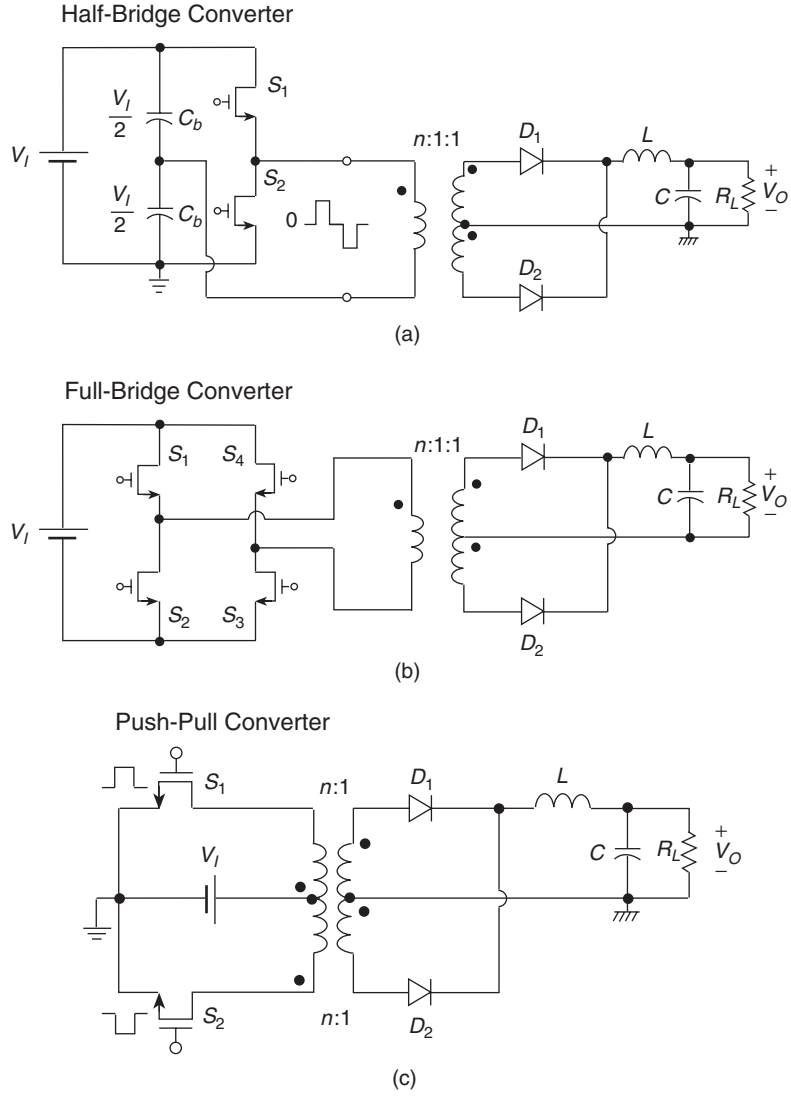


Figure 1.18 Multiple-switch isolated PWM dc–dc converters.

transformer. Likewise, the Ćuk and dual SEPIC converters are identical on the secondary side of the transformer.

Figure 1.18 depicts the multiple-switch PWM dc–dc converters: half-bridge, full-bridge, and push-pull converters. Switched-mode converters use duty-cycle control of a switching element to block the flow of energy from the input to the output and thus achieve voltage regulation. The advantages of these converters include significant reduction of a transformer and energy storage components. Since switched-mode converters can operate at high frequencies, a small transformer with a ferrite core can be used. The reduced size is very important in many applications, such as aerospace, computers, and wireless technologies. However, there is a penalty paid due to the increased noise, which is present at both input and output of the supply due to the switching action of semiconductor devices. In addition, the control circuit is much more complicated than that used in linear regulators.

Power MOSFETs are often used as controllable switches. In 1979, International Rectifier patented the first commercially viable power MOSFET, called the HEXFET. Fast recovery diodes, ultrafast recovery, and hyperfast recovery pn junction diodes, or Schottky diodes, are used in switching dc–dc power converters. In 1976, Silicon General introduced the industry's first PWM controller integrated circuit (IC), the SG1524.

1.9 Relationships among Current, Voltage, Energy, and Power

The average value of current $i(t)$ is given by

$$I_{AV} = \frac{1}{T}\int_0^T i(t)\,dt, \tag{1.54}$$

and the rms value of the current is

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i^2(t)\,dt}. \tag{1.55}$$

Likewise, the average value of voltage $v(t)$ is expressed by

$$V_{AV} = \frac{1}{T}\int_0^T v(t)\,dt, \tag{1.56}$$

and the rms value of the voltage is given by

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}. \tag{1.57}$$

The instantaneous power is

$$p(t) = i(t)v(t). \tag{1.58}$$

The energy dissipated in a component or delivered by a source over a time interval t_1 is

$$W = \int_0^{t_1} p(t)\,dt = \int_0^{t_1} i(t)v(t)\,dt. \tag{1.59}$$

For periodic waveforms in steady state, the average real power absorbed by a component or delivered by a source is the time-average value of the instantaneous power over a period T of the operating frequency,

$$P = \frac{1}{T}\int_0^T p(t)\,dt = \frac{1}{T}\int_0^T i(t)v(t)\,dt = \frac{W}{T} = f\,W. \tag{1.60}$$

For periodic waveforms in steady state, the average charge stored in a capacitor over one period is zero,

$$Q = \int_0^T i_C(t)\,dt = 0. \tag{1.61}$$

This is called the principle of *capacitor charge balance* or *capacitor ampere-second balance*. Thus, the average current through a capacitor for steady-state operation is zero,

$$I_{C(AV)} = \frac{Q}{T} = \frac{1}{T}\int_0^T i_C(t)\,dt = 0. \tag{1.62}$$

For periodic waveforms in steady state, the average magnetic flux linkage of an inductor over one period is zero,

$$\lambda = \int_0^T v_L(t)\,dt = 0. \tag{1.63}$$

This is called the principle of *inductor flux linkage balance* or *inductor volt-second balance*. Hence, the average voltage across an inductor in steady state is zero,

$$V_{L(AV)} = \frac{\lambda}{T} = \frac{1}{T}\int_0^T v_L(t)\,dt = 0. \tag{1.64}$$

The instantaneous energy stored in a capacitor is

$$w_C(t) = \frac{1}{2}Cv_C^2(t), \tag{1.65}$$

and in an inductor is

$$w_L(t) = \frac{1}{2}Li_L^2(t). \tag{1.66}$$

1.10 Electromagnetic Compatibility

Switching action causes current pulses at the input of power supplies. Understanding and optimizing the electromagnetic compatibility in switching-mode power supplies is an important problem. Due to the switching action of transistors and diodes, PWM converters have rectangular current and voltage waveforms with short rise times, short fall times, and high dv/dt and di/dt. Therefore, these waveforms exhibit a wide and strong harmonic spectrum. PWM converters are notorious sources of electromagnetic interference and radio-frequency interference, generally called noise. Suppression of EMI is a major issue in switching-mode power converter design. Strong harmonics may interfere with various signals in electronic hardware (i.e., noise receptors), causing EMI. The IEC 61000-3-2 international standard [14] sets limits on the maximum level of harmonics. Other standards of conducted noise are those of the Federal Communications Commission (USA), CISPR (France), VDE (Germany), and military standards.

Depending on noise transmission, there are two categories of noise:

- conducted noise (450 kHz to 30 MHz);
- radiated noise (30 MHz to 1 GHz).

Conducted noise can be divided into differential-mode noise and common-mode noise. Conducted noise is usually suppressed by adding properly designed filters that reduce the power levels of various frequency components in a specific frequency band. Metallic

shields (e.g., metal cabinets) are normally used to prevent radiated noise. Another approach to solving this problem is through spectral modification of EMI at source, which affects all emission routes simultaneously, both conducted and radiated interference. The idea is to spread the spectrum of the converter waveforms such that the power levels at specific frequencies are reduced below the required levels to conform with EMI standards without any additional filters and shields. One method to accomplish this objective is *random modulation* of the converter switching (clock) frequency. This produces a random jitter around the normal periodic voltage and current waveforms, which results in spread in the spectrum and consequent reduction of the spectral peaks. Another method is converter operation under chaos and chaotic modulation. All switching-mode converters are strongly nonlinear systems, and the occurrence of chaos is quite common in them. The chaotic behavior that naturally occurs in switching-mode dc–dc converters has some inherent problems in practical applications. First, the current ripple and hence the power level of ac components increase under chaotic operation, reducing efficiency. Second, the spectrum under chaotic operation has a higher emission floor, and it spreads into the low-frequency range. This may result in audible acoustic disturbances.

1.11 Summary

- The main function of voltage regulators is the regulation of the dc output voltage against changes in the load current, the input voltage, and the temperature.
- Additional functions of voltage regulators are dc isolation, ripple voltage reduction, and fast transient response to rapid changes in the load current and the input voltage.
- Voltage regulators can be categorized into linear voltage regulators, switching-mode dc–dc converters, and switched-capacitor voltage regulators.
- Linear voltage regulators have low power levels, low noise (EMI), low output ripple voltage, excellent load and line regulation, wide bandwidth and fast transient response to load and line changes, but have low efficiency and are only step-down regulators.
- There are series and shunt linear voltage regulators.
- In linear voltage regulators, transistors are operated as dependent current sources.
- In PWM dc–dc converters, transistors are operated as switches. Therefore, the voltage is low when the current is high and the current is zero when the voltage is high, yielding low conduction loss and high efficiency.
- PWM converters are sources of EMI because of the hard switching action of transistors and diodes.
- Switching voltage regulators have high efficiency, high power density, and high power levels. They can be step-down or step-up converters and can have multiple output voltages, but they have slow response to load and line changes, produce high level of EMI, and have high output ripple voltage.

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1.13 Review Questions

1.1 List the main functions of dc–dc converters.

1.2 Give a classification of power supplies.

1.3 Define line regulation of voltage regulators.

1.4 Define load regulation of voltage regulators.

1.5 Define thermal regulation of voltage regulators.

1.6 Define the dc input resistance of voltage regulators.

1.7 Define the dynamic input resistance of voltage regulators.

1.8 Define the ripple rejection ratio of voltage regulators.

1.9 What is the line transient response of voltage regulators?

1.10 What is the load transient response of voltage regulators?

1.11 How are transistors operated in linear voltage regulators?

1.12 What are the basic topologies of linear voltage regulators?

1.13 Give the expression for the efficiency of the series voltage regulator.

1.14 What is the range of efficiency for linear voltage regulators?

1.15 What is the range of output power for linear voltage regulators?

1.16 Can you build a step-up linear voltage regulator?

1.17 What is the size and weight of a transformer in power supplies with linear voltage regulators?

1.18 What is the noise level in linear voltage regulators?

1.19 What are LDO voltage regulators?

1.20 How are transistors and diodes operated in switching-mode dc–dc power converters?

1.21 How is the dc isolation achieved in switching-mode power supplies?

1.22 Compare the efficiency of linear and PWM switching-mode voltage regulators.

1.14 Problems

1.1 A voltage regulator experiences a 100 mV change in the output voltage, when its input voltage changes by 10 V at $I_O = 0.2$ A and $T_A = 25\ ^\circ$C. The nominal output voltage is $V_{Onom} = 3.3$ V. Determine the line regulation and the percentage line regulation.

1.2 A voltage regulator is rated for an output current $I_O = 0$ to 50 mV. Under no-load conditions, the output voltage is 5 V. Under full-load conditions, the output voltage 4.99 V. Find the load regulation, the percentage load regulation, the dc output resistance, and load/line regulation.

1.3 A series linear voltage regulator is operated under the following conditions: $V_I = 6$ to 15 V, $V_O = 3.3$ V, and $I_O = 0$ to 0.4 A. Find the minimum and maximum efficiency of the voltage regulator at full load.

1.4 A voltage regulator has $R_L = 10\,\Omega$, $V_I = 10$ V, $V_O = 5$ V, and $\eta = 90\,\%$. Find the dc input resistance.

2

Buck PWM DC–DC Converter

2.1 Introduction

This chapter studies the PWM buck switching-mode converter, often referred to as a 'chopper' [1]–[25]. Analysis is given for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Current and voltage waveforms for all components of the converter are derived. The dc voltage function is derived for both the modes. Voltage and current stresses of the components are found. The boundary between CCM and DCM is determined. An expression for the output voltage ripple is derived. The power losses in all the components and the transistor gate-drive power are estimated. The overall efficiency of the converter is determined. Design examples are also given.

2.2 DC Analysis of PWM Buck Converter for CCM

2.2.1 Circuit Description

A PWM buck dc–dc converter circuit is depicted in Figure 2.1(a). It consists of four components: a power MOSFET used as a controllable switch S, a diode D_1, an inductor L, and a filter capacitor C. Resistor R_L represents a dc load. Power MOSFETs are the most commonly used controllable switches in dc–dc converters because of their high speeds. In 1979, International Rectifier patented the first commercially viable power MOSFET, the HEXFET. Other power switches such as bipolar junction transistors, insulated gate bipolar transistors, or MOSFET-controlled thyristors may also be used. The diode D_1 is called a *freewheeling diode*, a *flywheel diode*, or a *catch diode*. The switching network composed of the transistor and the diode 'chops' the dc input voltage V_I and therefore the converter

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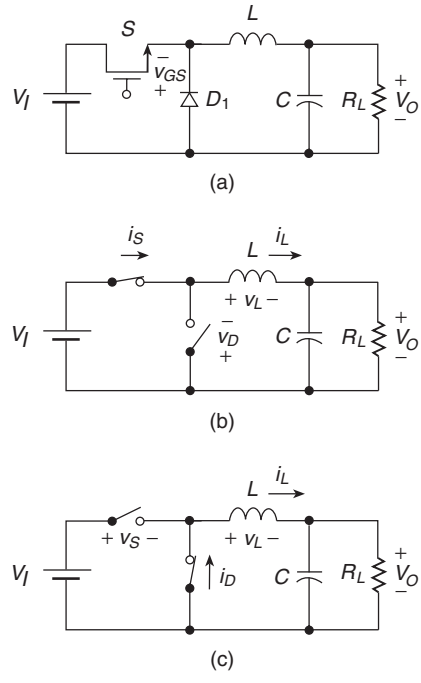


Figure 2.1 PWM buck converter and its ideal equivalent circuits for CCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON.

is often called a 'chopper', which produces a reduced average voltage. The switch S is controlled by a pulse-width modulator and is turned on and off at the switching frequency $f_s = 1/T$ and the duty cycle D defined as

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} = f_s t_{on} \tag{2.1}$$

where t_{on} is the time interval when the switch S is closed and t_{off} is the time interval when the switch S is open. Since the duty cycle D of the drive voltage v_{GS} varies, so does the duty ratio of other waveforms. This permits the regulation of the dc output voltage against changes in the dc input voltage V_I and the load resistance R_L (or the load current I_O). The output voltage V_O of the buck converter is always lower than the input voltage V_I. Therefore, it is a *step-down* converter. The buck converter 'bucks' the voltage to a lower level. Because the gate of the MOSFET is not referenced to ground, it is difficult to drive the transistor. The converter requires a floating gate drive. With the input currrent of the converter being discontinuous, a smoothing LC filter may be required at the input.

The buck converter can operate in a continuous conduction mode or in a discontinuous conduction mode, depending on the waveform of the inductor current. In CCM the inductor current flows during the entire cycle, whereas in DCM the inductor current flows only during part of the cycle. In DCM it falls to zero, remains at zero for some time interval, and then starts to increase. Operation at the CCM/DCM boundary is called the critical mode.

Let us consider operation in the CCM. Figure 2.1(b)–(c) shows the equivalent circuits of the buck converter for CCM when the switch S is ON and the diode D_1 is OFF, and when

the switch is OFF and the diode is ON, respectively. The principle of converter operation is explained by the idealized current and voltage waveforms depicted in Figure 2.2. At time $t = 0$, the switch is turned on by the driver. Consequently, the voltage across the diode is $v_D = -V_I$, causing the diode to be reverse biased. The voltage across the inductor L is $v_L = V_I - V_O$ and therefore the inductor current increases linearly with a slope of $(V_I - V_O)/L$. The inductor current i_L flows through the switch. Hence, $i_S = i_L$. During this time interval, the energy is transferred from the dc input voltage source V_I to the inductor, capacitor, and load. At time $t = DT$, the switch is turned off by the driver.

The inductor has a nonzero current when the switch is turned off. Because the inductor current waveform is a continuous function of time, the inductor current continues to flow in the same direction after the switch turns off. Therefore, the inductor L acts as a current source, which forces the diode to turn on. The voltage across the switch is V_I and the voltage across the inductor is $-V_O$. Hence, the inductor current decreases linearly with a slope of $-V_O/L$. During this time interval, the input source V_I is disconnected from the circuit and does not deliver energy to the load and the LC circuit. The inductor L and capacitor C form an energy reservoir that maintains the load voltage and current when the switch is OFF. At time $t = T$, the switch is turned on again, the inductor current increases and hence energy increases. PWM converters are operated at *hard switching* because the switch voltage waveform is rectangular and the transistor is turned on at a high voltage.

The power switch S and the diode D_1 convert the dc input voltage V_I into a square wave at the input of the L–C–R_L circuit. In other words, the dc input voltage V_I is chopped by the transistor-diode switching network. The L–C–R_L circuit acts as a second-order low-pass filter and converts the square wave into a low-ripple dc output voltage. Since the average voltage across the inductor L is zero for steady state, the average output voltage V_O is equal to the average voltage of the square wave. The width of the square wave is equal to the on-time of the switch S and can be controlled by varying the duty cycle D of the MOSFET gate-to-drive voltage. Thus, the square wave is a PWM voltage waveform. The average value of the PWM voltage waveform is $V_O = DV_I$, which depends on the duty cycle D and is almost independent of the load for CCM operation. Theoretically, the duty cycle D may be varied from 0 to 100 %. This means that the output V_O ranges from 0 to V_I. Thus, the buck circuit is a *step-down* converter. In practice, the dc input voltage V_I varies over a specified range while the output voltage V_O should be held at a fixed value. If the dc voltage V_I is increased, the duty cycle D is reduced so that the product DV_I, being the average value of the PWM voltage, remains constant. On the other hand, if the input voltage, V_I is reduced, the duty cycle D is increased so that the average value of the PWM signal is constant. Therefore, the amount of energy delivered from the input voltage source V_I to the load can be controlled by varying the switch on-duty cycle D. If the output voltage V_O and the load resistance R_L (or the load current I_O) are constant, the output power is also constant. When the input voltage V_I increses, the switch on-time is reduced to transfer the same amount of energy. The practical range of D is usually from 5 % to 95 % due to resolution. The duty cycle D is controlled by a control circuit.

The inductor current contains an ac component which is independent of the dc load current in CCM and a dc component which is equal to the dc load current I_O. As the dc output current I_O flows through the inductor L, only one-half of the B–H curve of the inductor ferrite core is exploited. Therefore, the inductor L should be designed such that the core will not saturate. To avoid core saturation, a core with an air gap and a sufficiently large volume may be required.

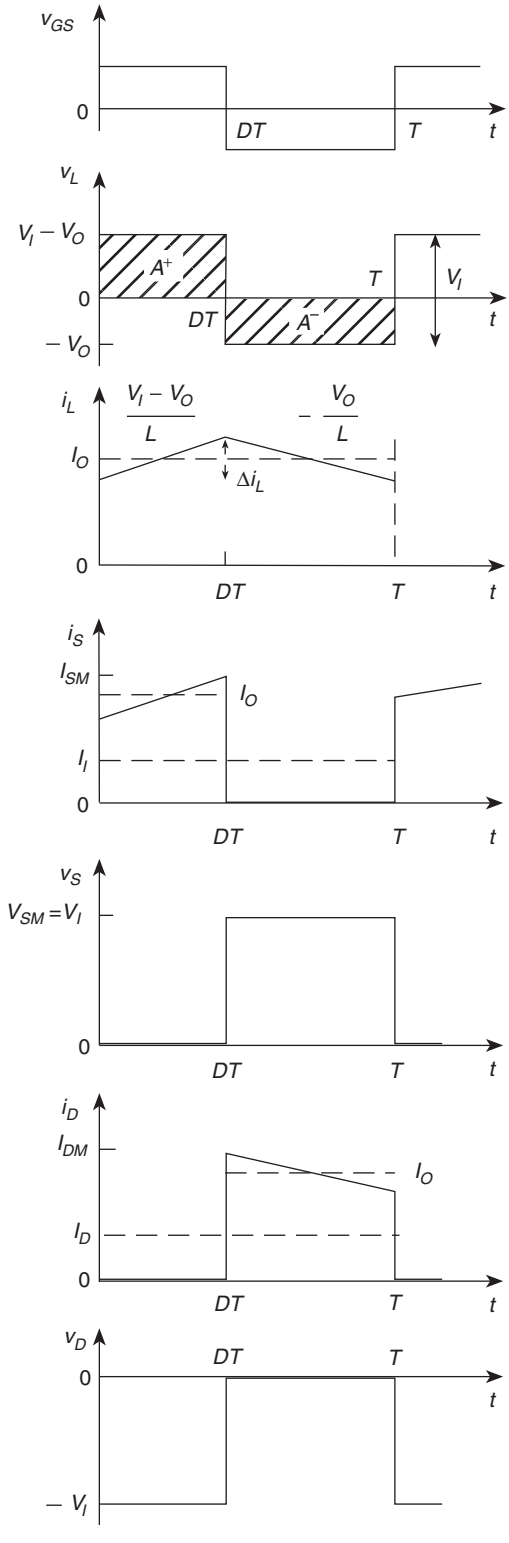


Figure 2.2 Idealized current and voltage waveforms in the PWM buck converter for CCM.

2.2.2 Assumptions

The analysis of the buck PWM converter of Figure 2.1(a) begins with the following assumptions:

1. The power MOSFET and the diode are ideal switches.
2. The transistor output capacitance, the diode capacitance, and the lead inductances are zero, and thus switching losses are neglected.
3. Passive components are linear, time-invariant, and frequency-independent.
4. The output impedance of the input voltage source V_I is zero for both dc and ac components.
5. The converter is operating in steady state.
6. The switching period $T = 1/f_s$ is much shorter than the time constants of reactive components.

2.2.3 Time Interval $0 < t \leq DT$

During the time interval $0 < t \leq DT$, the switch S is ON and the diode D_1 is OFF. An ideal equivalent circuit for this time interval is shown in Figure 2.1(b). When the switch is ON, the voltage across the diode v_D is approximately equal to $-V_I$, causing the diode to be reverse biased. The voltage across the switch v_S and the diode current are zero. The voltage across the inductor L is given by

$$v_L = V_I - V_O = L\frac{di_L}{dt}. \tag{2.2}$$

Hence, the current through the inductor L and the switch S is

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\,dt + i_L(0) = \frac{V_I - V_O}{L}\int_0^t dt + i_L(0) = \frac{V_I - V_O}{L}t + i_L(0), \tag{2.3}$$

where $i_L(0)$ is the initial current in the inductor L at time $t = 0$. The peak inductor current becomes

$$i_L(DT) = \frac{(V_I - V_O)DT}{L} + i_L(0), \tag{2.4}$$

and the peak-to-peak ripple current of the inductor L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{(V_I - V_O)DT}{L} = \frac{(V_I - V_O)D}{f_sL} = \frac{V_ID(1-D)}{f_sL}. \tag{2.5}$$

The diode voltage is

$$v_D = -V_I. \tag{2.6}$$

Thus, the peak value of the diode reverse voltage is

$$V_{DM} = V_I. \tag{2.7}$$

The average value of the inductor current is equal to the dc output current I_O. Hence, one arrives at the peak value of the switch current,

$$I_{SM} = I_O + \frac{\Delta i_L}{2}. \tag{2.8}$$

The increase in the magnetic energy stored in the inductor L during the time interval 0 to DT is given by

$$\Delta W_{L(in)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(0)]. \tag{2.9}$$

The time interval 0 to DT is terminated when the switch is turned off by the driver.

2.2.4 Time Interval $DT < t \leq T$

During the time interval $DT < t \leq T$, the switch S is OFF and the diode D_1 is ON. Figure 2.1(c) shows an ideal equivalent circuit for this time interval. Since $i_L(DT)$ is nonzero at that instant the switch turns off and since the inductor current i_L is a continuous function of time, the inductor acts as a current source and turns the diode on. The switch current i_S and the diode voltage v_D are zero and the voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}. \tag{2.10}$$

The current through the inductor L and the diode can be found as

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = -\frac{V_O}{L}\int_{DT}^{t} dt + i_L(DT) \\ &= -\frac{V_O}{L}(t - DT) + i_L(DT), \end{aligned} \tag{2.11}$$

where $i_L(DT)$ is the initial condition of the inductor L at $t = DT$. The peak-to-peak ripple current of the inductor L is

$$\Delta i_L = i_L(DT) - i_L(T) = \frac{V_O T(1-D)}{L} = \frac{V_O(1-D)}{f_s L}. \tag{2.12}$$

Note that the peak-to-peak value of the inductor current ripple Δi_L is independent of the load current I_O in CCM and depends only on the dc input voltage V_I and thereby on the duty cycle D. For a fixed output voltage V_O, the maximum value of the peak-to-peak inductor ripple current occurs at the maximum input voltage V_{Imax}, which corresponds to the minimum duty cycle D_{min}. It is given by

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L}. \tag{2.13}$$

The switch voltage v_S and the peak switch voltage V_{SM} are given by

$$v_S = V_{SM} = V_I. \tag{2.14}$$

The peak diode and switch currents are given by

$$I_{DM} = I_{SM} = I_O + \frac{\Delta i_L}{2}. \tag{2.15}$$

This time interval ends at $t = T$ when the switch is turned on by the driver.

The decrease in the magnetic energy stored in the inductor L during time interval $DT < t \leq T$ is given by

$$\Delta W_{L(out)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(T)]. \tag{2.16}$$

For steady-state operation, the increase in the magnetic energy $\Delta W_{L(in)}$ is equal to the decrease in the magnetic energy $\Delta W_{L(out)}$.

2.2.5 Device Stresses for CCM

The maximum voltage and current stresses of the switch and the diode in CCM for steady-state operation are

$$V_{SMmax} = V_{DMmax} = V_{Imax} \tag{2.17}$$

and

$$I_{SMmax} = I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = I_{Omax} + \frac{(V_{Imax} - V_O)D_{min}}{2f_sL}$$
$$= I_{Omax} + \frac{V_O(1 - D_{min})}{2f_sL}. \tag{2.18}$$

The transient and steady-state waveforms in converters with commercial components can be obtained from computer simulations using SPICE, described in Appendix A.

2.2.6 DC Voltage Transfer Function for CCM

The voltage and current across a linear inductor are related by Faraday's law in its differential form,

$$v_L = L\frac{di_L}{dt}. \tag{2.19}$$

For steady-state operation, the boundary condition

$$i_L(0) = i_L(T) \tag{2.20}$$

is satisfied. Rearranging (2.19),

$$\frac{1}{L}v_L\,dt = di_L \tag{2.21}$$

and integrating both sides yields

$$\frac{1}{L}\int_0^T v_L\,dt = \int_0^T di_L = i_L(T) - i_L(0) = 0. \tag{2.22}$$

The integral form of Faraday's law for an inductor under steady-state conditions is

$$\int_0^T v_L\,dt = 0. \tag{2.23}$$

The average value of the voltage across an inductor for steady state is zero. Thus,

$$V_{L(AV)} = \frac{1}{T}\int_0^T v_L\,dt = 0. \tag{2.24}$$

This equation is also called a *volt-second balance* for an inductor, which means that 'volt-second' stored is equal to 'volt-second' released.

For PWM converters operating in CCM,

$$\int_0^{DT} v_L\,dt + \int_{DT}^T v_L\,dt = 0, \tag{2.25}$$

from which

$$\int_0^{DT} v_L\,dt = -\int_{DT}^T v_L\,dt. \tag{2.26}$$

This means that the area enclosed by the positive part of the inductor voltage waveform A^+ equals the area enclosed by the negative part of the inductor voltage waveform A^-, that is,

$$A^+ = A^-, \tag{2.27}$$

where

$$A^+ = \int_0^{DT} v_L \, dt \tag{2.28}$$

and

$$A^- = -\int_{DT}^{T} v_L \, dt. \tag{2.29}$$

Referring to Figure 2.2,

$$(V_I - V_O)DT = V_O(1 - D)T, \tag{2.30}$$

which simplifies to the form

$$V_O = DV_I. \tag{2.31}$$

For a lossless converter, $V_I I_I = V_O I_O$. Hence, from (2.31), the dc voltage transfer function (or the voltage conversion ratio) of the lossless buck converter is given by

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = D. \tag{2.32}$$

The range of $M_{V\,DC}$ is

$$0 \le M_{V\,DC} \le 1. \tag{2.33}$$

Note that the output voltage V_O is independent of the load resistance R_L. It depends only on the dc input voltage V_I and the duty cycle D. The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = V_I. \tag{2.34}$$

In most practical situations, $V_O = DV_I$ is constant, which means that if V_I is increased, D should be decreased by a control circuit to keep V_O constant, and vice versa.

The dc current transfer function is given by

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{1}{D} \tag{2.35}$$

and its value decreases from ∞ to 1 as D is increased from 0 to 1.

From (2.8), (2.14), and (2.32), the switch and the diode utilization in the buck converter is characterized by the output-power capability

$$c_p \equiv \frac{P_O}{V_{SM} I_{SM}} = \frac{V_O I_O}{V_{SM} I_{SM}} \approx \frac{V_O}{V_{SM}} = \frac{V_O}{V_I} = D. \tag{2.36}$$

As D increases from 0 to 1, so does c_p.

2.2.7 Boundary between CCM and DCM

Figure 2.3 depicts the inductor current waveform at the boundary between the continuous conduction mode and the discontinuous conduction mode. This waveform can be described by

$$i_L = \frac{V_I - V_O}{L} t, \quad \text{for } 0 < t \le DT, \tag{2.37}$$

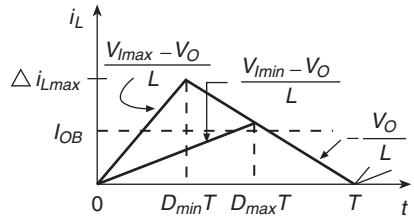


Figure 2.3 Waveforms of the inductor current at the CCM/DCM boundary at V_{Imin} and V_{Imax}.

resulting in the peak inductor current

$$\Delta i_L = i_L(DT) = \frac{(V_I - V_O)DT}{L} = \frac{V_O(1-D)}{f_s L}. \tag{2.38}$$

Hence, one obtains a dc load current at the boundary

$$I_{OB} = \frac{\Delta i_L}{2} = \frac{V_O(1-D)}{2f_s L}, \tag{2.39}$$

and the load resistance at the boundary

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{1-D}. \tag{2.40}$$

Figures 2.4 and 2.5 show the normalized load current $I_{OB}/(V_O/2f_sL) = 1 - D$ and the load resistance $R_{LB}/(2f_sL) = 1/(1-D)$ at the CCM/DCM boundary as functions of the duty cycle D, respectively. The plots can be obtained using MATLAB, described in Appendix B.

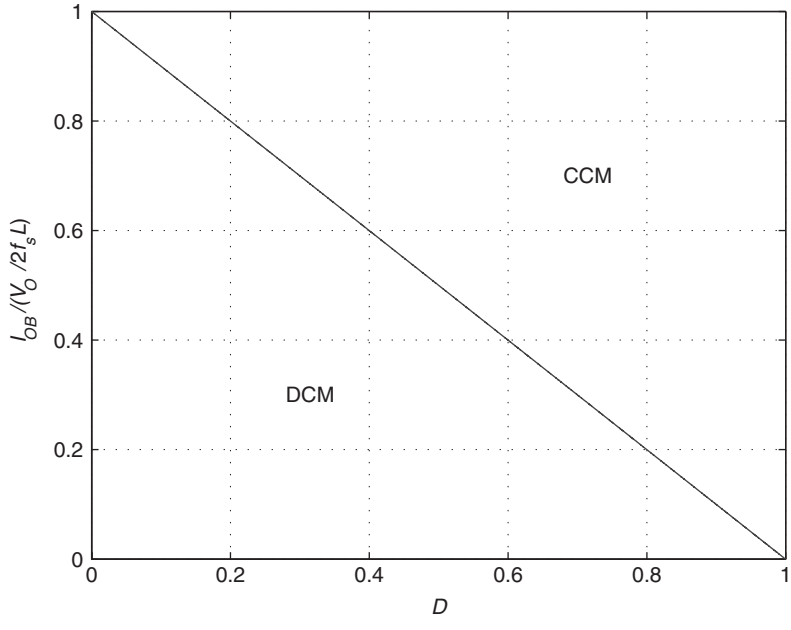


Figure 2.4 Normalized load current $I_{OB}/(V_O/2f_sL)$ at the CCM/DCM boundary as a function of the duty cycle D for buck converter.

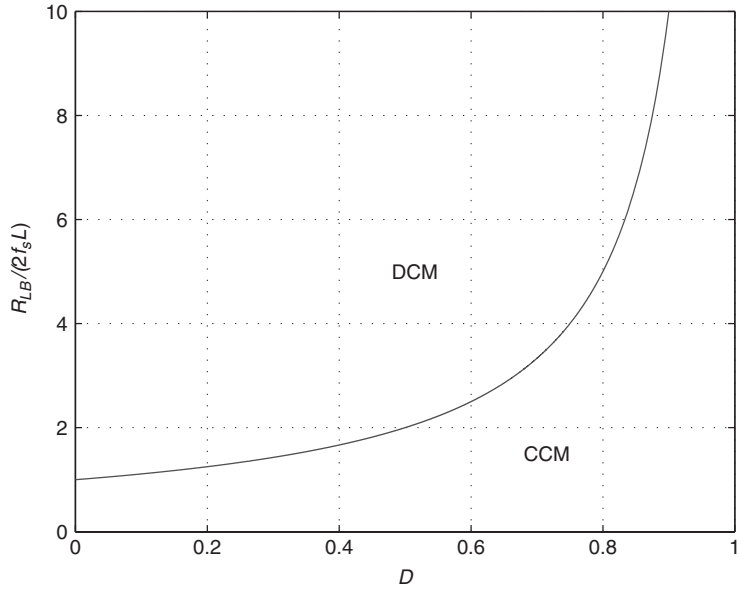


Figure 2.5 Normalized load resistance $R_{LB}/(2f_sL)$ at the CCM/DCM boundary as a function of the duty cycle D for buck converter.

For the worst case,

$$I_{Omin} = I_{OBmax} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O(1 - D_{min})}{2f_sL_{min}}. \tag{2.41}$$

Hence, the minimum inductance required to maintain the CCM operation for the duty cycle ranging from D_{min} to D_{max} is

$$L_{min} = \frac{V_O(1 - D_{min})}{2f_sI_{Omin}} = \frac{R_{Lmax}(1 - D_{min})}{2f_s} = \frac{D_{min}(V_{Imax} - V_O)}{2f_sI_{Omin}}. \tag{2.42}$$

As the switching frequency f_s increases, the minimum inductance L_{min} decreases. Therefore, high switching frequencies are desirable to reduce the size of the inductor. In some applications, the inductance L can be much higher than L_{min} in order to reduce the ripple current through the inductor and the filter capacitor. Therefore, it is easier to reduce the output voltage ripple, to avoid the core saturation, and to reduce the winding and core losses.

If the dc output current I_O and the dc input voltage V_I are fixed, the peak-to-peak inductor current $\Delta i_L = 2I_O$ can be made very large while maintaining the converter operation in CCM. In this case, the ripple current of the inductor should be limited (e.g., $\Delta i_L/(2I_O) \leq 10\,\%$).

2.2.8 Ripple Voltage in Buck Converter for CCM

The input voltage of the second-order low-pass *LCR* output filter is rectangular with a maximum value V_I and a duty cycle D. This voltage can be expanded into a Fourier series

$$v = DV_I\left[1 + 2\sum_{n=1}^{\infty}\frac{\sin(n\pi D)}{n\pi D}\cos\, n\omega_s t\right]$$

$$= DV_I + 2DV_I \left[\frac{\sin \pi D}{\pi D} \cos \omega_s t + \frac{\sin 2\pi D}{2\pi D} \cos 2\omega_s t + \frac{\sin 3\pi D}{3\pi D} \cos 3\omega_s t + \ldots \right]. \tag{2.43}$$

The components of this series are transmitted through the output filter to the load. It is difficult to determine the peak-to-peak output voltage ripple V_r using the Fourier series of the output voltage. Therefore, a different approach will be taken to derive an expression for V_r.

The output part of the buck converter is shown in Figure 2.6. The filter capacitor in this figure is modeled by its capacitance C and its equivalent series resistance (ESR) designated by r_C. Figure 2.7 depicts current and voltage waveforms in the converter output circuit. The dc component of the inductor current flows through the load resistor R_L, while the ac component is divided between the capacitor C and the load resistor R_L. In practice, the filter capacitor is designed so that the impedance of the capacitive branch is much less than the load resistance R_L. Consequently, the load ripple current is very small and can be neglected. Thus, the current through the capacitor is approximately equal to the ac component of the inductor current, $i_C \approx i_L - I_O$.

For the interval $0 < t \leq DT$, when the switch is ON and the diode is OFF, the capacitor current is given by

$$i_C = \frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2}, \tag{2.44}$$

resulting in the ac component of the voltage across the ESR,

$$v_{rc} = r_C i_C = r_C \Delta i_L \left(\frac{t}{DT} - \frac{1}{2} \right). \tag{2.45}$$

The voltage across the filter capacitance v_C consists of the dc voltage V_C and the ac voltage v_c, $v_C = V_C + v_c$. Only the ac component v_c may contribute to the output ripple voltage. The ac component of the voltage across the filter capacitance is given by

$$v_c = \frac{1}{C} \int_0^t i_C \, dt + v_c(0) = \frac{\Delta i_L}{C} \int_0^t \left(\frac{t}{DT} - \frac{1}{2} \right) dt + v_c(0) = \frac{\Delta i_L}{2C} \left(\frac{t^2}{DT} - t \right) + v_c(0). \tag{2.46}$$

In steady state, $v_c(DT) = v_c(0)$. The waveform of the voltage across capacitance C is a parabolic function. The ac component of the output voltage is the sum of voltage across the filter capacitor ESR r_C and the filter capacitance C,

$$v_o = v_{rc} + v_c = \Delta i_L \left[\frac{t^2}{2C\,DT} + \left(\frac{r_C}{DT} - \frac{1}{2C} \right) t - \frac{r_C}{2} \right] + v_c(0). \tag{2.47}$$

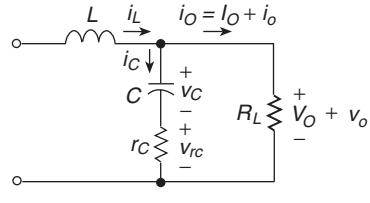


Figure 2.6 Output circuit of the buck converter.

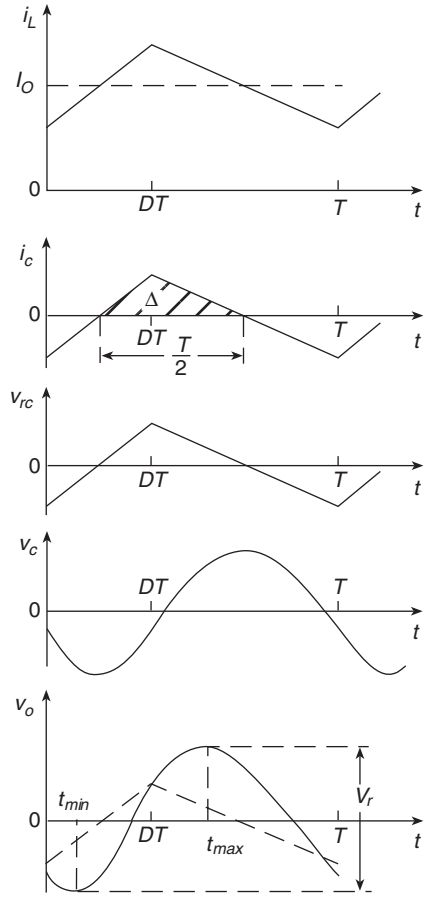


Figure 2.7 Waveforms illustrating the ripple voltage in the PWM buck converter.

Let us consider the minimum value of the voltage v_o. The derivative of the voltage v_o with respect to time is

$$\frac{dv_o}{dt} = \Delta i_L \left(\frac{t}{C\,DT} + \frac{r_C}{DT} - \frac{1}{2C} \right). \tag{2.48}$$

Setting this derivative to zero, the time at which the minimum value of v_o occurs is given by

$$t_{min} = \frac{DT}{2} - r_C C. \tag{2.49}$$

The minimum value of v_o is equal to the minimum value of v_{rc} if $t_{min} = 0$. This occurs at a minimum capacitance given by

$$C_{min(on)} = \frac{D_{max}}{2 f_s r_{Cmax}}. \tag{2.50}$$

Consider the time interval $DT < t \leq T$ when the switch S is OFF and the diode D_1 is ON. Referring to Figure 2.7, the current through the capacitor is

$$i_C = -\frac{\Delta i_L (t - DT)}{(1 - D)T} + \frac{\Delta i_L}{2}, \tag{2.51}$$

resulting in the voltage across the ESR,

$$v_{rc} = r_C i_C = r_C \Delta i_L \left[-\frac{t - DT}{(1-D)T} + \frac{1}{2} \right], \tag{2.52}$$

and the voltage across the capacitor,

$$\begin{aligned} v_c &= \frac{1}{C} \int_{DT}^{t} i_C \, dt + v_c(DT) = \frac{\Delta i_L}{C} \int_{DT}^{t} \left[-\frac{t - DT}{(1-D)T} + \frac{1}{2} \right] dt + v_c(DT) \\ &= \frac{\Delta i_L}{2C} \left[-\frac{t^2 - 2DTt + (DT)^2}{(1-D)T} + t - DT \right] + v_c(0). \end{aligned} \tag{2.53}$$

Adding (2.52) and (2.53) yields the ac component of the output voltage,

$$v_o = r_c \Delta i_L \left[-\frac{t - DT}{(1-D)T} + \frac{1}{2} \right] + \frac{\Delta i_L}{2C} \left[-\frac{t^2 - 2DTt + (DT)^2}{T(1-D)} + t - DT \right] + v_c(0). \tag{2.54}$$

The derivative of v_o with respect to time is

$$\frac{dv_o}{dt} = -\frac{r_C \Delta i_L}{(1-D)T} + \frac{\Delta i_L}{C} \left[-\frac{t - DT}{(1-D)T} + \frac{1}{2} \right]. \tag{2.55}$$

Setting the derivative to zero, the time at which the maximum value of v_o occurs is expressed by

$$t_{max} = \frac{(1+D)T}{2} - r_C C. \tag{2.56}$$

The maximum value of v_o is equal to the maximum value of v_{rc} if $t_{max} = DT$. This occurs at a minimum capacitance given by

$$C_{min(off)} = \frac{1 - D_{min}}{2 f_s r_{Cmax}}. \tag{2.57}$$

The peak-to-peak ripple voltage is independent of the voltage across the filter capacitance C and is determined only by the ripple voltage across the ESR if

$$C \geq C_{min} = \max\{C_{min(on)}, C_{min(off)}\} = \frac{\max\{D_{max}, 1 - D_{min}\}}{2 f_s r_C}. \tag{2.58}$$

For the worst case, $D_{min} = 0$ or $D_{max} = 1$. Thus, the above condition is satisfied at any value of D if

$$C \geq C_{min} = \frac{1}{2 r_C f_s}. \tag{2.59}$$

If condition (2.58) is satisfied, the peak-to-peak ripple voltage of the buck converter is

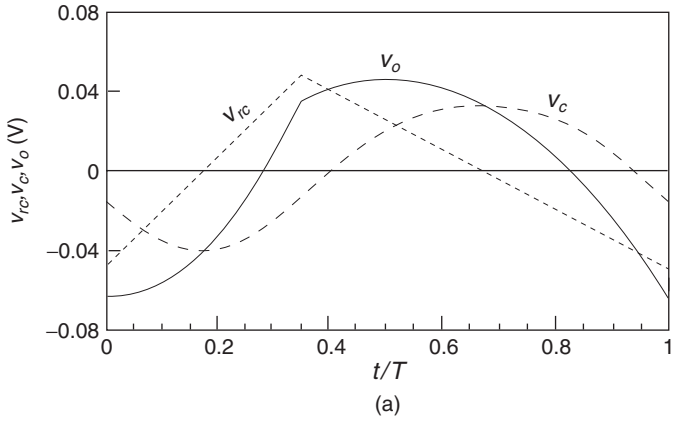
$$V_r = r_C \Delta i_{Lmax} = \frac{r_C V_O (1 - D_{min})}{f_s L}. \tag{2.60}$$

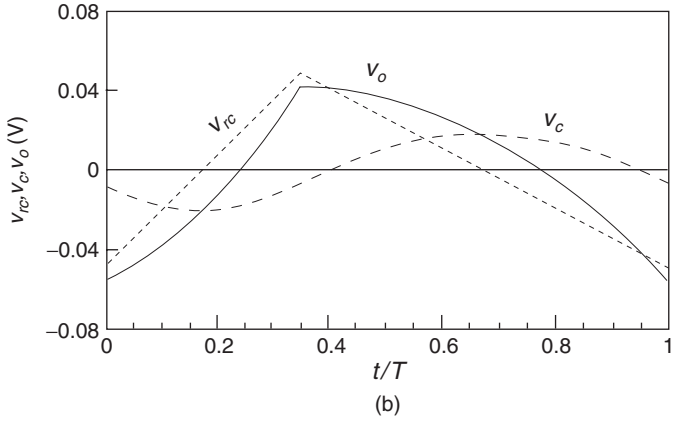
For steady-state operation, the average value of the ac component of the capacitor voltage v_c is zero, that is,

$$\frac{1}{T} \int_0^T v_c \, dt = 0, \tag{2.61}$$

resulting in

$$v_c(0) = \frac{\Delta i_L (2D - 1)}{12 f_s C}. \tag{2.62}$$





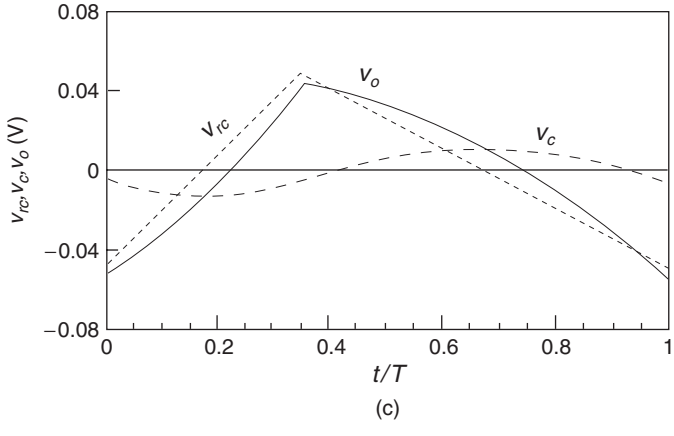


Figure 2.8 Waveforms of v_c, v_{rc}, and v_o at three values of the filter capacitor for CCM. (a) $C < C_{min}$. (b) $C = C_{min}$. (c) $C > C_{min}$.

Waveforms of v_{rc}, v_c, and v_o are depicted in Figure 2.8 for three values of the filter capacitance C. In Figure 2.8(a), the peak-to-peak value of v_o is higher than the peak-to-peak value of v_{rc} because $C < C_{min}$. Figure 2.8(b)–(c) shows the waveforms for $C = C_{min}$ and $C > C_{min}$, respectively. For both these cases, the peak-to-peak voltages of v_o and v_{rc} are the same. For aluminum electrolytic capacitors, $Cr_C \approx 65 \times 10^{-6}$ s.

If condition (2.58) is not satisfied, both the voltage drop across the filter capacitor C and the voltage drop across the ESR contribute to the ripple output voltage. The maximum increase of the charge stored in the filter capacitor in every cycle T is

$$\Delta Q = \frac{\frac{T}{2}\frac{\Delta i_{Lmax}}{2}}{2} = \frac{T\,\Delta i_{Lmax}}{8} = \frac{\Delta i_{Lmax}}{8f_s}. \tag{2.63}$$

Hence, using (2.38), the voltage ripple across the capacitance C is

$$V_{Cpp} = \frac{\Delta Q}{C} = \frac{\Delta i_{Lmax}}{8f_s C} = \frac{V_O(1 - D_{min})}{8f_s^2 LC} = \frac{(1 - D_{min})\pi^2 V_O f_o^2}{2f_s^2}, \tag{2.64}$$

where $f_o = 1/(2\pi\sqrt{LC})$ is the corner frequency of the output filter. The minimum filter capacitance required to reduce its peak-to-peak ripple voltage below a specified level V_{Cpp} is

$$C_{min} = \frac{\Delta i_{Lmax}}{8f_s V_{Cpp}} = \frac{(1 - D_{min})V_O}{8f_s^2 L V_{Cpp}}. \tag{2.65}$$

Thus, C_{min} is inversely proportional to f_s^2. Therefore, high switching frequencies are desirable to reduce the size of the filter capacitor.

Using (2.38), the peak-to-peak voltage ripple across the ESR is

$$V_{rcpp} = r_C\,\Delta i_{Lmax} = \frac{r_C V_O(1 - D_{min})}{f_s L}. \tag{2.66}$$

Hence, the conservative estimation of the total voltage ripple is

$$V_r \approx V_{Cpp} + V_{rcpp} = \frac{V_O(1 - D_{min})}{8f_s^2 LC} + \frac{r_C V_O(1 - D_{min})}{f_s L}. \tag{2.67}$$

2.2.9 Switching Losses with Linear MOSFET Output Capacitance

Let us assume that the MOSFET output capacitance C_o is linear. First, we shall consider the transistor *turn-off transition*. During this time interval, the transistor is OFF, the drain-to-source voltage v_{DS} increases from nearly zero to V_I, and the transistor output capacitance is charged. Because $dQ = C_o dv_{DS}$, the charge transferred from the input voltage source V_I to the transistor output capacitance C_o during the turn-off transition is

$$Q = \int_0^T i_I\,dt = \int_0^{V_I} dQ = C_o \int_0^{V_I} dv_{DS}, = C_o V_I, \tag{2.68}$$

yielding the energy transferred from the input voltage source V_I to the converter during the turn-off transition,

$$W_{V_I} = \int_0^T p(t)\,dt = \int_0^T v_I i_I\,dt = V_I \int_0^T i_I\,dt = V_I Q = C_o V_I^2. \tag{2.69}$$

An alternative method for deriving an expression for the energy delivered from a dc source V_I to a series $R-C_o$ circuit after turning on V_I is as follows. The input current is

$$i_I = \frac{V_I}{R} e^{-\frac{t}{\tau}}, \tag{2.70}$$

where $\tau = RC_o$ is the time constant. Hence,

$$W_{V_I} = \int_0^\infty v_I i_I \, dt = V_I \int_0^\infty i_I \, dt = \frac{V_I^2}{R} \int_0^\infty e^{-\frac{t}{\tau}} \, dt = \frac{V_I^2 \tau}{R} = C_o V_I^2. \tag{2.71}$$

Using $dW_s = Q dv_{DS}/2$, the energy stored in the transistor output capacitance C_o at the end of the transistor turn-off transition when $v_{DS} = V_I$ is given by

$$W_s = \int_0^{V_I} dW_s = \frac{1}{2} Q \int_0^{V_I} dv_{DS} = \frac{1}{2} Q V_I = \frac{1}{2} C_o V_I^2. \tag{2.72}$$

Thus, the energy lost in the parasitic resistance of the capacitor charging path is the turn-off switching energy loss described by

$$W_{turn\text{-}off} = W_{V_I} - W_s = C_o V_I^2 - \tfrac{1}{2} C_o V_I^2 = \tfrac{1}{2} C_o V_I^2, \tag{2.73}$$

which results in the *turn-off switching power loss* in the resistance of the charging path

$$P_{turn\text{-}off} = \frac{W_{turn\text{-}off}}{T} = f_s W_{turn\text{-}off} = \frac{1}{2} f_s C_o V_I^2. \tag{2.74}$$

After turn-off, the transistor remains in the off-state for some time interval and the charge W_s is stored in the output capacitance C_o. The efficiency of charging a linear capacitance from a dc voltage source is 50 %.

Now consider the transistor *turn-on transition*. When the transistor is turned on, its output capacitance C_o is shorted out through the transistor on-resistance r_{DS}, the charge stored in C_o decreases, and the drain-to-source voltage decreases from V_I to nearly zero. As a result, all the energy stored in the transistor output capacitance is dissipated as heat in the transistor on-resistance r_{DS}. Therefore, the turn-on switching energy loss is

$$W_{turn\text{-}on} = W_s = \tfrac{1}{2} C_o V_I^2 \tag{2.75}$$

resulting in the turn-on switching power loss in the MOSFET,

$$P_{turn\text{-}on} = P_{sw(FET)} = \frac{W_{turn\text{-}on}}{T} = f_s W_{turn\text{-}on} = \frac{1}{2} f_s C_o V_I^2. \tag{2.76}$$

The turn-on loss is independent of the transistor on-resistance r_{DS} as long as the transistor output capacitance is fully discharged before the turn-off transition begins.

The total switching energy loss in every cycle of the switching frequency during the process of first charging and then discharging the output capacitance is given by

$$W_{sw} = W_{turn\text{-}off} + W_{turn\text{-}on} = W_{V_I} = C_o V_I^2, \tag{2.77}$$

and the total switching loss in the converter is

$$P_{sw} = \frac{W_{sw}}{T} = f_s W_{sw} = f_s C_o V_I^2. \tag{2.78}$$

For a linear capacitance, one-half of the switching power is lost in the MOSFET and the other half in the resistance of the charging path of the transistor output capacitance, that is, $P_{turn\text{-}on} = P_{turn\text{-}off} = P_{sw}/2$.

The behavior of a diode is different from that of a transistor because a diode cannot discharge its parallel capacitance through its forward resistance. This is because a diode does not turn on until its voltage drops to the threshold voltage. However, the junction diodes suffer from the reverse recovery at turn-off.

2.2.10 Switching Losses with Nonlinear MOSFET Output Capacitance

The MOSFET drain-to-source capacitance C_{ds} is a nonlinear capacitance of the pn step-junction body diode, which depends on the drain-to-source voltage v_{DS},

$$C_{ds} = \frac{C_{J0}}{\sqrt{1 + \dfrac{v_{DS}}{V_B}}} = C_{J0}\sqrt{\frac{V_B}{v_{DS} + V_B}}, \quad \text{for } v_{DS} \geq -V_B, \tag{2.79}$$

where C_{J0} is the zero-bias junction capacitance and V_B is the built-in potential barrier, which ranges from 0.55 V to 0.9 V. From (2.79),

$$C_{ds}(v_{DS}) = C_{ds}(V_I)\sqrt{\frac{V_I + V_B}{v_{DS} + V_B}} \approx C_{ds}(V_I)\sqrt{\frac{V_I}{v_{DS}}}. \tag{2.80}$$

Manufacturers of power MOSFETs usually specify the capacitances $C_{rss} = C_{gd}$, $C_{iss} = C_{gs} + C_{gd}$, and $C_{oss} = C_{ds} + C_{gd}$ at $f = 1$ MHz. The capacitances C_{rss} and C_{oss} are measured at $V_{DS} = 25$ V and $V_{GS} = 0$ V. Hence, $C_{ds25} = C_{oss} - C_{rss}$. The output capacitance at $v_{DS} = V_I$ is

$$C_{ds}(V_I) = \frac{C_{J0}}{\sqrt{1 + \dfrac{V_I}{V_B}}} = C_{ds25}\sqrt{\frac{25 + V_B}{V_I + V_B}} \approx \frac{5C_{ds25}}{\sqrt{V_I}}. \tag{2.81}$$

Since $dQ = C_{ds}dv_{DS}$, the charge transferred from the dc input voltage source V_I to the drain-to-source junction capacitance C_{ds} during the *turn-off transition* is given by

$$\begin{aligned} Q(v_{DS}) &= \int_{-V_B}^{v_{DS}} C_{ds}(v_{DS})\, dv_{DS} = C_{J0}\int_{-V_B}^{v_{DS}} \sqrt{\frac{V_B}{v_{DS} + V_B}}\, dv_{DS} \\ &= 2C_{J0}\sqrt{V_B(v_{DS} + V_B)} = 2(v_{DS} + V_B)C_{ds}(v_{DS}) \approx 2C_{ds}(v_{DS})v_{DS}. \end{aligned} \tag{2.82}$$

Hence,

$$Q(V_I) = 2(V_I + V_B)C_{ds}(V_I) \approx 2C_{ds}(V_I)V_I. \tag{2.83}$$

The energy transferred from the input dc voltage source V_I to the converter during the turn-off transition is given by

$$\begin{aligned} W_{V_I} &= \int_{-V_B}^{V_I} v_I i_I\, dt = V_I \int_{-V_B}^{V_I} i_I\, dt = V_I Q(V_I) \\ &= 2V_I(V_I + V_B)C_{ds}(V_I) \approx 2C_{ds}(V_I)V_I^2. \end{aligned} \tag{2.84}$$

Because $dW_s = Qdv_{DS}/2$, the energy stored in the drain-to-source capacitance C_{ds} at v_{DS} is

$$\begin{aligned} W_s(v_{DS}) &= \int_{-V_B}^{v_{DS}} dE_s = \frac{1}{2}\int_{-V_B}^{v_{DS}} Q dv_{DS} = C_{J0}\sqrt{V_B}\int_{-V_B}^{v_{DS}} \sqrt{v_{DS} + V_B}\, dv_{DS} \\ &= \frac{2}{3}(v_{DS} + V_B)^2 C_{ds}(v_{DS}) \approx \frac{2}{3}C_{ds}(v_{DS})v_{DS}^2. \end{aligned} \tag{2.85}$$

Hence, one obtains the energy stored in C_{ds} at V_I,

$$W_s = \tfrac{2}{3}(V_I + V_B)^2 C_{ds}(V_I) \approx \tfrac{2}{3}C_{ds}(V_I)V_I^2. \tag{2.86}$$

Therefore, the energy lost in the resistance of the charging path of the MOSFET output capacitance is

$$W_{turn\text{-}off} = W_{V_I} - W_s \approx 2C_{ds}(V_I)V_I^2 - \tfrac{2}{3}C_{ds}(V_I)V_I^2 = \tfrac{4}{3}C_{ds}(V_I)V_I^2. \tag{2.87}$$

Hence, the switching power loss dissipated in the resistance r of the path of charging the transistor output capacitance is

$$\begin{aligned} P_r = P_{turn\text{-}off} &= \frac{W_{turn\text{-}off}}{T} = f_s W_{turn\text{-}off} = \frac{4}{3} f_s C_{ds}(V_I)V_I^2 \\ &= \frac{20}{3} f_s C_{ds25}\sqrt{V_I^3}. \end{aligned} \tag{2.88}$$

The transistor equivalent linear output capacitance that causes the same switching power loss in the charging path resistance r during the turn-off transition as the linear one is derived as

$$\frac{1}{2} f_s C_{eq(r)} V_I^2 = \frac{4}{3} f_s C_{ds}(V_I)V_I^2 = \frac{20}{3} f_s C_{ds25}\sqrt{V_I^3}, \tag{2.89}$$

producing

$$C_{eq(r)} = \frac{8}{3}C_{ds}(V_I) = \frac{40C_{ds25}}{3\sqrt{V_I}}. \tag{2.90}$$

During the *turn-on transition*, all the energy stored in the transistor output capacitance is lost in the MOSFET on-resistance r_{DS}:

$$W_{turn\text{-}on} = W_s = \tfrac{2}{3}C_{ds}(V_I)(V_I + V_B)^2 \approx \tfrac{2}{3}C_{ds}(V_I)V_I^2. \tag{2.91}$$

Thus, the MOSFET turn-on switching loss is

$$\begin{aligned} P_{sw(FET)} = P_{turn\text{-}on} &= \frac{W_{turn\text{-}on}}{T} = f_s W_{turn\text{-}on} = \frac{2}{3} f_s C_{ds}(V_I)V_I^2 \\ &= \frac{10}{3} f_s C_{ds25}\sqrt{V_I^3}. \end{aligned} \tag{2.92}$$

The transistor equivalent linear output capacitance that causes the same switching power loss in the MOSFET on-resistance during the turn-on transition as the linear one can be obtained as

$$\frac{1}{2} f_s C_{eq(FET)} V_I^2 = \frac{2}{3} f_s C_{ds}(V_I)V_I^2 = \frac{10}{3} f_s C_{ds25}\sqrt{V_I^3}, \tag{2.93}$$

resulting in

$$C_{eq(FET)} = \frac{4}{3}C_{ds}(V_I) = \frac{20C_{ds}(V_I)}{3\sqrt{V_I}}. \tag{2.94}$$

The total switching energy loss in each cycle of the switching frequency is

$$W_{sw} = W_{turn\text{-}off} + W_{turn\text{-}on} = W_{V_I} = 2C_{ds}(V_I)V_I^2, \tag{2.95}$$

and the total switching loss in the converter is

$$P_{sw} = \frac{W_{sw}}{T} = f_s W_{sw} = 2f_s C_{ds}(V_I)V_I^2 = 10 f_s C_{ds25}\sqrt{V_I^3}. \tag{2.96}$$

The transistor equivalent linear output capacitance $C_{eq(sw)}$ that produces the same amount of the switching loss as the nonlinear one at a given V_I can be derived as

$$f_s C_{eq(sw)} V_I^2 = 2f_s C_{ds}(V_I)V_I^2 = 10 f_s C_{ds25}\sqrt{V_I^3}, \tag{2.97}$$

yielding

$$C_{eq(sw)} = 2C_{ds}(V_I) = \frac{10C_{ds25}}{\sqrt{V_I}}. \tag{2.98}$$

The turn-off switching power loss is twice as high as the turn-on switching power loss for the MOSFET with a nonlinear output capacitance:

$$\frac{P_{turn\text{-}off}}{P_{turn\text{-}on}} = 2. \tag{2.99}$$

Example 2.1

An IRF510 power MOSFET with $V_B = 0.774158\,\text{V}$, $C_{rss} = 25\,\text{pF}$, and $C_{oss} = 100\,\text{pF}$ is operated in the buck PWM converter at $V_I = 100\,\text{V}$ and $f_s = 100\,\text{kHz}$. Find C_{ds25}, C_{J0}, $C_{ds}(V_I)$, $Q(V_I)$, W_{sw}, P_{sw}, $C_{eq(sw)}$, $W_{turn\text{-}on}$, $P_{sw(FET)}$, $C_{eq(FET)}$, $W_{turn\text{-}off}$, $P_{turn\text{-}off}$, and $C_{eq(r)}$.

Solution. The transistor drain-to-source capacitance at $V_{DS} = 25\,\text{V}$ is

$$C_{ds25} = C_{oss} - C_{rss} = 100 - 25 = 75\,\text{pF}. \tag{2.100}$$

The zero-bias drain-to-source capacitance is

$$C_{J0} = C_{ds25}\sqrt{1 + \frac{25}{V_B}} = 75 \times \sqrt{1 + \frac{25}{0.774158}} = 432.75\,\text{pF}. \tag{2.101}$$

The drain-to-source capacitance at $V_I = 100\,\text{V}$ is

$$C_{ds}(V_I) = \frac{C_{J0}}{\sqrt{1 + \dfrac{V_I}{V_B}}} = \frac{432.75}{\sqrt{1 + \dfrac{100}{0.774158}}} = 37.93\,\text{pF}. \tag{2.102}$$

The charge transferred from the dc input source to C_{ds} during the turn-off transition is

$$Q(V_I) = 2(V_I + V_B)C_{ds}(V_I) = 2 \times (100 + 0.774158) \times 37.93 \times 10^{-12} = 7.6447\,\text{nC}. \tag{2.103}$$

The switching energy is

$$W_{sw} = W_{V_I} = 2V_I^2 C_{ds}(V_I) = 2 \times 100^2 \times 37.93 \times 10^{-12} = 758.6\,\text{nJ}. \tag{2.104}$$

The switching loss is

$$P_{sw} = 2f_s V_I^2 C_{ds}(V_I) = 2 \times 100 \times 10^3 \times 100^2 \times 37.93 \times 10^{-12} = 75.86\,\text{mW}. \tag{2.105}$$

The equivalent linear switching capacitance is

$$C_{eq(sw)} = 2C_{ds}(V_I) = 2 \times 37.93 \times 10^{-12} = 75.86\,\text{pF}. \tag{2.106}$$

The energy lost during the turn-on transition is equal to the energy stored in C_{ds} at the end of the turn-off transition when $v_{DS} = V_I$. This energy is

$$W_{turn\text{-}on} = W_s = \tfrac{2}{3}V_I^2 C_{ds}(V_I) = \tfrac{2}{3} \times 100^2 \times 37.93 \times 10^{-12} = 252.87\,\text{nJ}. \tag{2.107}$$

The switching power loss in the MOSFET is

$$P_{sw(FET)} = \tfrac{2}{3} f_s V_I^2 C_{ds}(V_I) = \tfrac{2}{3} \times 100 \times 10^3 \times 100^2 \times 37.93 \times 10^{-12} = 25.287\,\text{mW}. \tag{2.108}$$

The equivalent linear turn-on capacitance is

$$C_{eq(FET)} = \tfrac{4}{3}C_{ds}(V_I) = \tfrac{4}{3} \times 37.93 \times 10^{-12} = 50.57\,\text{pF}. \tag{2.109}$$

The energy lost in the resistance of the charging path of C_{ds} during the turn-off transition is

$$W_{turn\text{-}off} = \tfrac{4}{3}V_I^2 C_{ds}(V_I) = \tfrac{4}{3} \times 100^2 \times 37.93 \times 10^{-12} = 505.73\,\text{nJ}. \tag{2.110}$$

The turn-off switching loss is

$$P_{turn\text{-}off} = \tfrac{4}{3} f_s V_I^2 C_{ds}(V_I) = \tfrac{4}{3} \times 100 \times 10^3 \times 100^2 \times 37.93 \times 10^{-12} = 50.573\,\text{mW}. \tag{2.111}$$

The turn-off equivalent linear capacitance is

$$C_{eq(r)} = \tfrac{8}{3}C_{ds}(V_I) = \tfrac{8}{3} \times 37.93 \times 10^{-12} = 101.1\,\text{pF}. \tag{2.112}$$

2.2.11 Power Losses and Efficiency of Buck Converter for CCM

An equivalent circuit of the buck converter with parasitic resistances is shown in Figure 2.9. In this figure, r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The slope of the $I_D - V_{DS}$ curves in the ohmic region is equal to the inverse of the MOSFET on-resistance $1/r_{DS}$. The MOSFET on-resistance r_{DS} increases with temperature because the mobility of electrons $\mu_n \approx K_1/T^{2.5}$ decreases with temperature T in the range from 100 to 400 K, where K_1 is a constant. Typically, r_{DS} doubles as the temperature rises by 100°C.

The large-signal model of a diode consists of a battery V_F in series with a forward resistance R_F. The voltage across the conducting diode is $V_D = V_F + R_F I_D$. If a line is drawn along the linear high-current portion of the $I_D - V_D$ curve (or $\log(I_D) - V_D$) extending to the V_D-axis, the intercept on the V_D-axis is V_F and the slope is $1/R_F$. The threshold voltage V_F is typically 0.7 V for silicon (Si) pn junction diodes, and $V_F = 2.8$ V for silicon carbide (SiC) pn junction diodes. The threshold voltage $V_F = 0.3$–0.4 V for Si Schottky diodes and is $V_F = 2$ V for SiC Schottky diodes. The threshold voltage V_F of Si diodes decreases with temperature at a rate of 2 mV/°C. The series resistance R_F of pn junction diodes decreases with the temperature, while the resistance R_F of Schottky diodes increases with temperature.

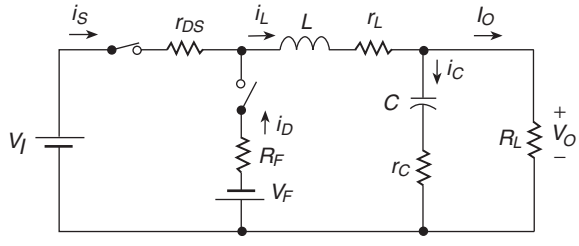


Figure 2.9 Equivalent circuit of the buck converter with parasitic resistances and the diode offset voltage.

The conduction losses will be evaluated assuming that the inductor current i_L is ripple-free and equals the dc output current I_O. Hence, the switch current can be approximated by

$$i_S = \begin{cases} I_O, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{2.113}$$

which results in its rms value

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \sqrt{\frac{1}{T}\int_0^{DT} I_O^2\, dt} = I_O\sqrt{D} \tag{2.114}$$

and the MOSFET conduction loss

$$P_{rDS} = r_{DS}I_{Srms}^2 = Dr_{DS}I_O^2 = \frac{Dr_{DS}}{R_L}P_O. \tag{2.115}$$

The transistor conduction loss P_{rDS} is proportional to the duty cycle D at a fixed load current I_O. At $D = 0$, the switch is OFF during the entire cycle and therefore the conduction loss is zero. At $D = 1$, the switch is ON during the entire cycle, resulting in a maximum conduction loss. Assuming that $D_{max} = V_O/V_{Imin}$ as for the lossless converter, the maximum MOSFET conduction power is

$$P_{rDSmax} = D_{max}r_{DS}I_{Omax}^2 = \frac{D_{max}r_{DS}}{R_{Lmin}}P_{Omax} \approx \frac{V_O}{V_{Imin}}\frac{r_{DS}}{R_{Lmin}}P_{Omax}. \tag{2.116}$$

Assuming that the transistor output capacitance C_o is linear, the switching loss is expressed by

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o V_O^2}{M_{V\,DC}^2} = \frac{f_s C_o R_L}{M_{V\,DC}^2}P_O. \tag{2.117}$$

The maximum switching loss is

$$P_{sw(max)} = f_s C_o V_{Imax}^2 = \frac{f_s C_o V_O^2}{M_{V\,DCmin}^2} = \frac{f_s C_o R_{Lmin} V_{Imax}^2}{V_O^2}P_O. \tag{2.118}$$

Excluding the MOSFET gate-drive power, the total power dissipation in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = Dr_{DS}I_O^2 + \frac{1}{2}f_s C_o V_I^2 = \left(\frac{Dr_{DS}}{R_L} + \frac{f_s C_o R_L}{2M_{V\,DC}^2}\right)P_{Omax}. \tag{2.119}$$

Similarly, the diode current can be approximated by

$$i_D = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ I_O, & \text{for } DT < t \le T, \end{cases} \tag{2.120}$$

yielding its rms value,

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \sqrt{\frac{1}{T}\int_{DT}^T I_O^2\, dt} = I_O\sqrt{1-D}, \tag{2.121}$$

and the power loss in R_F,

$$P_{RF} = R_F I_{Drms}^2 = (1-D)R_F I_O^2 = \frac{(1-D)R_F}{R_L}P_O. \tag{2.122}$$

The average value of the diode current is

$$I_D = \frac{1}{T}\int_0^T i_D\, dt = \frac{1}{T}\int_{DT}^T I_O\, dt = (1-D)I_O, \tag{2.123}$$

which gives the power loss associated with the voltage V_F,

$$P_{VF} = V_F I_D = (1-D)V_F I_O = \frac{(1-D)V_F}{V_O} P_O. \tag{2.124}$$

Thus, the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = (1-D)V_F I_O + (1-D)R_F I_O^2 = (1-D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right) P_O. \tag{2.125}$$

The diode conduction loss P_D decreases, when the duty cycle D increases at a fixed load current I_O. At $D = 0$, the diode is ON during the entire cycle, resulting in a maximum conduction loss. At $D = 1$, the diode is OFF during the entire cycle and therefore the conduction loss is zero. The maximum diode conduction loss is

$$P_{Dmax} = (1-D_{min})\left(\frac{V_F}{V_O} + \frac{R_F}{R_{Lmin}}\right) P_{Omax} \approx \left(1 - \frac{V_O}{V_{Imax}}\right)\left(\frac{V_F}{V_O} + \frac{R_F}{R_{Lmin}}\right) P_{Omax}. \tag{2.126}$$

Typically, the power loss in the inductor core can be ignored and only the copper loss in the inductor winding should be considered. The inductor current can be approximated by

$$i_L \approx I_O, \tag{2.127}$$

leading to its rms value

$$I_{Lrms} = I_O \tag{2.128}$$

and the inductor conduction loss

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 = \frac{r_L}{R_L} P_O. \tag{2.129}$$

The maximum power loss in the inductor is

$$P_{rLmax} = r_L I_{Omax}^2 = \frac{r_L}{R_{Lmin}} P_{Omax}. \tag{2.130}$$

Using (2.12), (2.44), and (2.51), the rms current through the filter capacitor is found to be

$$I_{Crms} = \sqrt{\frac{1}{T}\int_0^T i_C^2\, dt} = \frac{\Delta i_L}{\sqrt{12}} = \frac{V_O(1-D)}{\sqrt{12} f_s L}, \tag{2.131}$$

and the power loss in the filter capacitor

$$P_{rC} = r_C I_{Crms}^2 = \frac{r_C \Delta i_L^2}{12} = \frac{r_C V_O^2 (1-D)^2}{12 f_s^2 L^2} = \frac{r_C R_L (1-D)^2}{12 f_s^2 L^2} P_O. \tag{2.132}$$

The maximum power loss in the capacitor is

$$P_{rCmax} = \frac{r_C \Delta i_{Lmax}^2}{12} = \frac{r_C V_O^2 (1-D_{min})^2}{12 f_s^2 L^2} \approx \frac{r_C R_L \left(1 - \dfrac{V_O}{V_{Imax}}\right)^2}{12 f_s^2 L^2} P_{Omax}. \tag{2.133}$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} \\ &= D r_{DS} I_O^2 + f_s C_o V_I^2 + (1-D)(V_F I_O + R_F I_O^2) + r_L I_O^2 + \frac{r_C \Delta i_L^2}{12} \\ &= \left[\frac{D r_{DS}}{R_L} + \frac{f_s C_o R_L}{M_{V\,DC}^2} + (1-D)\left(\frac{V_F}{V_O} + \frac{R_F}{R_L}\right) + \frac{r_L}{R_L} + \frac{r_C R_L (1-D)^2}{12 f_s^2 L^2}\right] P_O. \end{aligned} \tag{2.134}$$

Thus, the converter efficiency is

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}$$

$$= \frac{1}{1 + \dfrac{Dr_{DS} + (1-D)R_F + r_L}{R_L} + \dfrac{(1-D)V_F}{V_O} + \dfrac{f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{r_C R_L (1-D)^2}{12 f_s^2 L^2}}. \quad (2.135)$$

For $D = 0$, the switch is OFF and the diode is ON, and the efficiency is

$$\eta = \frac{1}{1 + \dfrac{R_F + r_L}{R_L} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{r_C R_L}{12 f_s^2 L^2}}. \quad (2.136)$$

For $D = 1$, the switch is ON and the diode is OFF, and the efficiency is

$$\eta = \frac{1}{1 + \dfrac{r_{DS} + r_L}{R_L} + f_s C_o R_L}. \quad (2.137)$$

If the inductor peak-to-peak current ripple Δi_L is taken into account, the rms values of the switch is given by

$$I_{Srms} = \sqrt{\frac{D}{3}(I_{Smin}^2 + I_{Smin} I_{Smax} + I_{Smax}^2)} = I_O \sqrt{D} \sqrt{1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2}, \quad (2.138)$$

where $I_{Smin} = I_O - \Delta i_L/2$ and $I_{Smax} = I_O + \Delta i_L/2$. Similarly, the rms value of the diode current is

$$I_{Drms} = \sqrt{\frac{1-D}{3}(I_{Dmin}^2 + I_{Dmin} I_{Dmax} + I_{Dmax}^2)} = I_O \sqrt{1-D} \sqrt{1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2}, \quad (2.139)$$

where $I_{Dmin} = I_O - \Delta i_L/2$ and $I_{Dmax} = I_O + \Delta i_L/2$. The rms value of the inductor current is

$$I_{Lrms} = \sqrt{\frac{1}{3}(I_{Lmin}^2 + I_{Lmin} I_{Dmax} + I_{Lmax}^2)} = I_O \sqrt{1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2}. \quad (2.140)$$

For example, for $\Delta i_L/I_O = 0.1$, $I_{Lrms} = 1.0017 I_O$, and for $\Delta i_L/I_O = 0.5$, $I_{Lrms} = 1.0408 I_O$.

The conduction power loss in the MOSFET is given by

$$P_{rDS} = r_{DS} I_{Srms}^2 = r_{DS} D I_O^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2\right]. \quad (2.141)$$

The conduction power loss in the diode forward resistance is

$$P_{RF} = R_F I_{Drms}^2 = R_F (1-D) I_O^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2\right]. \quad (2.142)$$

Assuming that the inductor resistance r_L is independent of frequency, the power loss in the inductor winding is given by

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_L}{I_O}\right)^2\right]. \quad (2.143)$$

For example, for $\Delta i_L/I_O = 0.1$,

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 \left[1 + \frac{1}{12}\left(\frac{1}{10}\right)^2\right] = P_O \left(1 + \frac{1}{1200}\right) = 1.0008333 P_O. \quad (2.144)$$

For $\Delta i_L/I_O = 0.2$,

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 \left[1 + \frac{1}{12}\left(\frac{1}{5}\right)^2\right] = P_O\left(1 + \frac{1}{300}\right) = 1.00333 P_O. \tag{2.145}$$

In the buck converter, the dc input power is partially transferred directly to the output and is converted to ac power and then is converted back to dc power. It can be shown that the amount of power which is converted to ac power is

$$P_{AC} = (1 - D)P_O, \tag{2.146}$$

and the amount of the dc power that directly flows to the output is

$$P_{DC} = DP_O. \tag{2.147}$$

2.2.12 DC Voltage Transfer Function of Lossy Converter for CCM

The dc component of the input current is

$$I_I = \frac{1}{T}\int_0^T i_S\, dt = \frac{1}{T}\int_0^{DT} I_O\, dt = DI_O, \tag{2.148}$$

leading to the dc current transfer function of the buck converter,

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{1}{D}. \tag{2.149}$$

This equation holds true for both lossless and lossy converters. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = \frac{M_{V\,DC}}{D}, \tag{2.150}$$

from which the voltage transfer function of the lossy buck converter is

$$\begin{aligned} M_{V\,DC} &= \frac{\eta}{M_{I\,DC}} = \eta D \\ &= \frac{D}{1 + \dfrac{Dr_{DS} + (1-D)R_F + r_L}{R_L} + \dfrac{(1-D)V_F}{V_O} + \dfrac{f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{r_C R_L (1-D)^2}{12 f_s^2 L^2}}. \end{aligned} \tag{2.151}$$

For $D = 1$, $M_{V\,DC} = \eta < 1$.

From (2.151), the on-duty cycle is

$$D = \frac{M_{V\,DC}}{\eta} = \frac{V_O}{\eta V_I}. \tag{2.152}$$

The duty cycle D at a given dc voltage transfer function is higher for the lossy converter than that of a lossless converter. This is because the switch S must be closed for a longer period of time for the lossy converter to transfer enough energy to supply both the required output energy and the converter losses.

Substitution of (2.152) into (2.135) gives the converter efficiency

$$\eta = \frac{N_\eta}{D_\eta}, \tag{2.153}$$

where

$$N_\eta = 1 + M_{V\,DC}\left(\frac{V_F}{V_O} + \frac{r_C R_L}{6f_s^2 L^2} - \frac{r_{DS} - R_F}{R_L}\right) + \left\{\left[1 + M_{V\,DC}\left(\frac{V_F}{V_O} + \frac{r_C R_L}{6f_s^2 L^2} - \frac{r_{DS} - R_F}{R_L}\right)\right]^2 - \frac{M_{V\,DC}^2 r_C R_L}{3f_s^2 L^2}\left(1 + \frac{R_F + r_L}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{12 f_s^2 L^2}\right)\right\}^{\frac{1}{2}} \quad (2.154)$$

and

$$D_\eta = 2\left(1 + \frac{R_F + r_L}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{12 f_s^2 L^2}\right). \quad (2.155)$$

2.2.13 MOSFET Gate-drive Power

When the transistor is driven by a square-wave voltage source, the MOSFET gate-drive power is associated with charging the transistor input capacitance when the gate-to-source voltage increases and discharging this capacitance when the gate-to-source voltage decreases. Unfortunately, the input capacitance of power MOSFETs is highly nonlinear and therefore it is difficult to determine the gate-drive power, using the transistor input capacitance. In manufactures' data sheets, a total gate charge Q_g stored in the gate-to-source capacitance and the gate-to-drain capacitance is given at a specified gate-to-source voltage V_{GS} (usually, $V_{GS} = 10\,\text{V}$) and a specified drain-to-source voltage V_{DS} (usually, $V_{DS} = 0.8$ of the maximum rating). Using a square-wave voltage source to drive the MOSFET gate, the energy transferred from the gate-drive source to the transistor is

$$W_G = Q_g V_{GSpp}. \quad (2.156)$$

This energy is lost during one cycle T of the switching frequency $f_s = 1/T$ for charging and discharging the MOSFET input capacitance. Thus, the MOSFET gate-drive power is

$$P_G = \frac{W_G}{T} = f_s W_G = f_s Q_g V_{GSpp}. \quad (2.157)$$

The gate-drive power P_G is proportional to the switching frequency f_s.

The *power gain* is defined by

$$k_p = \frac{P_O}{P_G}. \quad (2.158)$$

The *power-added efficiency* (PAE) incorporates the gate-drive power P_G by subtracting it from the output power P_O and is defined by

$$\eta_{PAE} = \frac{P_O - P_G}{P_I}. \quad (2.159)$$

If the power gain k_p is high, $\eta_{PAE} \approx \eta$. If the power gain $k_p < 1$, $\eta_{PAE} < 0$.

The *total efficiency* is defined by

$$\eta_t = \frac{P_O}{P_I + P_G}. \quad (2.160)$$

The *average efficiency* is defined by

$$\eta_{AVG} = \frac{P_{OAVG}}{P_{IAVG}}. \quad (2.161)$$

In order to determine this efficiency, the probability density functions of the average input and output powers are required.

2.2.14 Design of Buck Converter for CCM

Design a PWM buck converter operating in CCM to meet the following specifications: $V_I = 28 \pm 4\,\text{V}$, $V_O = 12\,\text{V}$, $I_{Omin} = 1\,\text{A}$, $I_{Omax} = 10\,\text{A}$, $f_s = 100\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$.

Solution. The minimum, nominal, and maximum values of the input voltage are $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$. The maximum and minimum values of the dc output power are

$$P_{Omax} = V_O I_{Omax} = 12 \times 10 = 120\,\text{W} \tag{2.162}$$

and

$$P_{Omin} = V_O I_{Omin} = 12 \times 1 = 12\,\text{W}. \tag{2.163}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{10} = 1.2\,\Omega \tag{2.164}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{12}{1} = 12\,\Omega. \tag{2.165}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{12}{32} = 0.375, \tag{2.166}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{12}{28} = 0.43, \tag{2.167}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{12}{24} = 0.5. \tag{2.168}$$

Assume the converter efficiency is $\eta = 85\,\%$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{M_{V\,DCmin}}{\eta} = \frac{0.375}{0.85} = 0.441, \tag{2.169}$$

$$D_{nom} = \frac{M_{V\,DCnom}}{\eta} = \frac{0.43}{0.85} = 0.506, \tag{2.170}$$

and

$$D_{max} = \frac{M_{V\,DCmax}}{\eta} = \frac{0.5}{0.85} = 0.588. \tag{2.171}$$

Assuming the switching frequency is $f_s = 100\,\text{kHz}$, the minimum inductance that is required to maintain the converter in CCM is

$$L_{min} = \frac{R_{Lmax}(1 - D_{min})}{2f_s} = \frac{12 \times (1 - 0.441)}{2 \times 10^5} = 33.54\,\mu\text{H}. \tag{2.172}$$

Let $L = 40\,\mu\text{H}/0.05\,\Omega$.

The maximum inductor ripple current is

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L} = \frac{12 \times (1 - 0.441)}{10^5 \times 40 \times 10^{-6}} = 1.677\,\text{A}. \tag{2.173}$$

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{12}{100} = 120\,\text{mV}. \tag{2.174}$$

If the filter capacitance is large enough, $V_r = r_{Cmax}\Delta i_{Lmax}$ and the maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{120 \times 10^{-3}}{1.677} = 71.56\,\text{m}\Omega. \tag{2.175}$$

Let $r_C = 50\,\text{m}\Omega$. The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is

$$\begin{aligned} C_{min} &= \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{1 - D_{min}}{2f_s r_C}\right\} = \frac{D_{max}}{2f_s r_C} \\ &= \frac{0.588}{2 \times 10^5 \times 50 \times 10^{-3}} = 58.8\,\mu\text{F}. \end{aligned} \tag{2.176}$$

Pick $C = 100\,\mu\text{F}/25\,\text{V}/50\,\text{m}\Omega$.

The corner frequency of the output low-pass filter is

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{40 \times 10^{-6} \times 100 \times 10^{-6}}} = 2.516\,\text{kHz}. \tag{2.177}$$

Thus, $f_s/f_o = 100/2.516 = 39.75$.

The power MOSFET and diode voltage and current stresses are

$$V_{SMmax} = V_{DMmax} = V_{Imax} = 32\,\text{V} \tag{2.178}$$

and

$$I_{SMmax} = I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = 10 + \frac{1.677}{2} = 10.839\,\text{A}. \tag{2.179}$$

An International Rectifier IRF150 power MOSFET is selected, which has $V_{DSS} = 100\,\text{V}$, $I_{SM} = 40\,\text{A}$, $r_{DS} = 55\,\text{m}\Omega$, $C_o = 100\,\text{pF}$, and $Q_g = 63\,\text{nC}$. Also, an MBR1060 Schottky barrier diode is chosen, which has $I_{DM} = 20\,\text{A}$, $V_{DM} = 60\,\text{V}$, $V_F = 0.4\,\text{V}$, and $R_F = 25\,\text{m}\Omega$.

The power losses and the efficiency will be calculated at full load resistance $R_{Lmin} = 1.2\,\Omega$, and the maximum dc input voltage $V_{Imax} = 32\,\text{V}$, which corresponds to the minimum duty cycle $D_{min} = 0.441$. The conduction power loss in the MOSFET is

$$P_{rDS} = D_{min} r_{DS} I_{Omax}^2 = 0.441 \times 0.055 \times 10^2 = 2.426\,\text{W}, \tag{2.180}$$

and the switching loss is

$$P_{sw} = f_s C_o V_{Imax}^2 = 10^5 \times 100 \times 10^{-12} \times 32^2 = 0.01\,\text{W}. \tag{2.181}$$

Hence, the total power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 2.426 + 0.005 = 2.431\,\text{W}. \tag{2.182}$$

However, the maximum conduction power loss in the MOSFET occurs at $V_{Imax} = 32\,\text{V}$, $R_{Lmin} = 1.2\,\Omega$, and $D_{max} = 0.588$.

The diode loss due to V_F is

$$P_{VF} = (1 - D_{min}) V_F I_{Omax} = (1 - 0.441) \times 0.4 \times 10 = 2.236\,\text{W}, \tag{2.183}$$

the diode loss due to R_F is

$$P_{RF} = (1 - D_{min})R_F I_{Omax}^2 = (1 - 0.441) \times 0.025 \times 10^2 = 1.398\,\text{W}, \tag{2.184}$$

and the total diode conduction loss is

$$P_D = P_{VF} + P_{RF} = 2.236 + 1.398 = 3.634\,\text{W}. \tag{2.185}$$

The power loss in the inductor with dc ESR $r_L = 50\,\text{m}\Omega$ is

$$P_{rL} = r_L I_{Omax}^2 = 0.05 \times 10^2 = 5\,\text{W}. \tag{2.186}$$

The power loss in the capacitor ESR is

$$P_{rC} = \frac{r_C(\Delta i_{Lmax})^2}{12} = \frac{0.05 \times 1.677^2}{12} = 0.012\,\text{W}. \tag{2.187}$$

The total power loss is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} \\ &= 2.426 + 0.01 + 3.634 + 5 + 0.012 = 11.082\,\text{W}, \end{aligned} \tag{2.188}$$

and the efficiency of the converter at full load is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{120}{120 + 11.082} = 91.55\,\%. \tag{2.189}$$

If the assumed efficiency is much different than that calculated in (2.189), a further iteration step is needed with a new assumed converter efficiency.

Note that the maximum conduction power loss in the MOSFET occurs at $V_{Imin} = 24\,\text{V}$ and $R_{Lmin} = 1.2\,\Omega$ and is given by

$$P_{rDS} = D_{max} r_{DS} I_{Omax}^2 = 0.588 \times 0.055 \times 10^2 = 3.234\,\text{W}. \tag{2.190}$$

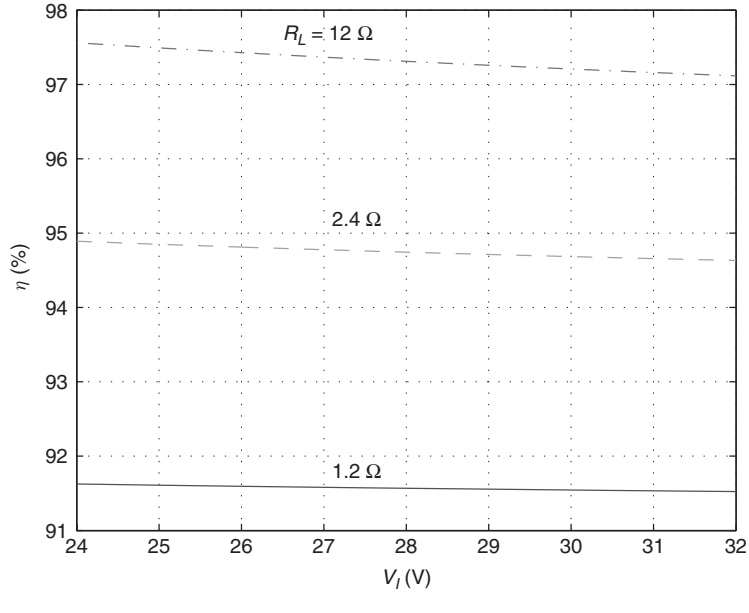


Figure 2.10 Efficiency η of the designed buck converter as a function of dc input voltage V_I for CCM at $R_L = 1.2\,\Omega$, $2.4\,\Omega$, and $12\,\Omega$.

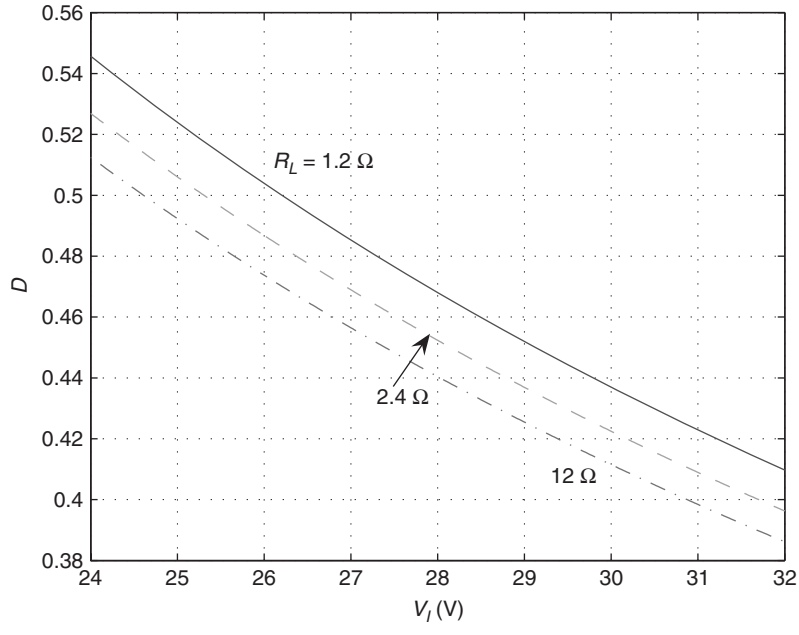


Figure 2.11 Duty cycle D of the designed buck converter as a function of dc input voltage V_I for CCM at $R_L = 1.2\,\Omega$, $2.4\,\Omega$, and $12\,\Omega$.

Assuming that the peak-to-peak gate-to-source voltage is $V_{GSpp} = 16\,\text{V}$, the MOSFET gate-drive power is

$$P_G = f_s Q_g V_{GSpp} = 10^5 \times 63 \times 10^{-9} \times 16 = 100.8\,\text{mW}. \tag{2.191}$$

The efficiency η of the designed buck converter was computed from (2.153)–(2.155) over the entire range of the specified operating conditions. Next, the duty cycle D was computed from (2.152), using the calculated efficiency η. The plots of η and D as functions of V_I, I_O, and R_L are shown in Figures 2.10–2.15. The converter efficiency η decreases as the load current I_O increases (or the load resistance R_L decreases). The minimum efficiency η_{min} occurs at the maximum load current I_{Omax} and the maximum dc input voltage V_{Imax}. The duty cycle D decreases when V_I increases, and D increases when I_O increases (or R_L decreases).

2.3 DC Analysis of PWM Buck Converter for DCM

Equivalent circuits for the PWM buck converter operating in the DCM are depicted in Figure 2.16. Idealized current and voltage waveforms are shown in Figure 2.17. At time $t = 0$ when the switch is turned on, the inductor current is zero. For the time interval $0 < t \leq DT$, the switch is ON and the diode is OFF as depicted in Figure 2.16(b). The voltage across the diode is $-V_I$. The voltage across the inductor is $V_I - V_O$ and causes the inductor current to increase linearly from zero. At time $t = DT$, the switch is turned off and the inductor current is diverted from the switch to the freewheeling diode. The equivalent

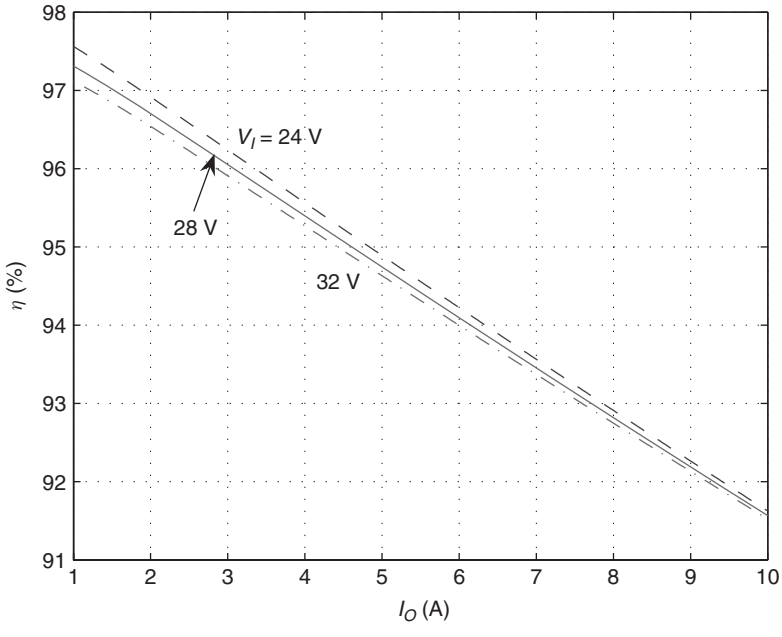


Figure 2.12 Efficiency η of the designed buck converter as a function of load current I_O for CCM at $V_I = 24\,\text{V}$, 28 V, and 32 V.

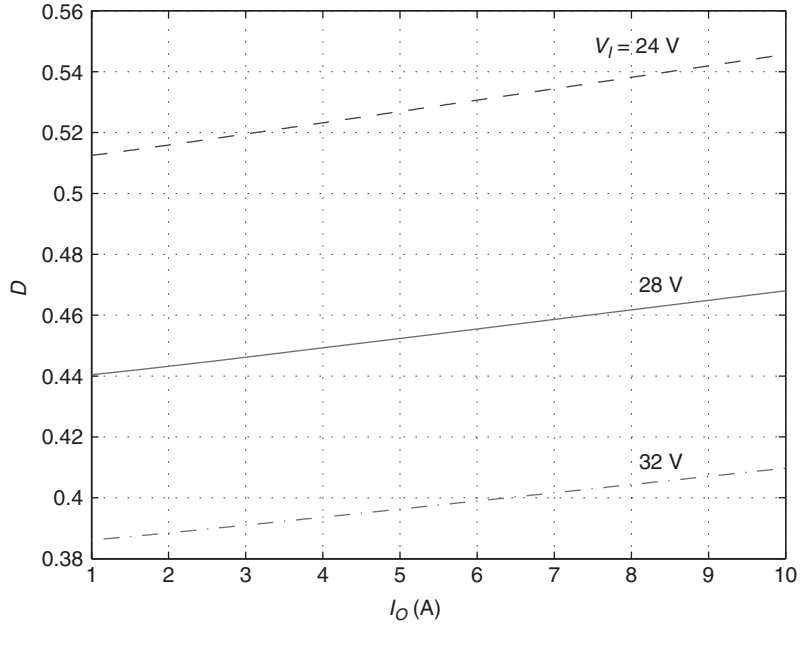


Figure 2.13 Duty cycle D of the designed buck converter as a function of load current I_O for CCM at $V_I = 24\,\text{V}$, 28 V, and 32 V.

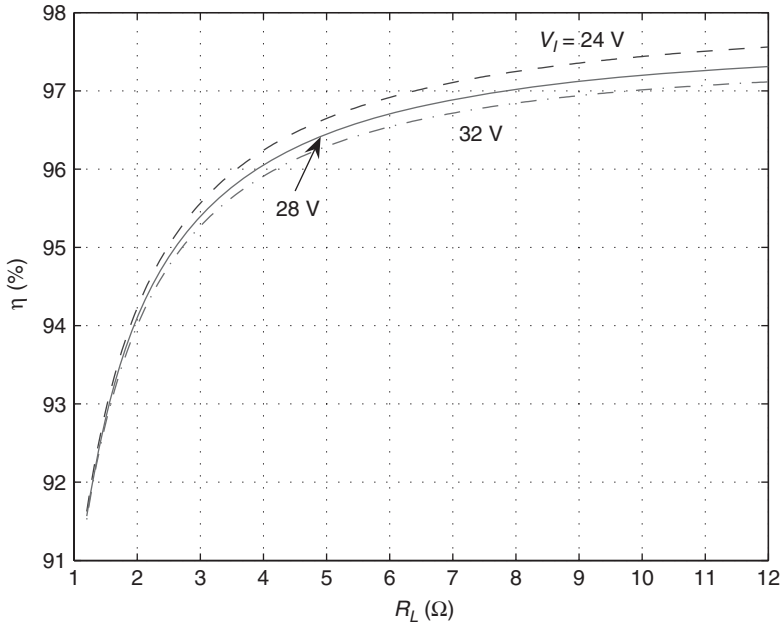


Figure 2.14 Efficiency η of the designed buck converter as a function of load resistance R_L for CCM at $V_I = 24\,\text{V}$, 28 V, and 32 V.

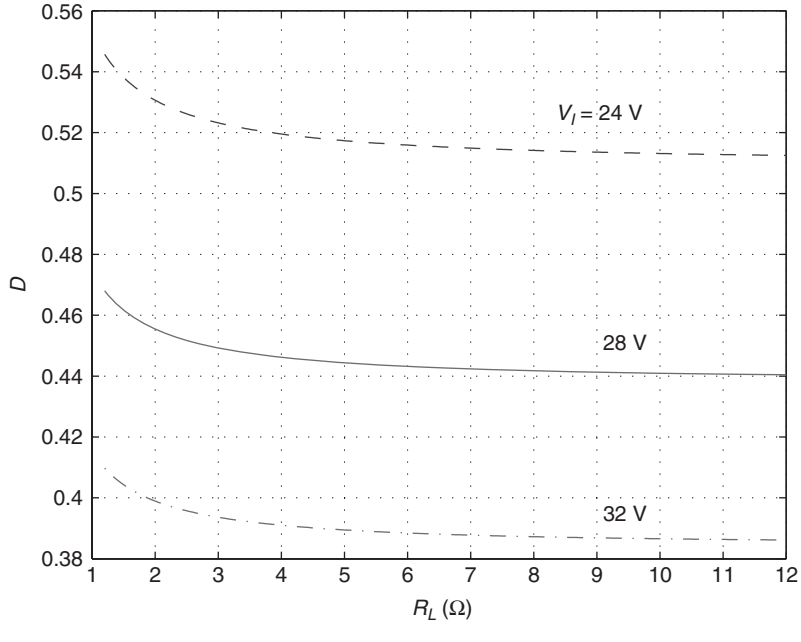


Figure 2.15 Duty cycle D of the designed buck converter as a function of load resistance R_L for CCM at $V_I = 24\,\text{V}$, 28 V, and 32 V.

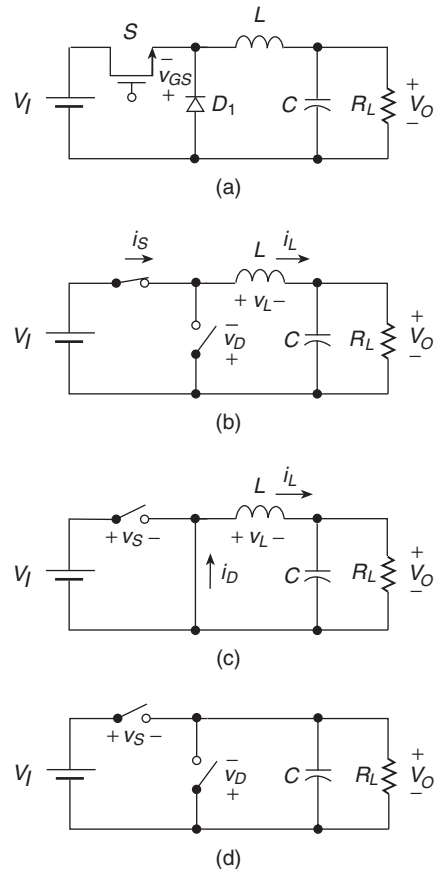


Figure 2.16 PWM buck converter and its ideal equivalent circuits for DCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON. (d) Equivalent circuit when both the switch and the diode are OFF.

circuit is shown in Figure 2.16(c) for time interval $DT < t \leq (D + D_1)T$. The voltage across the switch is V_I. The voltage across the inductor is $-V_O$, causing the inductor current to decrease linearly. This current flows through the diode. At time $t = (D + D_1)T$, the diode current reaches zero and the diode begins to turn off. Since the diode cannot conduct negative current (neglecting the reverse recovery current), the inductor current remains zero until the switch is turned on at time $t = T$. Figure 2.16(d) shows the equivalent circuit for time interval $(D + D_1)T < t \leq T$. The voltage across the inductor is zero because its current is constant and equals zero. At time $t = T$, the switch is turned on and the inductor current increases from zero.

2.3.1 Time Interval $0 < t \leq DT$

During this time interval, the switch is ON and the diode is OFF. The equivalent circuit is shown in Figure 2.16(b). The switch voltage v_S and the diode current i_D are zero. The

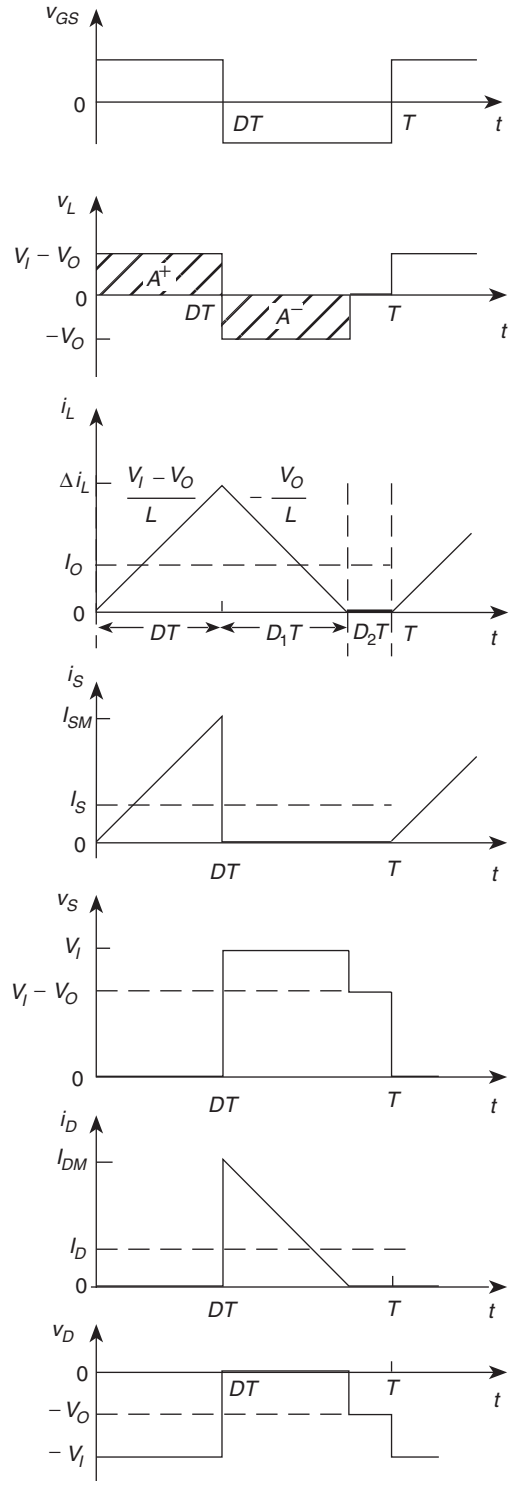


Figure 2.17 Idealized current and voltage waveforms in the PWM buck converter for DCM.

voltage across the inductor L is

$$v_L = V_I - V_O = L\frac{di_L}{dt}, \qquad i_L(0) = 0. \tag{2.192}$$

Hence, the inductor and switch current is

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\,dt = \frac{1}{L}\int_0^t (V_I - V_O)\,dt = \frac{V_I - V_O}{L}t. \tag{2.193}$$

Thus, the peak switch and inductor current is

$$I_{SM} = \Delta i_L = i_L(DT) = \frac{(V_I - V_O)DT}{L} = \frac{(V_I - V_O)D}{f_s L}. \tag{2.194}$$

The voltage across the diode is

$$v_D = -V_I. \tag{2.195}$$

The end of this time interval occurs when the switch is turned off by the driver.

2.3.2 Time Interval $DT < t \le (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 2.16(c). The switch is OFF and the diode is ON. Hence, $i_S = 0$ and $v_D = 0$. The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{2.196}$$

and the inductor and diode currents are obtained using (2.194),

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{DT}^t v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^t (-V_O)\,dt + i_L(DT) \\ &= -\frac{V_O}{L}(t - DT) + i_L(DT) = -\frac{V_O}{L}(t - DT) + \frac{(V_I - V_O)DT}{L}. \end{aligned} \tag{2.197}$$

These currents can also be derived as

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{(D+D_1)T}^t v_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^t (-V_O)\,dt \\ &= -\frac{V_O}{L}[t - (D + D_1)T] = -\frac{V_O}{L}(t - DT) + \frac{V_O D_1 T}{L} \\ &= -\frac{V_O}{L}(t - DT) + i_L(DT). \end{aligned} \tag{2.198}$$

Hence, the peak diode and inductor currents are given by

$$I_{DM} = \Delta i_L = i_L(DT) = \frac{D_1 V_O}{f_s L} \tag{2.199}$$

or

$$I_{DM} = \Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^{DT} (-V_O)\,dt = \frac{V_O D_1 T}{L} = \frac{V_O D_1}{f_s L}. \tag{2.200}$$

The peak voltage across the switch is

$$V_{SM} = V_I. \tag{2.201}$$

This time interval ends when the diode current reaches zero.

2.3.3 Time Interval $(D + D_1)T < t \leq T$

During this time interval, both the switch and the diode are OFF. The equivalent circuit is shown in Figure 2.16(d). The inductor current i_L, the inductor voltage v_L, the switch current i_S, and the diode current i_D are zero. The voltage across the switch is

$$v_S = V_I - V_O \tag{2.202}$$

and the voltage across the diode is

$$v_D = -V_O. \tag{2.203}$$

This time interval ends when the switch is turned on by the driver.

2.3.4 Device Stresses for DCM

Using (2.7) and (2.14), one obtains the voltage stress of the switch and the diode in DCM for steady-state operation,

$$V_{SMmax} = V_{DMmax} = V_{Imax}. \tag{2.204}$$

From (2.194), the current stress of the switch and the diode in DCM for steady-state operation is

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{(V_{Imax} - V_O)D_{min}}{f_s L}. \tag{2.205}$$

2.3.5 DC Voltage Transfer Function for DCM

Referring to Figure 2.17 and using the volt-second balance principle, $A^+ = A^-$. Hence,

$$(V_I - V_O)DT = V_O D_1 T, \tag{2.206}$$

which leads to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{D + D_1}. \tag{2.207}$$

From (2.194) and (2.207), the peak-to-peak value of the inductor current is

$$\Delta i_L = \frac{(V_I - V_O)DT}{L} = \frac{V_O D(1 - M_{V\,DC})}{f_s L M_{V\,DC}}. \tag{2.208}$$

The dc output current is equal to the average value of the inductor current,

$$I_O = \frac{1}{T}\int_0^T i_L\,dt = \frac{(D + D_1)\Delta i_L}{2} = \frac{V_{OD}(D + D_1)(1 - M_{V\,DC})}{2 f_s L M_{V\,DC}}. \tag{2.209}$$

Substitution of (2.207) into (2.209) yields

$$I_O = \frac{V_O D^2(1 - M_{V\,DC})}{2 f_s L M_{V\,DC}^2} = \frac{V_O}{R_L}, \tag{2.210}$$

which can be rearranged to the form

$$D = \sqrt{\frac{2 f_s L M_{V\,DC}^2 I_O}{(1 - M_{V\,DC})V_O}} = \sqrt{\frac{2 f_s L M_{V\,DC}^2}{R_L(1 - M_{V\,DC})}}, \quad \text{for } D \leq 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}. \tag{2.211}$$

Thus, the duty cycle D increases with increasing I_O when V_O and $M_{V\,DC}$ (or V_I) are held constant. The inductance required to obtain a desired dc voltage transfer function at given values of D, R_L, and f_s is

$$L = \frac{D^2 R_L (1 - M_{V\,DC})}{2 f_s M_{V\,DC}^2}. \tag{2.212}$$

At the boundary between CCM and DCM,

$$M_{V\,DCB} = D_B \tag{2.213}$$

as in CCM. Substitution of this into (2.211) yields the duty cycle D_B at the boundary,

$$M_{V\,DCB} = D_B = 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}. \tag{2.214}$$

As the normalized load current $I_O/(V_O/2f_sL)$ is increased from 0 to 1, the boundary duty cycle D_B decreases from 1 to 0. At D close to 1, the converter operates in CCM at practically any load. At D close to zero, there is a large load range in which the converter operates in DCM. Figures 2.18 and 2.19 show plots of D versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of $M_{V\,DC}$ for both CCM and DCM for the lossless buck converter, respectively.

Rearranging (2.211), one obtains

$$\frac{2 f_s L}{D^2 R_L} M_{V\,DC}^2 + M_{V\,DC} - 1 = 0. \tag{2.215}$$

Solving this equation for $M_{V\,DC}$ gives

$$\begin{aligned} M_{V\,DC} &= \frac{2}{1 + \sqrt{1 + \dfrac{8 f_s L}{D^2 R_L}}} = \frac{2}{1 + \sqrt{1 + \dfrac{8 f_s L I_O}{D^2 V_O}}}, \quad \text{for } M_{V\,DC} \le 1 - \frac{2 f_s L}{R_L} \\ &= 1 - \frac{2 f_s L I_O}{V_O}. \end{aligned} \tag{2.216}$$

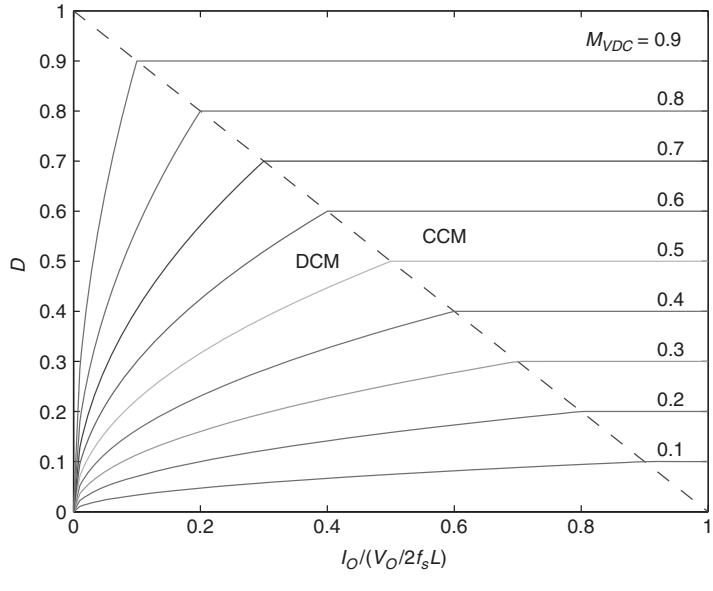


Figure 2.18 Duty cycle D as a function of the normalized load current $I_O/(V_O/2f_sL)$ at various values of $M_{V\,DC}$ for the lossless buck converter.

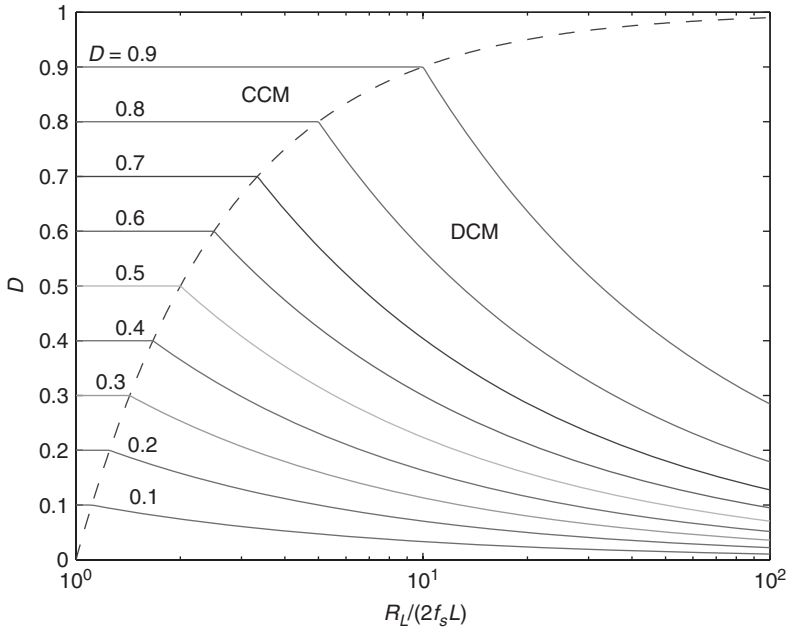


Figure 2.19 Duty cycle D as a function of the normalized load resistance $R_L/(2f_sL)$ at various values of $M_{V\,DC}$ for the lossless buck converter.

The dc voltage transfer function depends on the load resistance R_L for DCM. Figures 2.20 and 2.21 display $M_{V\,DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of D for both CCM and DCM for the lossless buck converter, respectively.

Using (2.207) and (2.216), D_1 can be expressed in terms of D, R_L, f_s, and L as

$$D_1 = D\left(\frac{1}{M_{V\,DC}} - 1\right) = \sqrt{\frac{2f_sL(1 - M_{V\,DC})}{R_L}} = \frac{D}{2}\left(\sqrt{1 + \frac{8f_sL}{D^2R_L}} - 1\right). \tag{2.217}$$

It can be seen that D_1 depends on D, R_L, L, and f_s.

2.3.6 Maximum Inductance for DCM

Figure 2.22 shows the waveforms of the inductor current at the CCM/DCM boundary for $V_I = V_{Imin}$ and $V_I = V_{Imax}$. Using (2.38), the minimum value of the inductor peak current at the CCM/DCM boundary is

$$\Delta i_{Lmin} = \frac{V_O(1 - D_{Bmax})}{f_sL_{max}}. \tag{2.218}$$

Therefore, the dc output current at the boundary can be expressed as

$$I_{OB} = I_{Omax} = \frac{\Delta i_{Lmin}}{2} = \frac{V_O(1 - D_{Bmax})}{2f_sL_{max}} = \frac{V_O}{R_{Lmin}}, \tag{2.219}$$

which yields

$$L_{max} = \frac{R_{Lmin}(1 - D_{Bmax})}{2f_s}, \tag{2.220}$$

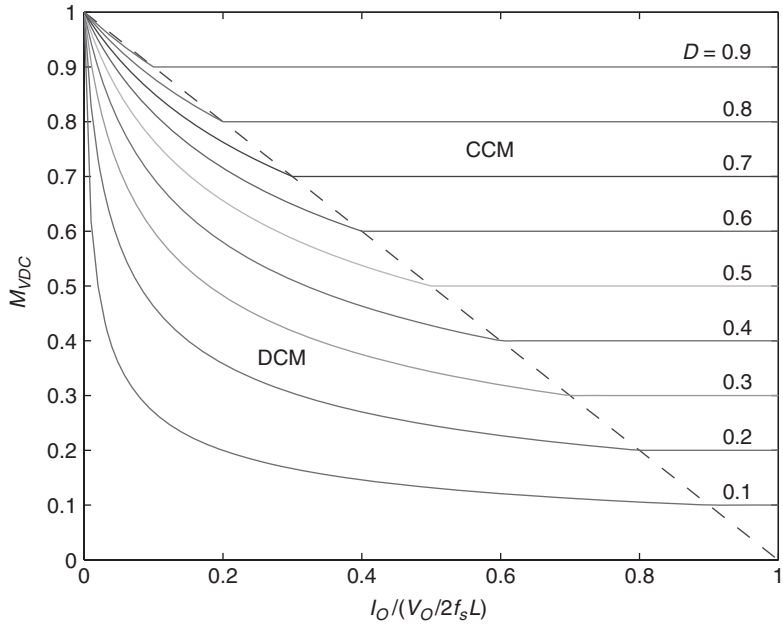


Figure 2.20 DC voltage transfer function $M_{V\,DC}$ as a function of the normalized load current $I_O/(V_O/2f_sL)$ at fixed values of D for the lossless buck converter.

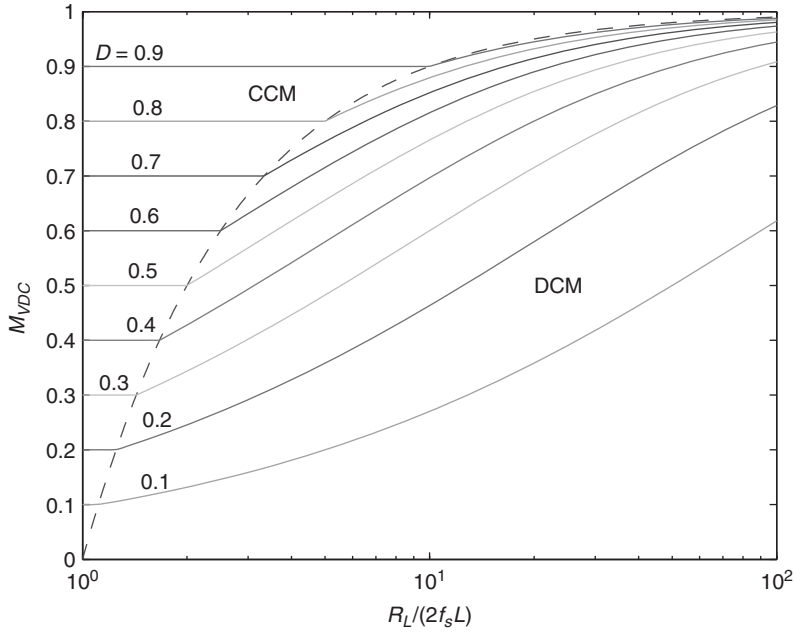


Figure 2.21 DC voltage transfer function $M_{V\,DC}$ as a function of the normalized load resistance $R_L/(2f_sL)$ at fixed values of D for the lossless buck converter.

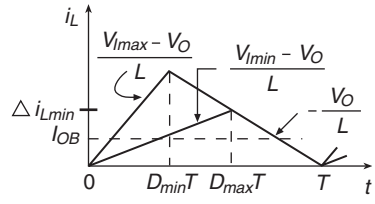


Figure 2.22 Waveforms of the inductor current at the CCM/DCM boundary for $V_I = V_{Imin}$ and $V_I = V_{Imax}$.

where D_{Bmax} is the maximum duty cycle at the CCM/DCM boundary and is given by

$$D_{Bmax} = \frac{M_{V\,DCmax}}{\eta} = \frac{V_O}{\eta V_{Imin}}. \tag{2.221}$$

The filter capacitor can be designed using the same approach as that for CCM. The maximum ripple voltage occurs at full power, for which the inductor waveform is close to that for the CCM/DCM boundary.

2.3.7 Power Losses and Efficiency of Buck Converter for DCM

Substitution of (2.207) into (2.208) yields the inductor, switch, and diode peak current

$$\Delta i_L = I_{SM} = I_{DM} = \frac{DV_O}{f_s L}\left(\frac{1}{M_{V\,DC}} - 1\right) = V_O\sqrt{\frac{2(1 - M_{V\,DC})}{f_s L R_L}}. \tag{2.222}$$

Using this expression, one obtains the rms value of the switch current

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2\, dt} = \Delta i_L\sqrt{\frac{D}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2M_{V\,DC}^2(1 - M_{V\,DC})}{f_s L R_L}}} \tag{2.223}$$

and the conduction loss in the MOSFET

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{r_{DS} D\,\Delta i_L^2}{3} = \frac{2r_{DS}}{3}\sqrt{\frac{2M_{V\,DC}^2(1 - M_{V\,DC})}{f_s L R_L}} P_O. \tag{2.224}$$

The switching loss is

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o V_O^2}{M_{V\,DC}^2} = \frac{f_s C_o R_L}{M_{V\,DC}^2} P_O. \tag{2.225}$$

The total power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \left[\frac{2r_{DS}}{3}\sqrt{\frac{2M_{V\,DC}^2(1 - M_{V\,DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{2M_{V\,DC}^2}\right] P_O. \tag{2.226}$$

Using (2.217) and (2.222), one arrives at the rms value of the diode current

$$I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} i_D^2\, dt} = \Delta i_L\sqrt{\frac{D_1}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2(1 - M_{V\,DC})^3}{f_s L R_L}}}, \tag{2.227}$$

which gives the diode conduction loss due to R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{D_1 R_F \Delta i_L^2}{3} = \frac{2R_F}{3}\sqrt{\frac{2(1-M_{V\,DC})^3}{f_s L R_L}}P_O. \tag{2.228}$$

Using (2.197), (2.209), (2.217), and (2.222), one obtains the average diode current

$$I_D = \frac{1}{T}\int_0^T i_D\,dt = \frac{D^2 V_O}{2f_s L}\left(\frac{1}{M_{V\,DC}} - 1\right)^2 = I_O(1 - M_{V\,DC}), \tag{2.229}$$

resulting in the diode conduction loss due to V_F,

$$P_{VF} = V_F I_D = V_F I_O(1 - M_{V\,DC}) = \frac{V_F(1 - M_{V\,DC})}{V_O}P_O. \tag{2.230}$$

Hence, the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = \left[\frac{V_F(1 - M_{V\,DC})}{V_O} + \frac{2R_F}{3}\sqrt{\frac{2(1-M_{V\,DC})^3}{f_s L R_L}}\right]P_O. \tag{2.231}$$

Using (2.217) and (2.222), one obtains the rms value of the inductor current

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^{(D+D_1)T} i_L^2\,dt} = \Delta i_L\sqrt{\frac{D + D_1}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2(1 - M_{V\,DC})}{f_s L R_L}}}, \tag{2.232}$$

which leads to the power loss in the inductor ESR,

$$P_{rL} = r_L I_{Lrms}^2 = \frac{r_L \Delta i_L^2 (D + D_1)}{3} = \frac{2r_L}{3}\sqrt{\frac{2(1 - M_{V\,DC})}{f_s L R_L}}P_O. \tag{2.233}$$

Neglecting the power loss in the ESR of the filter capacitor, the total converter power loss is given by

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} \\ &= \left[\frac{2r_{DS}}{3}\sqrt{\frac{2M_{V\,DC}^2(1 - M_{V\,DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{M_{V\,DC}^2} + \frac{2R_F}{3}\sqrt{\frac{2(1 - M_{V\,DC})^3}{f_s L R_L}}\right. \\ &\quad \left. + \frac{V_F(1 - M_{V\,DC})}{V_O} + \frac{2r_L}{3}\sqrt{\frac{2(1 - M_{V\,DC})}{f_s L R_L}}\right]P_O. \end{aligned} \tag{2.234}$$

The efficiency of the buck converter in DCM is defined as

$$\eta \equiv \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}, \tag{2.235}$$

which gives

$$\begin{aligned} \eta = \left[1 + \frac{2r_{DS}}{3}\sqrt{\frac{2M_{V\,DC}^2(1 - M_{V\,DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{M_{V\,DC}^2} + \frac{2R_F}{3}\sqrt{\frac{2(1 - M_{V\,DC})^3}{f_s L R_L}}\right. \\ \left. + \frac{V_F(1 - M_{V\,DC})}{V_O} + \frac{2r_L}{3}\sqrt{\frac{2(1 - M_{V\,DC})}{f_s L R_L}}\right]^{-1}. \end{aligned} \tag{2.236}$$

The dc input current of the converter is described by

$$I_I = \frac{1}{T}\int_0^{DT} i_S\,dt = \frac{1}{T}\int_0^{DT}\frac{(V_I - V_O)t}{L}dt = \frac{D^2(V_I - V_O)}{2f_s L}, \tag{2.237}$$

yielding the dc input power

$$P_I = V_I I_I = \frac{D^2(V_I^2 - V_O V_I)}{2 f_s L}. \tag{2.238}$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{2.239}$$

Using the definition of the efficiency,

$$\eta = \frac{P_O}{P_I} = \frac{2 f_s L M_{V\,DC}^2}{D^2 R_L (1 - M_{V\,DC})}, \tag{2.240}$$

one obtains the duty cycle

$$D = \sqrt{\frac{2 f_s L M_{V\,DC}^2 I_O}{\eta V_O (1 - M_{V\,DC})}} = \sqrt{\frac{2 f_s L M_{V\,DC}^2}{\eta R_L (1 - M_{V\,DC})}}, \quad \text{for } D < 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}, \tag{2.241}$$

and the dc voltage transfer function of the lossy buck converter for DCM,

$$M_{V\,DC} = \frac{2}{1 + \sqrt{1 + \dfrac{8 f_s L}{\eta D^2 R_L}}} = \frac{2}{1 + \sqrt{1 + \dfrac{8 f_s L I_O}{\eta D^2 V_O}}}, \quad \text{for } D < 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}. \tag{2.242}$$

At the CCM/DCM boundary $D = D_1 = 0.5$ and $\Delta i_L / I_O = 2$. Hence, the power loss in the inductor winding is given by

$$P_{rL} = r_L I_{Lrms}^2 = r_L \left[1 + \frac{1}{3} \left(\frac{\Delta i_L}{I_O} \right)^2 \right] = P_O \left(1 + \frac{1}{3} \times 2^2 \right) = 2.3333 P_O. \tag{2.243}$$

2.3.8 Design of Buck Converter for DCM

Design a PWM buck converter to meet the following specifications: $P_{Omin} = 0$, $P_{Omax} = 120\,\text{W}$, $V_O = 12\,\text{V}$, $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, $V_{Imax} = 32\,\text{V}$, $f_s = 100\,\text{kHz}$, and $V_r / V_O \leq 6\,\%$.

Solution. The maximum load current is

$$I_{Omax} = \frac{P_{Omax}}{V_O} = \frac{120}{12} = 10\,\text{A}, \tag{2.244}$$

and the minimum load resistance is

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{10} = 1.2\,\Omega. \tag{2.245}$$

The dc voltage transfer functions are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{12}{32} = 0.375, \tag{2.246}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{12}{28} = 0.4286, \tag{2.247}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{12}{24} = 0.5. \tag{2.248}$$

Let us assume $\eta = 0.9$. The maximum duty cycle at the CCM/DCM boundary at full load $R_{Lmin} = 1.2\,\Omega$ occurs at $V_{Imin} = 24\,\text{V}$,

$$D_{Bmax} = \frac{M_{V\,DCmax}}{\eta} = \frac{V_O}{\eta V_{Imin}} = \frac{12}{0.9 \times 24} = 0.5556, \tag{2.249}$$

resulting in the maximum inductance required for DCM operation,

$$L_{max} = \frac{R_{Lmin}(1 - D_{Bmax})}{2f_s} = \frac{1.2 \times (1 - 0.5556)}{2 \times 100 \times 10^3} = 2.6667\,\mu\text{H}. \tag{2.250}$$

Pick $L = 2.4\,\mu\text{H}$. The maximum duty cycle at $R_{Lmin} = 1.2\,\Omega$, $V_{Imin} = 24\,\text{V}$, and $L = 2.4\,\mu\text{H}$ is

$$D_{max} = \sqrt{\frac{2f_s L M_{V\,DCmax}^2}{\eta R_{Lmin}(1 - M_{V\,DCmax})}} = \sqrt{\frac{2 \times 100 \times 10^3 \times 2.4 \times 10^{-6} \times 0.5^2}{0.9 \times 1.2 \times (1 - 0.5)}} = 0.4714, \tag{2.251}$$

$$D_{1min} = D_{max}\left(\frac{1}{M_{V\,DCmax}} - 1\right) = 0.4714 \times \left(\frac{1}{0.5} - 1\right) = 0.4714, \tag{2.252}$$

and

$$D_{max} + D_{1min} = 0.4714 + 0.4714 = 0.9428 < 1. \tag{2.253}$$

The nominal duty cycle at $R_{Lmin} = 1.2\,\Omega$ and $V_{Inom} = 28\,\text{V}$ is

$$D_{nom} = \sqrt{\frac{2f_s L M_{V\,DCnom}^2}{\eta R_{Lmin}(1 - M_{V\,DCnom})}} = \sqrt{\frac{2 \times 100 \times 10^3 \times 2.4 \times 10^{-6} \times 0.4286^2}{0.9 \times 1.2 \times (1 - 0.4286)}} = 0.378, \tag{2.254}$$

$$D_{1nom} = D_{nom}\left(\frac{1}{M_{V\,DCnom}} - 1\right) = 0.378 \times \left(\frac{1}{0.4286} - 1\right) = 0.5039, \tag{2.255}$$

and

$$D_{nom} + D_{1nom} = 0.3448 + 0.5039 = 0.8487 < 1. \tag{2.256}$$

The minimum duty cycle at $R_{Lmin} = 1.2\,\Omega$ and $V_{Imax} = 32\,\text{V}$ is

$$D_{min} = \sqrt{\frac{2f_s L M_{V\,DCmin}^2}{\eta R_{Lmin}(1 - M_{V\,DCmin})}} = \sqrt{\frac{2 \times 100 \times 10^3 \times 2.4 \times 10^{-6} \times 0.375^2}{0.9 \times 1.2 \times (1 - 0.375)}} = 0.3162, \tag{2.257}$$

$$D_{1max} = D_{min}\left(\frac{1}{M_{V\,DCmin}} - 1\right) = 0.3162 \times \left(\frac{1}{0.375} - 1\right) = 0.527, \tag{2.258}$$

and

$$D_{min} + D_{1max} = 0.3162 + 0.527 = 0.8432 < 1. \tag{2.259}$$

The maximum peak switch, diode, and inductor current occurs at $R_{Lmin} = 1.2\,\Omega$ and $V_{Imax} = 32\,\text{V}$ and is found to be

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{D_{min}(V_{Imax} - V_O)}{f_s L} = \frac{0.3162 \times (32 - 12)}{100 \times 10^3 \times 2.4 \times 10^{-6}} = 26.35\,\text{A}. \tag{2.260}$$

The maximum switch and diode voltage stress is

$$V_{SMmax} = V_{DMmax} = V_{Imax} = 32\,\text{V}. \tag{2.261}$$

Let us choose an IRF150 power MOSFET with $V_{DSS} = 100\,\text{V}$, $I_{SM} = 40\,\text{A}$, $r_{DS} = 0.055\,\Omega$, $C_o = 100\,\text{pF}$, and $Q_g = 63\,\text{nC}$. In addition, we select an MBR4040 Schottky diode with $V_{DM} = 40\,\text{V}$, $I_{DM} = 40\,\text{A}$, $V_F = 0.4\,\text{V}$, and $R_F = 25\,\text{m}\Omega$.

The ripple voltage is

$$V_r = 0.06 V_O = 0.06 \times 12 = 720\,\text{mV}. \tag{2.262}$$

The minimum filter capacitor ESR is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{720}{26.35} = 27.32\,\text{m}\Omega. \tag{2.263}$$

Pick $r_C = 25\,\text{m}\Omega$. The minimum filter capacitance is

$$C_{min} = \frac{1}{2 r_C f_s} = \frac{1}{2 \times 0.025 \times 100 \times 10^3} = 200\,\mu\text{F}. \tag{2.264}$$

Pick $C = 220\,\mu\text{F}/25\,\text{V}/25\,\text{m}\Omega$.

Let us estimate the power losses in various components at $R_{Lmin} = 1.2\,\Omega$ and $V_{Imin} = 24\,\text{V}$. The conduction power loss in the MOSFET is

$$P_{rDS} = \frac{2 r_{DS}}{3} \sqrt{\frac{2 M_{V\,DCmax}^2 (1 - M_{V\,DCmax})}{f_s L R_{Lmin}}} P_{Omax} = \frac{2 \times 0.055}{3} \sqrt{\frac{2 \times 0.5^2 \times (1 - 0.5)}{100 \times 10^3 \times 2.4 \times 10^{-6} \times 1.2}} \times 120 = 4.1\,\text{W}. \tag{2.265}$$

The switching loss is

$$P_{sw} = f_s C_o V_{Imin}^2 = 100 \times 10^3 \times 100 \times 10^{-12} \times 24^2 = 0.006\,\text{W}. \tag{2.266}$$

Hence, the total power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 4.1 + 0.003 = 4.103\,\text{W}. \tag{2.267}$$

The diode conduction loss due to R_F is

$$P_{RF} = \frac{2 R_F}{3} \sqrt{\frac{2(1 - M_{V\,DCmax})^3}{f_s L R_{Lmin}}} P_{Omax} = \frac{2 \times 0.025}{3} \sqrt{\frac{2 \times (1 - 0.5)^3}{100 \times 10^3 \times 2.4 \times 10^{-6} \times 1.2}} \times 120 = 1.864\,\text{W}. \tag{2.268}$$

The power loss in the diode due to V_F is

$$P_{VF} = V_F I_{Omax} (1 - M_{V\,DCmax}) = 0.4 \times 10 \times (1 - 0.5) = 2\,\text{W}. \tag{2.269}$$

Hence, the overall diode conduction loss is

$$P_D = P_{RF} + P_{VF} = 1.864 + 2 = 3.864\,\text{W}. \tag{2.270}$$

Assuming $r_L = 0.05\,\Omega$, the power loss in the inductor ESR is

$$P_{rL} = \frac{2r_L}{3}\sqrt{\frac{2(1 - M_{V\,DCmax})}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.05}{3}\sqrt{\frac{2 \times (1 - 0.5)}{100 \times 10^3 \times 2.4 \times 10^{-6} \times 1.2}} \times 120 = 7.454\,\text{W}. \tag{2.271}$$

The total power loss is

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} = 4.1 + 0.006 + 3.864 + 7.454 = 15.424\,\text{W}, \tag{2.272}$$

resulting in the converter efficiency

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{120}{120 + 15.424} = 88.61\,\%. \tag{2.273}$$

Assuming the gate-to-source peak-to-peak voltage $V_{GSm} = 8\,\text{V}$, the MOSFET gate-drive voltage is

$$P_G = f_s Q_g V_{GSm} = 100 \times 10^3 \times 63 \times 10^{-9} \times 8 = 50.4\,\text{mW}. \tag{2.274}$$

The converter efficiency η can be computed from (2.235) and the duty cycle D from (2.241). Figures 2.23 and 2.24 show plots of the converter efficiency η and the duty cycle D as functions of the dc input voltage V_I at fixed load resistances R_L, respectively. It can be seen that the efficiency η decreases as the input voltage V_I increases. Figures 2.25–2.28 show plots of the converter efficiency η and duty cycle D versus the load current I_O and the load resistance R_L for DCM at fixed values of the dc input voltage V_I. The efficiency decreases with respect to I_O and increases with respect to R_L.

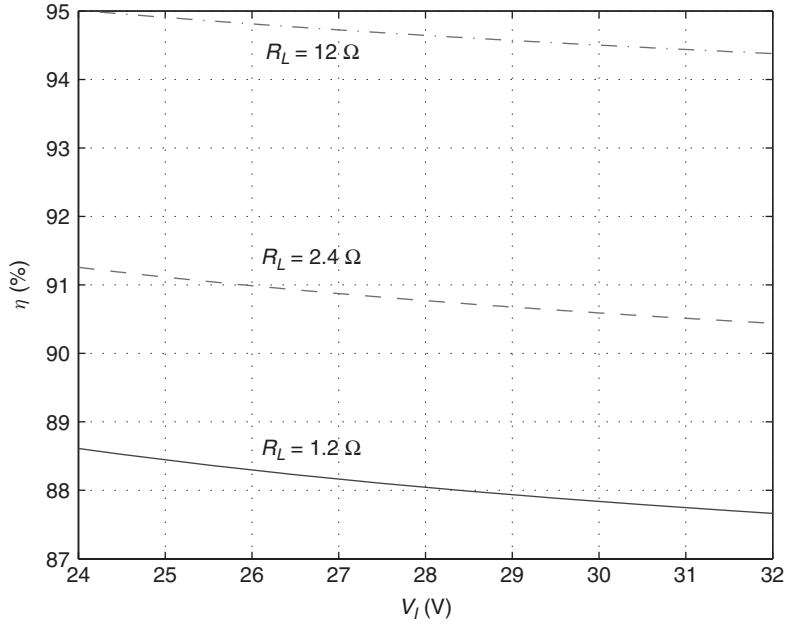


Figure 2.23 Efficiency η as a function of the dc input voltage V_I for the buck converter given in the designed example for DCM at $R_L = 1.2\,\Omega$, $2.4\,\Omega$, and $12\,\Omega$.

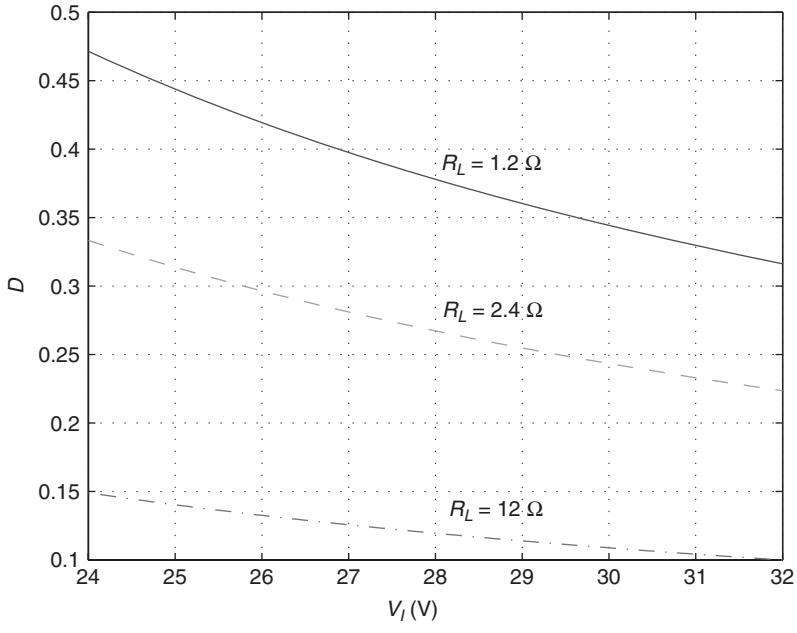


Figure 2.24 Duty cycle D as a function of the dc input voltage V_I for the buck converter given in the designed example for DCM at $R_L = 1.2\,\Omega$, $2.4\,\Omega$, and $12\,\Omega$.

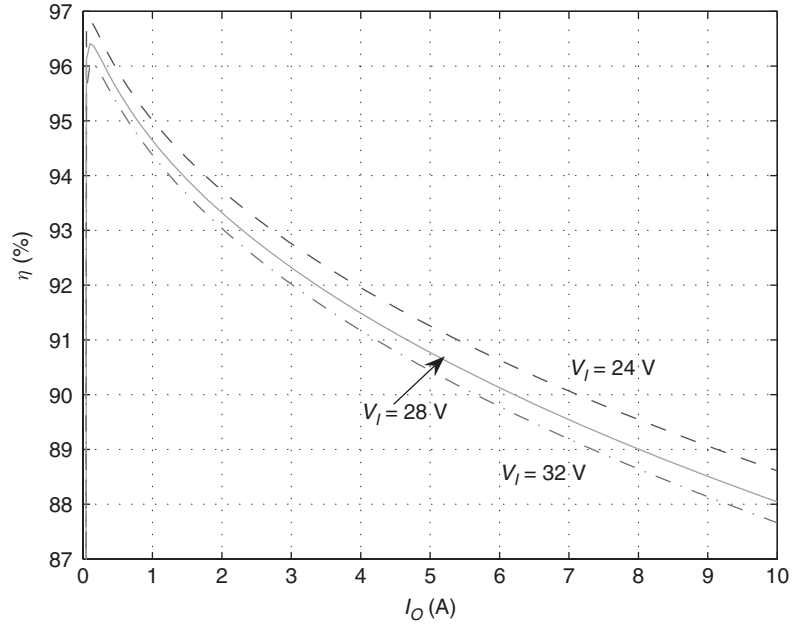


Figure 2.25 Efficiency η of the buck converter as a function of the load current I_O for DCM at $V_I = 24\,\text{V}$, $28\,\text{V}$, and $32\,\text{V}$.

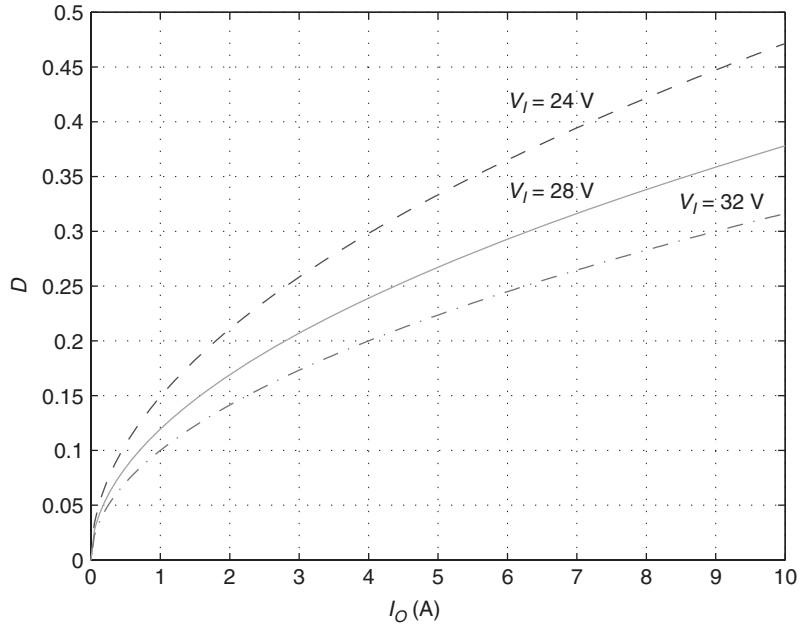


Figure 2.26 Duty cycle D of the buck converter as a function of the load current I_O for DCM at $V_I = 24\,\text{V}$, $28\,\text{V}$, and $32\,\text{V}$.

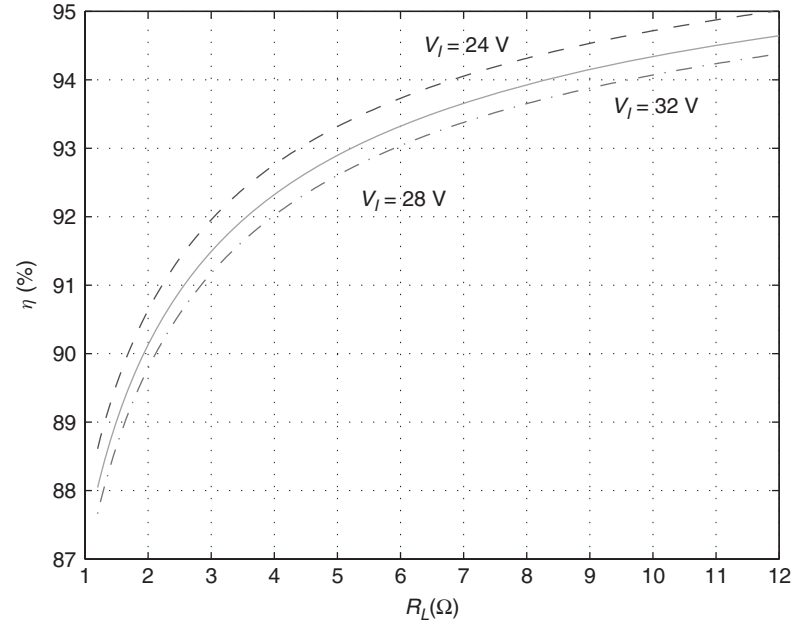


Figure 2.27 Efficiency η of the buck converter as a function of load resistance R_L for DCM at $V_I = 24\,\text{V}$, $28\,\text{V}$, and $32\,\text{V}$.

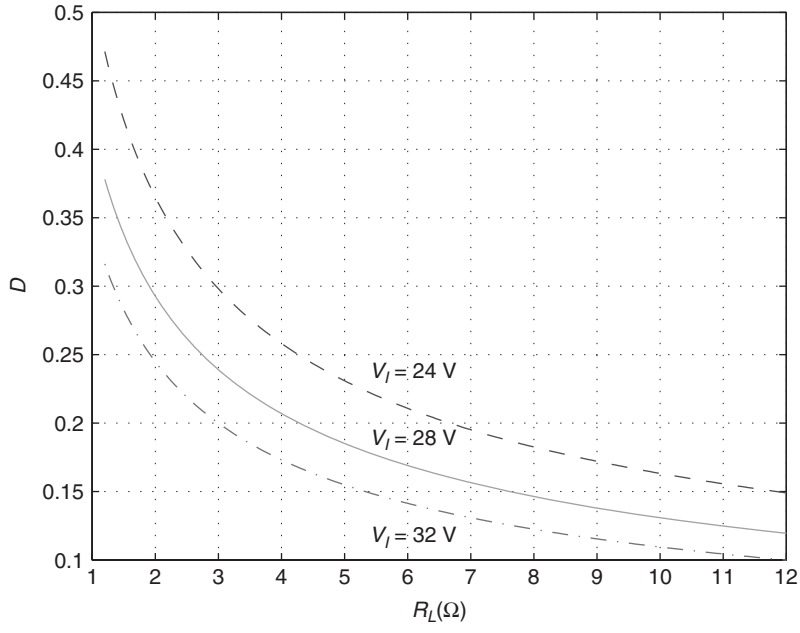


Figure 2.28 Duty cycle D of the buck converter as a function of load resistance R_L for DCM at $V_I = 24\,\text{V}$, $28\,\text{V}$, and $32\,\text{V}$.

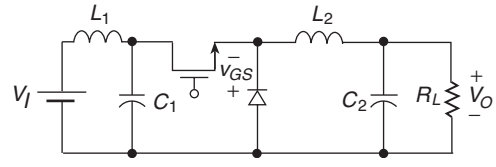


Figure 2.29 Buck converter with an input L_1-C_1 low-pass filter.

2.4 Buck Converter with Input Filter

The disadvantage of the buck converter topology shown in Figure 2.1(a) is its discontinuous, hence pulsating input current waveform because the switch is connected in series with the input voltage source. The input current flows when the switch is closed and is abruptly interrupted when the switch is open. In order to obtain a continuous input current, a second-order L_1-C_1 low-pass filter can be added at the input of the converter, as depicted in Figure 2.29.

2.5 Buck Converter with Synchronous Rectifier

A buck converter topology with a synchronous rectifier is shown in Figure 2.30(a). This circuit is obtained by replacing the diode with an n-channel MOSFET. In general, diodes have an offset voltage V_F and thus their forward voltage is relatively high and may become comparable with the output voltage in low-voltage applications. In contrast, MOSFETs do

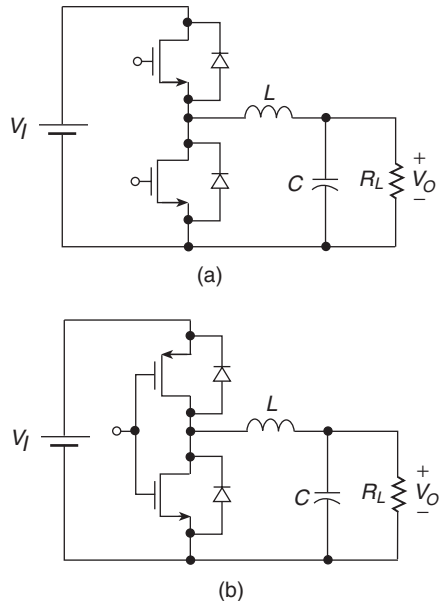


Figure 2.30 Buck converter with a synchronous rectifier. (a) With two n-channel MOSFETs. (b) CMOS buck converter.

not have an offset voltage. If the on-resistance of a MOSFET is low, the forward voltage drop across the MOSFET is very low, reducing the conduction loss and yielding high efficiency. Some low-breakdown voltage MOSFETs have the on-resistance r_{DS} as low as 6 mΩ. In addition, operation in DCM can be avoided because the channel of the transistor can conduct current in both directions. The synchronous buck converter operates in CCM even down to no load. The two MOSFETs are driven in a complementary manner. The low side n-channel MOSFET replacing a Schottky diode operates in the third quadrant because the current normally flows from source to drain. When both transistors are n-channel MOSFETs, it is difficult to drive the upper MOSFET because both the gate and the source are connected to 'hot' points. One solution is to use a transformer with one primary winding and two secondary windings. The primary winding is connected to a driver (e.g., an IC driver). One transformer output is noninverting and the other transformer output is inverting. The synchronous buck converter suffers from a cross-conduction (or shoot-through) effect, resulting in high current spikes in both transistors. This produces high losses and reduces the efficiency. A nonoverlapping driver can produce a dead time and reduce the cross-conduction loss. During the dead time periods, the inductor current flows through the lower MOSFET body diode. This body diode has a very slow reverse recovery characteristic that can adversely affect the converter efficiency. An external Schottky diode can be connected in parallel with the low-side MOSFET to shunt the body diode and to prevent it from affecting the converter performance. The added Schottky diode can have a much lower current rating than the diode in the conventional nonsynchronous buck converter because it only conducts during the short dead time when both MOSFETs are OFF.

If the upper MOSFET is a PMOS and the lower MOSFET is an NMOS, then the circuit is similar to a digital complementary metal oxide semiconductor (CMOS) inverter, as shown in Figure 2.30(b). In this case, both transistors can be driven by the same gate-to-source voltage. The peak-to-peak gate-to-source voltage should be equal or close to the dc input voltage V_I. Therefore, the CMOS buck synchronous converter is a good topology for

applications with a low dc voltage V_I. The whole converter can be integrated, except for the filter capacitor C. At a high voltage V_I, the peak-to-peak gate-to-source voltage is high and may break the MOSFET gate. The same gate-to-drive voltage may cause cross-conduction of both transistors, generating high spikes and drastically reducing the efficiency. A dead time will reduce the current spikes, but this requires two non-overlapping gate-to-source voltages to drive the MOSFETs. The synchronous buck converter is especially attractive in power supplies with a very low output voltage (e.g., $V_O = 3.3\,\text{V}$ or $V_O = 1.8\,\text{V}$) and/or a wide load range, including operation from no load to full load. Its main advantage is higher efficiency than that for the conventional buck converter. The synchronous buck converter may by used as a bidirectional converter.

Figure 2.31 shows a synchronous buck converter with a transformer driver. If both MOSFETs are n-channel devices, then the upper output of the transformer should be noninverting and the other should be inverting. If the upper transistor is a PMOS and the lower transistor is an NMOS, then both transformer outputs should be noninverting or inverting.

Figure 2.32 shows a synchronous buck converter with a voltage mirror driver. The voltage mirror driver acts as a voltage shifter for the ac voltage waveform so that the gate-to-source voltage of the n-channel MOSFET is the same as the source-to-gate voltage of the p-channel MOSFET. Unlike in the CMOS synchronous buck converter, the peak-to-peak voltage of the gate-to-source voltage can be lower than the dc input voltage V_I. Therefore, this driver is good for applications with a high values of V_I.

The minimum inductance is limited only by the inductor current for the converter with a synchronous rectifier. For CCM, the maximum inductor current ripple is

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L_{min}}. \tag{2.275}$$

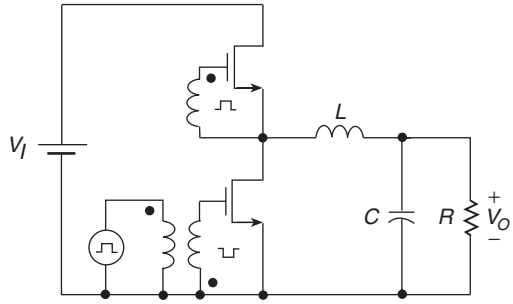


Figure 2.31 Synchronous buck converter with a transformer driver.

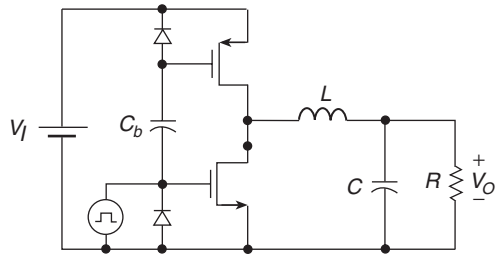


Figure 2.32 Synchronous buck converter with a voltage mirror driver.

Hence, the minimum inductance is given by

$$L_{min} = \frac{V_O(1 - D_{min})}{f_s \Delta i_{Lmax}} = \frac{(1 - D_{min})R_{Lmin}}{f_s \Delta i_{Lmax}/I_{Omax}}. \tag{2.276}$$

The choice between synchronous rectification and Schottky diode rectification is as follows. Synchronous rectifiers should be used for $V_O \leq 2\,\text{V}$, $f_s \leq 300\,\text{kHz}$, and $10\,\text{A} \leq I_O \leq 100\,\text{A}$. Schottky diodes should be used for $V_O > 5\,\text{V}$ and $f_s > 1\,\text{MHz}$, $I_O < 10\,\text{A}$, and $I_O > 100\,\text{A}$.

2.6 Buck Converter with Positive Common Rail

Figure 2.33 shows the derivation of a buck converter topology, in which the positive potential of both the input and output voltages is common and can be connected to ground. The classical buck converter with a negative common rail is depicted in Figure 2.33(a). Figure 2.33(b) shows the converter circuit with the MOSFET and the inductor moved to the common rail of Figure 2.33(a). The resulting positive bus is now the common rail. Figure 2.33(c) shows the circuit of Figure 2.33(b) flipped so that the positive rail is at the bottom.

One of the disadvantages of the buck converter shown in Figure 2.1(a) is the difficulty of driving the transistor because neither the gate nor the source is connected to ground. Figure 2.34 shows a topology of the buck converter, in which the gate is referenced to ground, but the output of the converter is not grounded. This topology may be useful in

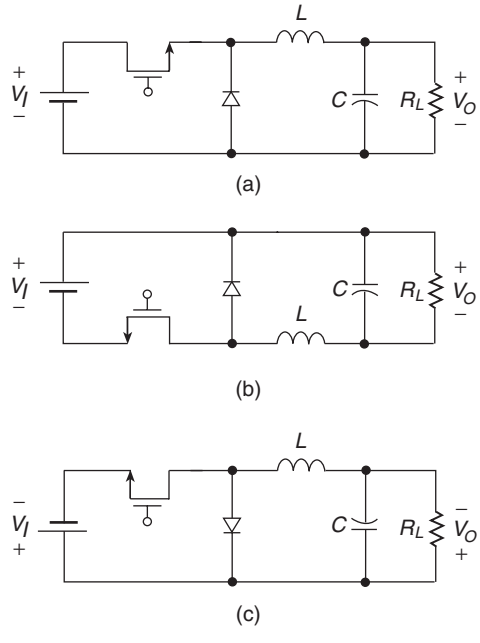


Figure 2.33 Derivation of the buck converter topology with the positive common rail. (a) Classical buck converter with a negative common rail. (b) Buck converter with the MOSFET and the inductor moved to the negative branch, resulting in the positive common rail. (c) Buck converter with a positive common rail.

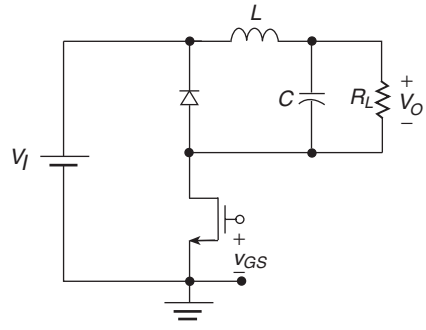


Figure 2.34 Topology of the buck converter with the gate referenced to ground and floating output voltage.

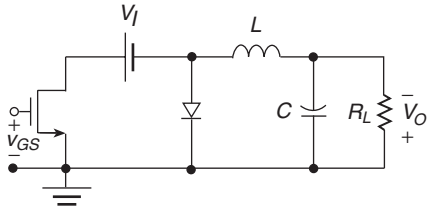


Figure 2.35 Topology of the buck converter in which both the MOSFET source and the converter output are grounded, but which requires a floating power supply.

some preliminary laboratory tests of the converter because a simple driver may be used. It can also be used in applications where the load is not connected to ground – for example, a bulb or an LED with variable brightness.

Figure 2.35 shows a topology of the buck converter, in which both the source of the MOSFET and the output of the converter are connected to ground, but it requires a floating power supply.

In order to increase the range of the conversion ratio, two buck converters can be cascaded. However, this circuit requires twice as many components as a single-stage buck converter, which increases the size, weight, and cost. A quadratic buck converter is shown in Figure 2.36 [23]. The dc voltage transfer function of this converter is

$$M_{V\,DC} = \frac{V_O}{V_I} = \eta D^2. \tag{2.277}$$

The quadratic buck converter contains only one transistor.

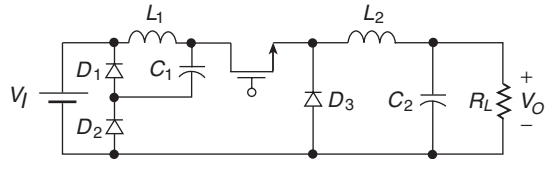


Figure 2.36 Quadratic buck converter.

2.7 Tapped-inductor Buck Converters

The simplest way to extend the range of the dc voltage transfer function $M_{V\,DC}$ is to replace the inductor L with a tapped inductor in the basic dc–dc converters. The turns ratio n of the tapped inductor is present in $M_{V\,DC}$. It permits the duty cycle D to be adjusted to a value at which the efficiency of the converter is high. Very low and very high values of the duty cycle can be avoided. Also, the utilization of the switching devices c_p and passive devices can be improved.

Tapped-inductor buck converters are shown in Figure 2.37. These circuits are high step-down converters. The tapped inductor acts as a transformer and its magnetizing inductance acts as an output filter inductor. A magnetic core with an air gap can be used to build the tapped inductor. The tapped inductor may store magnetic energy.

2.7.1 Tapped-inductor Common-diode Buck Converter

Consider the common-diode tapped-inductor buck converter shown in Figure 2.38(a). The voltage transfer function of the tapped inductor is

$$n = \frac{v}{v_s} = \frac{N_p + N_s}{N_s} = \frac{N_p}{N_s} + 1. \tag{2.278}$$

When the MOSFET is ON and the diode is OFF,

$$V_I - V_O = v = nv_s, \tag{2.279}$$

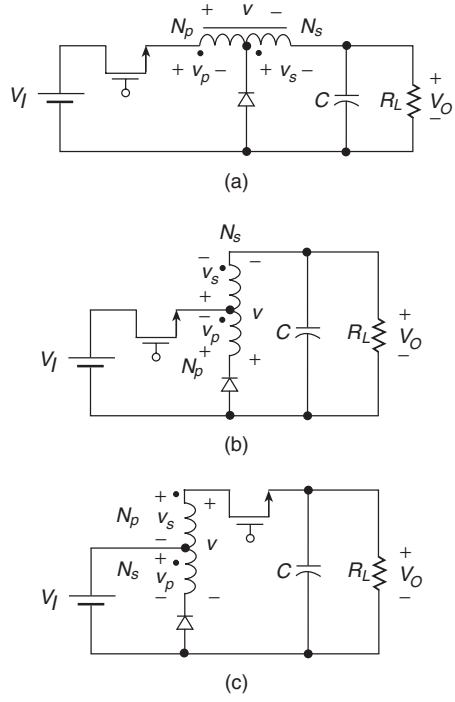


Figure 2.37 Tapped-inductor buck converters. (a) Tapped-inductor common-diode buck converter. (b) Tapped-inductor common-switch buck converter. (c) Watkins–Johnson (common-source) converter.

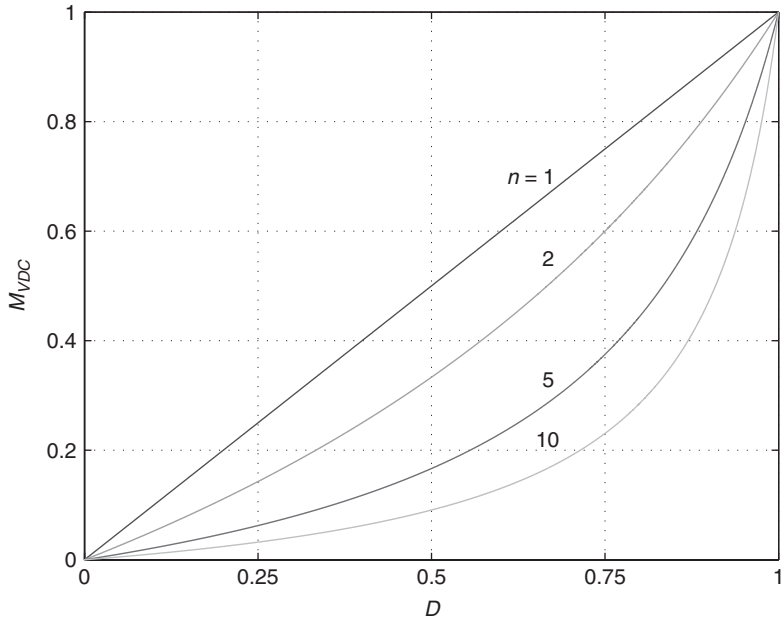


Figure 2.38 DC voltage transfer function of common-diode tapped-inductor buck converter for CCM.

producing the voltage across the N_s winding

$$v_s = \frac{V_I - V_O}{n}. \tag{2.280}$$

When the MOSFET is OFF and the diode is ON,

$$v_s = V_O. \tag{2.281}$$

Using the volt-second balance for the N_s winding, we obtain the dc voltage transfer function for the common-diode converter operating in CCM,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{D + n(1 - D)}. \tag{2.282}$$

The dc voltage transfer function $M_{V\,DC}$ versus D for CCM is illustrated in Figure 2.38. The current and voltage stresses are

$$I_{SM1} = \frac{M_{V\,DC}}{D} I_O = \left(M_{V\,DC} + \frac{1 - M_{V\,DC}}{n} \right) I_O, \tag{2.283}$$

$$V_{SM1} = V_I + (n - 1)V_O = \left(\frac{1}{M_{V\,DC}} + n - 1 \right) V_O, \tag{2.284}$$

$$V_{SM2} = \frac{V_I - V_O}{n} + V_O = \left(1 + \frac{n}{M} - \frac{1}{n} \right) V_O. \tag{2.285}$$

The magnetizing inductance on the terminals of winding N_s is

$$L_m = \left(\frac{L_s}{L_p + L_s} \right)^2 L, \tag{2.286}$$

where $L = L_p + L_s$ is the total inductance of winding.

The circuit has several advantages, such as high voltage conversion ratio, low switch current stress, and low diode voltage stress. The main disadvantage of the tapped-inductor buck converter is the effect of the leakage inductance of winding N_p. When the upper transistor is turned off, the leakage inductance forms a resonant circuit with the drain-to-source capacitance of that transistor, causing ringing. This increases the transistor peak voltage and switching loss. A higher-voltage transistor is required, which will have a higher on-resistance, resulting in a higher conduction loss. MOSFET on-resistance rapidly increases with rated breakdown voltage. An active-clamp technique may be used to reduce the switch peak voltage.

2.7.2 Tapped-inductor Common-transistor Buck Converter

Consider the tapped-inductor common-transistor tapped-inductor buck converter shown in Figure 2.38(b). When the MOSFET is ON and the diode is OFF,

$$v_s = V_I - V_O. \tag{2.287}$$

When the MOSFET is OFF and the diode is ON,

$$v = -V_O = nv_s, \tag{2.288}$$

resulting in

$$v_s = -\frac{V_O}{n}. \tag{2.289}$$

Applying the volt-second balance, we arrive at the dc voltage transfer function for the common-switch converter operating in CCM,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{D + \dfrac{1-D}{n}}. \tag{2.290}$$

Figure 2.39 plots $M_{V\,DC}$ as a function of D for CCM.

2.7.3 Watkins–Johnson Converter

We now analyze the Watkins–Johnson converter, which is a tapped-inductor common-source converter. The converter was named after its inventors, the Watkins–Johnson Company. It has been used to power traveling wave tubes that exhibit a negative input resistance and are used in satellite communications. The circuit has two poles and a single left-hand place zero. When the MOSFET is ON and the diode is OFF,

$$v_s = V_I - V_O = \frac{v}{n}, \tag{2.291}$$

yielding

$$v = n(V_I - V_O). \tag{2.292}$$

When the MOSFET is OFF and the diode is ON,

$$v_p = V_I = v - v_s = v - \frac{v}{n} = v\frac{n-1}{n}, \tag{2.293}$$

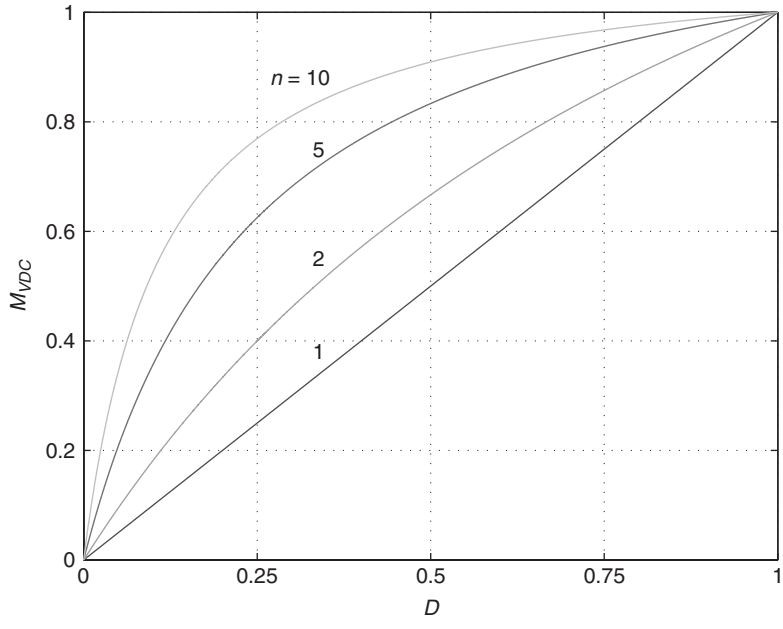


Figure 2.39 DC voltage transfer function of tapped-inductor common-switch buck converter for CCM.

resulting in

$$v = \frac{n}{n-1} V_I. \tag{2.294}$$

Applying the volt-second balance,

$$n(V_I - V_O)DT = \frac{n}{n-1} V_I (1-D)T, \tag{2.295}$$

we get the dc voltage transfer function of the Watkins–Johnson converter for CCM,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{nD-1}{D(n-1)}. \tag{2.296}$$

This function is illustrated in Figure 2.40. A multiple-output Watkins–Johnson converter can be built–for example, with $V_{O1} = 3.3\,\text{V}$ and $V_{O2} = 14\,\text{V}$ [25].

2.8 Multiphase Buck Converter

So far, we have studied a single-phase buck converter. This circuit requires a relatively large capacitor. Microprocessors are supplied by a very low voltage and a very high current (e.g., $V_O = 1.1\,\text{V}$ and $I_O = 100\,\text{A}$). In these applications, there is a stringent requirement on the output voltage tolerance. The output voltage must remain within the required range under dynamic load variations. This imposes restrictions on the values of the filter inductance and the filter capacitance.

In polyphase or multi-phase buck converters, two or more single-phase converters are operated in parallel on the same filter capacitor and load resistance. A two-phase buck converter is shown in Figure 2.41. Current and voltage waveforms are shown in Figure 2.42.

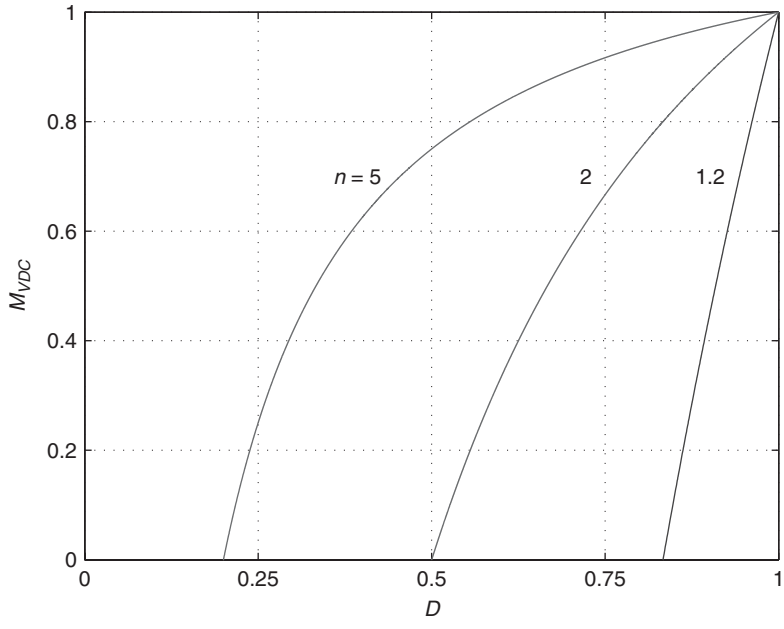


Figure 2.40 DC voltage transfer function of Watkins–Johnson (common-source) tapped-inductor buck converter for CCM.

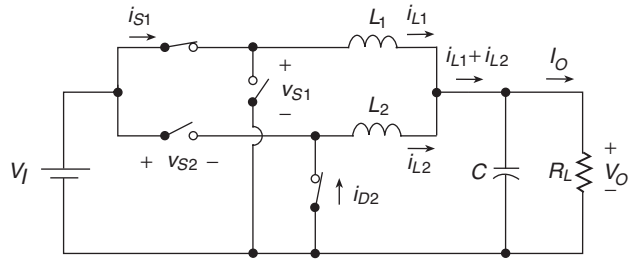


Figure 2.41 Two-phase buck converter.

In two-phase buck converters, the drive signals v_{GS1} and v_{GS2} are shifted by 180°. When the individual phases of the converter are switched complementarity, the output voltage ripple reduces considerably due to ripple cancellation. In a two-phase buck converter, $i_{L1} + i_{L2}$ is constant at $D = 0.5$. Its ac component is zero. Therefore, the ac component of the current through the filter capacitor is zero, resulting in zero ripple voltage. Partial ripple cancellation occurs at $D \neq 0.5$.

If n individual phases are operated in parallel, the frequency of the ripple in the output voltage is n times the switching frequency of each single-phase converter, i.e., $f_r = nf_s$. The ripple cancellation occurs at $D = 1/n$. Due to the reduced magnitude and increased frequency of the output voltage ripple, the filter capacitance required reduces significantly. This improves the transient response of the power supply.

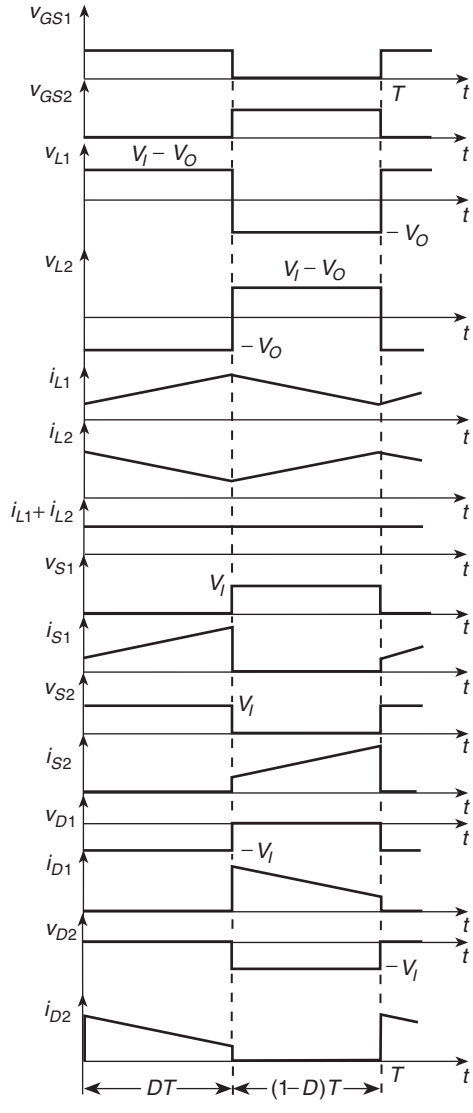


Figure 2.42 Waveforms in two-phase buck converter.

2.9 Summary

- The PWM buck converter is a step-down converter ($V_O < V_I$).
- It is a transformerless converter, which does not provide dc isolation.
- It can operate in two modes: CCM or DCM.
- The dc voltage transfer function of the buck converter is $M_{V\,DC} = V_O/V_I = D$ for CCM if the losses are neglected. It is independent of the load resistance R_L (or the load current

I_O) and depends only on the switch on-duty cycle D. Therefore, the output voltage $V_O = DV_I$ is independent of the load resistance R_L and depends only on the dc input voltage V_I and the duty cycle D.

- The converter has conduction losses and switching losses.
- The duty cycle D of the lossy converter is greater than that of the lossless converter at the same dc voltage transfer function.
- The peak-to-peak value of the inductor ripple current Δi_L is independent of the dc load current for CCM.
- The peak-to-peak value of the current through the filter capacitor C is relatively low and is equal to the peak-to-peak inductor ripple current Δi_L.
- If the capacitance of the filter capacitor is sufficiently high, the output ripple voltage is determined only by the ESR of the filter capacitor and is independent of the capacitance of the filter capacitor.
- The minimum value of the inductor is determined by the CCM/DCM boundary, ripple voltage, or ac losses in the inductor and the filter capacitor.
- A disadvantage of the buck converter is that the input current is pulsating. However, an LC filter can be placed at the converter input to obtain a non-pulsating input current waveform.
- The corner frequency of the output filter, $f_o = 1/(2\pi\sqrt{LC})$, is independent of the load resistance.
- It is relatively difficult to drive the transistor because neither the source nor the gate is referenced to ground. Therefore, a transformer or an optical coupler is required in the driver circuit.
- For CCM, the maximum conduction loss in the transistor occurs at the maximum load current I_{Omax} and at the minimum input voltage V_{Imin} (i.e., at D_{max}).
- For CCM, the maximum conduction loss in the diode occurs at the maximum load current I_{Omax} and at the maximum input voltage V_{Imax} (i.e., at D_{min}).
- The dc voltage transfer function $M_{V\,DC}$ is independent of the inductance L for CCM, whereas $M_{V\,DC}$ depends on L for DCM.
- The minimum efficiency occurs at the full load I_{Omax} (or R_{Lmin}) and at V_{Imin} for the buck converter operating in CCM and DCM.
- The peak currents, rms currents, and conduction losses in the switch, diode, and filter capacitor are higher in DCM than in CCM at the same values of the dc input and output currents and output power. The device current stresses in DCM are higher than those in CCM by a factor of 2 or more.
- The ESR of the inductor in DCM is usually lower than that in CCM because the inductance is lower.
- A filter capacitor with a very low ESR is required for the buck converter to achieve a low ripple voltage.
- The efficiency of the converter in CCM is higher than that in DCM at the same dc input and output currents and the same switching frequency.

- Only one-half of the $B-H$ curve of the inductor core is utilized in the buck converter because the dc current flows through the inductor L.

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2.11 Review Questions

2.1 Define the converter operation in the CCM and DCM.

2.2 Does the buck converter have a transformer version?

2.3 Is the input current of the basic buck converter pulsating?

2.4 How can the buck circuit be modified to obtain a nonpulsating input current?

2.5 Is the transistor driven with respect to ground in the buck converter?

2.6 How is the dc voltage transfer function $M_{V\,DC}$ related to the duty cycle D for the lossless buck converter operated in CCM?

2.7 Is the duty cycle D of the lossy buck converter smaller or greater than that of the lossless converter at a given value of $M_{V\,DC}$ for CCM?

2.8 Does the dc voltage transfer function of the buck converter depend on the load resistance?

2.9 Compare the voltage and current stresses for the transistor and the diode in the buck converter for CCM and DCM.

2.10 Is the corner frequency of the output filter dependent on the load resistance in the buck converter?

2.11 Is the efficiency high at heavy or light loads for the buck converter operated in CCM?

2.12 Are both halves of the B–H curve of the inductor core utilized in the buck converter?

2.12 Problems

2.1 Derive an expression for the dc voltage transfer function of the lossless buck converter operating in CCM using the diode voltage waveform.

2.2 A buck converter has $V_I = 22$ to 32 V, $V_O = 14$ V, $I_O = 0.2$ to 2 A, and $f_s = 40$ kHz. Find the minimum inductance L required to maintain the converter operation in the continuous conduction mode.

2.3 For the converter given in Problem 2.2, find the transistor and diode voltage and current stresses.

2.4 A buck PWM converter has $V_I = 10$ to 14 V, $V_O = 5$ V, $I_O = 0.2$ to 1 A, $f_s = 200$ kHz, $L = 100\,\mu$H, $C = 100\,\mu$F, and $r_C = 20\,\text{m}\Omega$. Find the ripple voltage V_r and $(V_r/V_O) \times 100\,\%$. Also, calculate the ripple voltage across the filter capacitance and the corner frequency of the output filter.

2.5 For the converter given in Problem 2.4, the filter capacitance has been reduced to 47 μF. Find the ripple voltage.

2.6 A PWM converter operates in CCM at $V_I = 10$ V and $V_O = 5$ V. Find the duty cycle D if (a) the converter efficiency $\eta = 100\,\%$ and (b) the converter efficiency $\eta = 80\,\%$.

2.7 A buck converter operating in CCM has a MOSFET whose $r_{DS} = 0.025\,\Omega$. The load current is $I_O = 10$ A. Determine the MOSFET conduction loss at $D = 0.1$ and 0.9.

2.8 A buck converter operating in CCM has a diode whose $R_F = 0.025\,\Omega$ and $V_F = 0.3$ V. The load current is $I_O = 10$ A. Determine the diode conduction loss at $D = 0.1$ and 0.9.

2.9 A power MOSFET has $V_B = 0.75\,\text{V}$, $C_{rss} = 30\,\text{pF}$, and $C_{oss} = 130\,\text{pF}$ at $V_{DS} = 25\,\text{V}$. It is used in a buck PWM converter with $V_I = 400\,\text{V}$ and $f_s = 1\,\text{MHz}$. Find C_{J0}, $C_{ds}(V_I)$, $Q(V_I)$, P_{sw}, $P_{turn\text{-}off}$ and $P_{sw(FET)}$.

2.10 A buck converter has $V_I = 22$ to $32\,\text{V}$, $V_O = 14\,\text{V}$, $I_O = 0$ to $2\,\text{A}$, and $f_s = 40\,\text{kHz}$. Find the maximum inductance L required to maintain the converter operation in the discontinuous conduction mode. Assume $\eta = 90\,\%$.

2.11 Design a buck PWM converter to meet the following specifications: $V_I = 12\,\text{V} \pm 4\,\text{V}$, $V_O = 5\,\text{V}$, $I_O = 1$ to $10\,\text{A}$, $V_r/V_O \leq 1\%$, $f_s = 100\,\text{kHz}$, $r_{L(dc)} = 50\,\text{m}\Omega$, $r_{DS} = 10\,\text{m}\Omega$, $C_o = 200\,\text{pF}$, $V_F = 0.3\,\text{V}$, and $R_F = 20\,\text{m}\Omega$.

2.12 Design a universal buck PWM converter to meet the following specifications: $V_{Imin} = 85\sqrt{2}\,\text{V}$, $V_{Imax} = 264\sqrt{2}\,\text{V}$, $V_O = 48\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, $V_r/V_O \leq 1\%$, $f_s = 200\,\text{kHz}$, $r_L = 1\,\Omega$, $r_{DS} = 1\,\Omega$, $C_o = 100\,\text{pF}$, $V_F = 0.7\,\text{V}$, and $R_F = 25\,\text{m}\Omega$.

2.13 A buck converter has the following specifications: $V_I = 4$ to $6\,\text{V}$, $V_O = 3\,\text{V}$, $I_O = 0$ to $5\,\text{A}$, and $V_r/V_O \leq 2\,\%$. Assume $\eta = 0.9$. Find L, C, and r_C.

2.14 A buck PWM converter has $V_I = 270\,\text{V} \pm 5\,\%$, $V_O = 28\,\text{V}$, $I_O = 0$ to $15\,\text{A}$, $V_r/V_O \leq 5\,\%$, $r_{L(dc)} = 0.05\,\Omega$, $r_C = 0.037\,\Omega$, $r_{DS} = 0.3\,\Omega$, $C_o = 150\,\text{pF}$, $V_F = 0.8\,\text{V}$, $R_F = 17.1\,\text{m}\Omega$, and $f_s = 100\,\text{kHz}$. Find L, C, and r_C. Assume the initial efficiency $\eta = 90\,\%$ at full power.

2.15 A buck PWM converter has $V_I = 5\,\text{V} \pm 20\,\%$, $V_O = 1.8\,\text{V}$, $I_O = 1$ to $10\,\text{A}$, $V_r/V_O \leq 3\,\%$, $r_{L(dc)} = 0.02\,\Omega$, $r_{DS} = 0.01\,\Omega$, $C_o = 150\,\text{pF}$, $V_F = 0.3\,\text{V}$, $R_F = 18\,\text{m}\Omega$, and $f_s = 500\,\text{kHz}$. Find L, C, r_{Cmax}, I_{SMmax}, and V_{SMmax}. Estimate P_{LS} and η at I_{Omax} and V_{Imin}. Assume the initial efficiency $\eta = 80\,\%$ at full power.

2.16 Design a buck converter to meet the following specifications: $V_I = 5 \pm 1\,\text{V}$, $V_O = 3.3\,\text{V}$, $I_O = 0$ to $5\,\text{A}$, $V_r/V_O \leq 1 f_s = 500\,\text{kHz}$, $r_{DS} = 8\,\text{m}\Omega$, $R_F = 20\,\text{m}\Omega$, $V_F = 0.3\,\text{V}$, $r_L = 50\,\text{m}\Omega$, and $Q_g = 50\,\text{nC}$.

3

Boost PWM DC–DC Converter

3.1 Introduction

This chapter is devoted to the PWM boost dc–dc switching-mode converter [1]–[27]. The converter is analyzed for both CCM and DCM. Voltage and current waveforms are derived. The dc voltage transfer function is determined. The voltage and current stresses of the converter components are given. Expressions for the inductance and the capacitance are derived. Power losses are estimated. Design examples are given.

3.2 DC Analysis of PWM Boost Converter for CCM

3.2.1 Circuit Description

The circuit of the PWM boost dc–dc converter [1]–[27] is shown in Figure 3.1(a). Its output voltage V_O is always higher than the input voltage V_I for steady-state operation. It 'boosts' the voltage to a higher level. The converter consists of an inductor L, a power MOSFET, a diode D_1, a filter capacitor C, and a load resistor R_L. The switch S is turned on and off at the switching frequency $f_s = 1/T$ with the ON duty ratio $D = t_{on}/T$, where t_{on} is the time interval when the switch S is ON.

The boost converter can operate in either continuous or discontinuous conduction mode, depending on the waveform of the inductor current. The boost converter in DCM cannot operate at $R_L = \infty$ because the filter capacitor has no path to discharge. The CCM will be considered first. Figure 3.1(b)–(c) shows equivalent circuits of the boost converter for CCM when the switch S is ON and the diode is OFF, and when the switch is OFF and the diode is ON, respectively. Idealized waveforms of the currents and voltages that explain

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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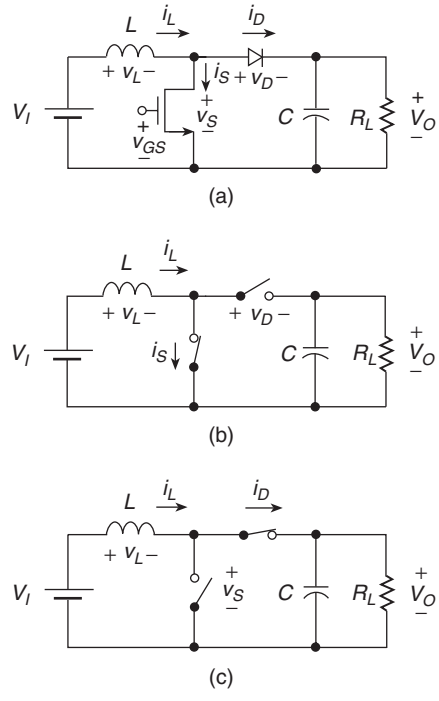


Figure 3.1 PWM boost converter and its ideal equivalent circuits for CCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON.

the principle of operation of the converter are depicted in Figure 3.2. For the time interval $0 < t \leq DT$, the switch is ON. Therefore, the voltage across the diode is $v_D = -V_O$, causing the diode to be reverse biased. The voltage across the inductor is $v_L = V_I$. As a result, the inductor current increases linearly with a slope of V_I/L. Consequently, the magnetic energy also increases. The switch current is equal to the inductor current. At $t = DT$, the switch is turned off by the gate-to-source voltage. The inductor acts as a current source and turns the diode on. The voltage across the inductor is $v_L = V_I - V_O < 0$. Hence, the inductor current decreases with a slope of $(V_I - V_O)/L$. The diode current equals the inductor current. During this time interval, the energy is transferred from the inductor L to the filter capacitor C and the load resistance R_L. At time $t = T$, the switch is turned on again, terminating the cycle.

The boost converter has poor ability to prevent hazardous transients and failures. If a high positive voltage surge appears at the converter input, the input voltage exceeds the output voltage and the diode D_1 is ON for many cycles due to cycle skip. This generates a large current spike through the diode, which may destroy the diode. A similar problem exists at the initial turn-on of the converter when the input voltage is high and the output voltage is initially zero and while the output voltage is lower than the input voltage until steady-state conditions are approached. One way to protect the converter is to add a diode whose anode is connected to the input source V_I and whose cathode is connected to the output filter capacitor C. When the output voltage is lower than the input voltage, the additional diode and the filter capacitor form a peak rectifier, and the energy flows from the input to the output of the converter through the additional diode. When the output voltage becomes higher than the input voltage, the additional diode is reverse biased and turns off, and the boost converter begins normal operation.

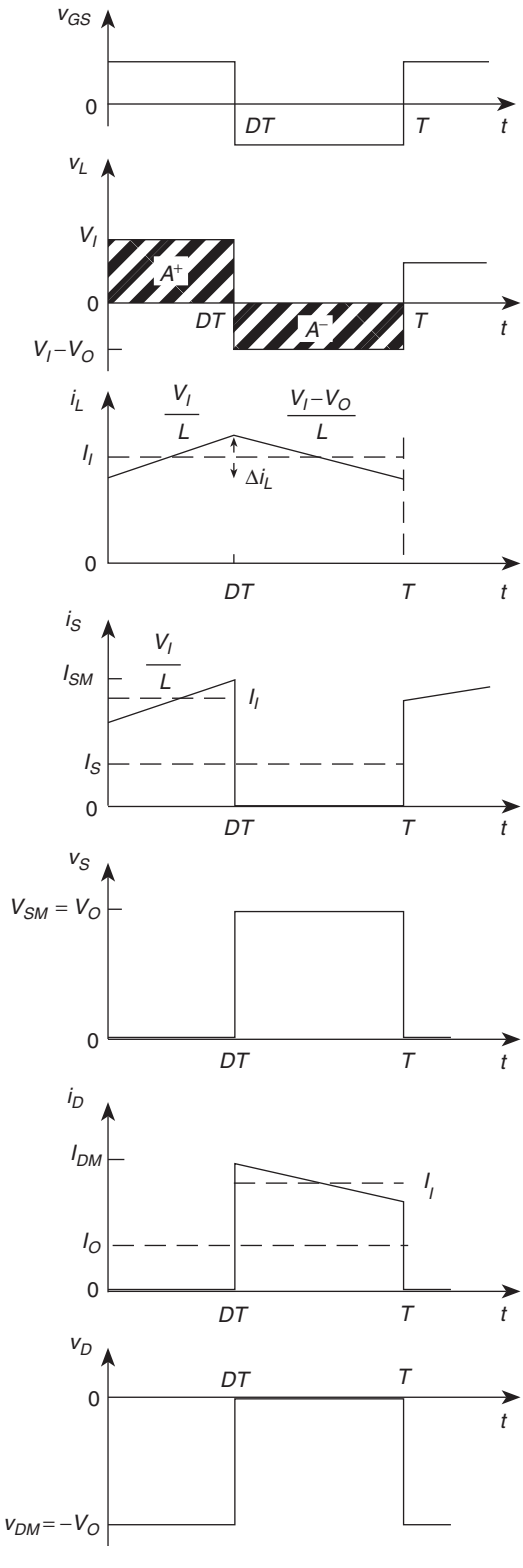


Figure 3.2 Idealized current and voltage waveforms in the PWM boost converter for CCM.

The output power level of the boost converter is usually between 20 and 400 W. This converter is commonly used as an active power factor corrector.

3.2.2 Assumptions

The analysis of the boost PWM converter of Figure 3.1(a) begins with the following assumptions:

1. The power MOSFET and the diode are ideal switches.
2. The transistor output capacitance, the diode capacitance, and lead inductances (and thus switching losses) are zero.
3. Passive components are linear, time-invariant, and frequency-independent.
4. The output impedance of the input voltage source V_I is zero for both dc and ac components.

3.2.3 Time Interval $0 < t \leq DT$

The switch S is ON and the diode is OFF during the time interval $0 < t \leq DT$. An ideal equivalent circuit for this time interval is shown in Figure 3.1(b). When the switch is ON, the voltage across the diode v_D is approximately equal to $-V_O$ and therefore the diode is reverse biased. The voltage across the switch v_S and the diode current are zero. The voltage across the inductor L is

$$v_L = V_I = L\frac{di_L}{dt}, \tag{3.1}$$

and the inductor current i_L and the switch current i_S are

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\,dt + i_L(0) = \frac{1}{L}\int_0^t V_I\,dt + i_L(0) = \frac{V_I}{L}t + i_L(0), \tag{3.2}$$

where $i_L(0)$ is the initial inductor current at time $t = 0$. From (3.2), the peak inductor current is given by

$$i_L(DT) = \frac{V_I DT}{L} + i_L(0). \tag{3.3}$$

It will shortly be shown that the dc voltage transfer function is $M_{V\,DC} = V_O/V_I = I_I/I_O = 1/(1-D)$. Hence, the peak-to-peak value of the inductor ripple current is expressed as

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_I DT}{L} = \frac{V_I D}{f_s L} = \frac{V_O D}{M_{V\,DC} f_s L} = \frac{V_O D(1-D)}{f_s L}. \tag{3.4}$$

For fixed values of V_O, f_s, and L,

$$\frac{d\,\Delta i_L}{dD} = \frac{V_O}{f_s L}(1-2D). \tag{3.5}$$

Setting this derivative to zero, one can show that the maximum value of Δi_L occurs at $D = 0.5$ and is given by

$$\Delta i_{Lmax} = \frac{V_O}{4 f_s L}. \tag{3.6}$$

As the duty cycle D is increased from 0 to 1, the peak-to-peak inductor ripple current Δi_L increases from zero, reaches its maximum at $D = 0.5$, and then decreases to zero.

The diode voltage is

$$v_D = -V_O. \tag{3.7}$$

The average value of the inductor current I_L is equal to the dc input current I_I. Hence, one arrives at the peak value of the switch current

$$I_{SM} = I_I + \frac{\Delta i_L}{2} = \frac{I_O}{1-D} + \frac{\Delta i_L}{2}. \tag{3.8}$$

This time interval is terminated at $t = DT$ when the switch is turned off by the driver. The inductor current i_L flows continuously for CCM. Since $i_L(DT)$ is nonzero when the switch is turned off, it acts almost as a current source and turns the diode on.

The increase in the inductor magnetic energy is

$$\Delta W_{L(in)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(0)]. \tag{3.9}$$

3.2.4 Time Interval DT < t ≤ T

During the time interval $DT < t \leq T$, the switch is OFF and the diode is ON. Figure 3.1(c) shows an ideal equivalent circuit of the lossless converter for this time interval. The switch current i_S and the diode voltage v_D are zero. The inductor discharges during this time interval. The voltage across the inductor L is

$$v_L = V_I - V_O = L\frac{di_L}{dt} < 0, \tag{3.10}$$

which indicates that $V_O > V_I$. The current through the inductor and the diode can be found to be

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t}(V_I - V_O)\,dt + i_L(DT) \\ &= \frac{V_I - V_O}{L}(t - DT) + i_L(DT), \end{aligned} \tag{3.11}$$

where $i_L(DT)$ is the initial inductor current i_L at $t = DT$. The peak-to-peak value of the inductor ripple current is

$$\Delta i_L = i_L(DT) - i_L(T) = \frac{(V_O - V_I)(1-D)T}{L} = \frac{V_O D(1-D)}{f_s L}, \tag{3.12}$$

where $V_I = V_O(1 - D)$.

The voltage across the switch S is given by

$$v_S = V_O = V_{SM}. \tag{3.13}$$

The peak diode current and the peak switch current are given by

$$I_{DM} = I_{SM} = I_I + \frac{\Delta i_L}{2} = \frac{I_O}{1-D} + \frac{\Delta i_L}{2}. \tag{3.14}$$

For the worst case, this expression becomes

$$I_{DMmax} = I_{SMmax} = I_{Imax} + \frac{\Delta i_{Lmax}}{2} = \frac{I_{Omax}}{1-D_{max}} + \frac{\Delta i_{Lmax}}{2}. \tag{3.15}$$

This time interval ends at $t = T$ when the switch is turned on by the driver.

The decrease in the magnetic energy stored in the inductor L during the time interval $DT < t \leq T$ is

$$\Delta W_{L(out)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(T)]. \tag{3.16}$$

In the steady state, the increase in the magnetic energy stored in the inductor during the time interval $0 < t \leq DT$ is equal to the decrease in the magnetic energy stored in the inductor during the time interval $DT < t \leq T$.

3.2.5 DC Voltage Transfer Function for CCM

The average value of the voltage across the inductor in the steady state is

$$V_{L(AV)} = \frac{1}{T}\int_0^T v_L\, dt = 0. \tag{3.17}$$

Referring to Figure 3.2,

$$V_I DT = (V_O - V_I)(1 - D)T, \tag{3.18}$$

which gives

$$V_O = \frac{V_I}{1 - D} \tag{3.19}$$

and results in the dc voltage transfer function for the lossless converter,

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1 - D}. \tag{3.20}$$

The range of $M_{V\,DC}$ for the lossless converter is

$$1 \leq M_{V\,DC} \leq \infty. \tag{3.21}$$

It will shortly be shown that the maximum value of $M_{V\,DC}$ is limited by losses. Rearrangement of (3.20) gives

$$D = 1 - \frac{1}{M_{V\,DC}} = \frac{M_{V\,DC} - 1}{M_{V\,DC}}. \tag{3.22}$$

The sensitivity of V_O with respect to D is

$$S \equiv \frac{dV_O}{dD} = \frac{V_I}{(1 - D)^2}. \tag{3.23}$$

The dc current transfer function is

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = 1 - D. \tag{3.24}$$

As D is increased from 0 to 1, $M_{I\,DC}$ decreases from 1 to 0. Using (3.20) and (3.24), the output-power capability of the boost converter is

$$c_p \equiv \frac{P_O}{V_{SM}I_{SM}} = \frac{V_O I_O}{V_{SM}I_{SM}} = \frac{I_O}{I_{SM}} \approx \frac{I_O}{I_I} = 1 - D. \tag{3.25}$$

As D is increased from 0 to 1, c_p decreases from 1 to 0.

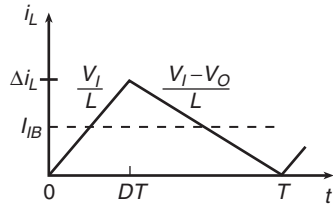


Figure 3.3 Waveform of the inductor current at the CCM/DCM boundary for the boost converter.

3.2.6 Boundary between CCM and DCM

Figure 3.3 shows the inductor current waveform at the boundary between the CCM and the DCM. This waveform is given by

$$i_L = \frac{V_I}{L}t, \qquad \text{for } 0 < t \le DT, \tag{3.26}$$

from which

$$\Delta i_L = i_L(DT) = \frac{V_I DT}{L} = \frac{V_O D}{f_s L M_{V\,DC}} = \frac{V_O D(1-D)}{f_s L}. \tag{3.27}$$

The dc input current at the CCM/DCM boundary is

$$I_{IB} = \frac{\Delta i_L}{2} = \frac{V_O D(1-D)}{2f_s L} \tag{3.28}$$

whose maximum value occurs at $D = 0.5$. From (3.20) and (3.28), the dc output current at the CCM/DCM boundary is

$$I_{OB} = I_{IB}(1-D) = \frac{V_O D(1-D)^2}{2f_s L} = \frac{V_O(M_{V\,DC}-1)}{2f_s L M_{V\,DC}^3} \tag{3.29}$$

and the load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{D(1-D)^2} = \frac{2f_s L M_{V\,DC}^3}{M_{V\,DC}-1}. \tag{3.30}$$

Figures 3.4 and 3.5 show the plots of $I_{OB}/(V_O/2f_sL) = D(1-D)^2$ and $R_{LB}/(2f_sL) = 1/[D(1-D)^2]$ as functions of D. To find the maximum value of I_{OB}, its derivative can be found to be

$$\frac{dI_{OB}}{dD} = \frac{V_O}{2f_s L}(1 - 4D + 3D^2) = 0. \tag{3.31}$$

Thus, the maximum value of I_{OB} occurs at

$$D_m = \tfrac{1}{3}, \tag{3.32}$$

which corresponds to $M_{V\,DC} = 1.5$. Substitution of (3.32) into (3.29) gives the maximum value of the load current at the boundary,

$$I_{OBmax} = \frac{2}{27}\,\frac{V_O}{f_s L_{min}}, \tag{3.33}$$

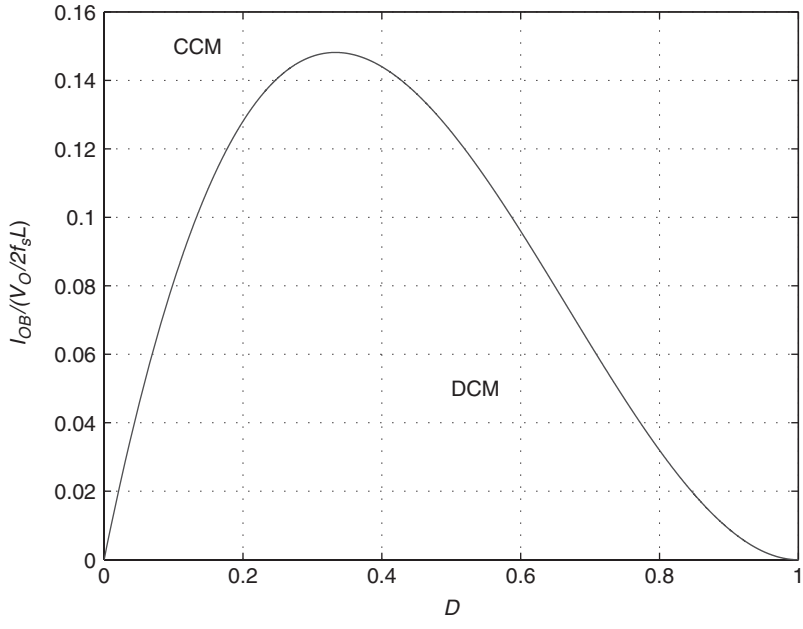


Figure 3.4 Normalized load current $I_{OB}/(V_O/2f_sL)$ at the CCM/DCM boundary as a function of D for boost converter.

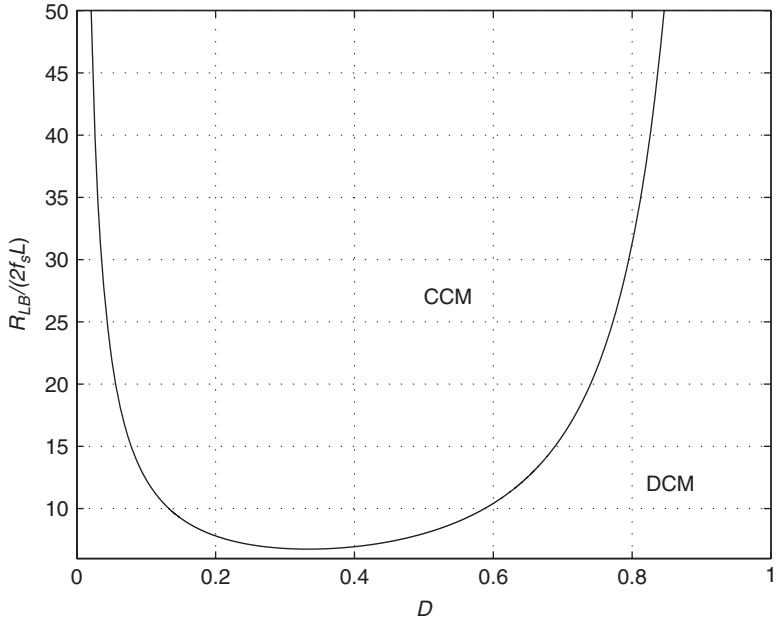


Figure 3.5 Normalized load resistance $R_{LB}/(2f_sL)$ at the CCM/DCM boundary as a function of D for boost converter.

and the minimum value of the load resistance at the boundary,

$$R_{LBmin} = \frac{V_O}{I_{OBmax}} = 13.5 f_s L_{min}. \tag{3.34}$$

Hence, using $I_{OBmax} = I_{Omin} = V_O / R_{Lmax}$, one arrives at the minimum value of the inductance L which ensures the operation in CCM at any value of D,

$$L_{min} = \frac{2}{27} \frac{V_O}{f_s I_{OBmax}} = \frac{2}{27} \frac{R_{Lmax}}{f_s}. \tag{3.35}$$

If $D_{max} < 1/3$ or $D_{min} > 1/3$, a less conservative approach can be taken. Using (3.29), the following expressions can be derived

$$I_{OBmax} = \begin{cases} \dfrac{V_O D_{max}(1 - D_{max})^2}{2 f_s L_{min}}, & \text{for } D < \dfrac{1}{3}, \\ \dfrac{V_O D_{min}(1 - D_{min})^2}{2 f_s L_{min}}, & \text{for } D \geq \dfrac{1}{3}, \end{cases} \tag{3.36}$$

and

$$L_{min} = \begin{cases} \dfrac{R_{Lmax} D_{max}(1 - D_{max})^2}{2 f_s}, & \text{for } D < \dfrac{1}{3}, \\ \dfrac{R_{Lmax} D_{min}(1 - D_{min})^2}{2 f_s}, & \text{for } D \geq \dfrac{1}{3}. \end{cases} \tag{3.37}$$

3.2.7 Ripple Voltage in Boost Converter for CCM

The output part of the boost converter is shown in Figure 3.6. The filter capacitor in this figure is modeled by its capacitance C and its equivalent series resistance r_C. Figure 3.7 shows current and voltage waveforms in the converter output circuit. The dc component of the diode current flows through the load resistor R_L. The ac component of the diode current is divided between the capacitor branch and the load resistance branch. In practice, the filter capacitor is designed in such a way that the impedance of the capacitor branch is much less than the load resistance R_L. Consequently, the current through the capacitor is approximately equal to the ac component of the diode current.

The maximum peak-to-peak value of the capacitor current is

$$I_{Cpp} = I_{DMmax} \approx I_{Imax} = \frac{I_{Omax}}{1 - D_{max}}, \tag{3.38}$$

resulting in the peak-to-peak value of the voltage across r_C,

$$V_{rcpp} = r_C I_{Cpp} = r_C I_{DMmax} \approx \frac{r_C I_{Omax}}{1 - D_{max}}. \tag{3.39}$$

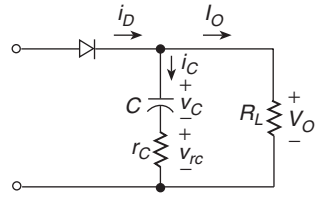


Figure 3.6 Equivalent circuit of the output part of the boost converter.

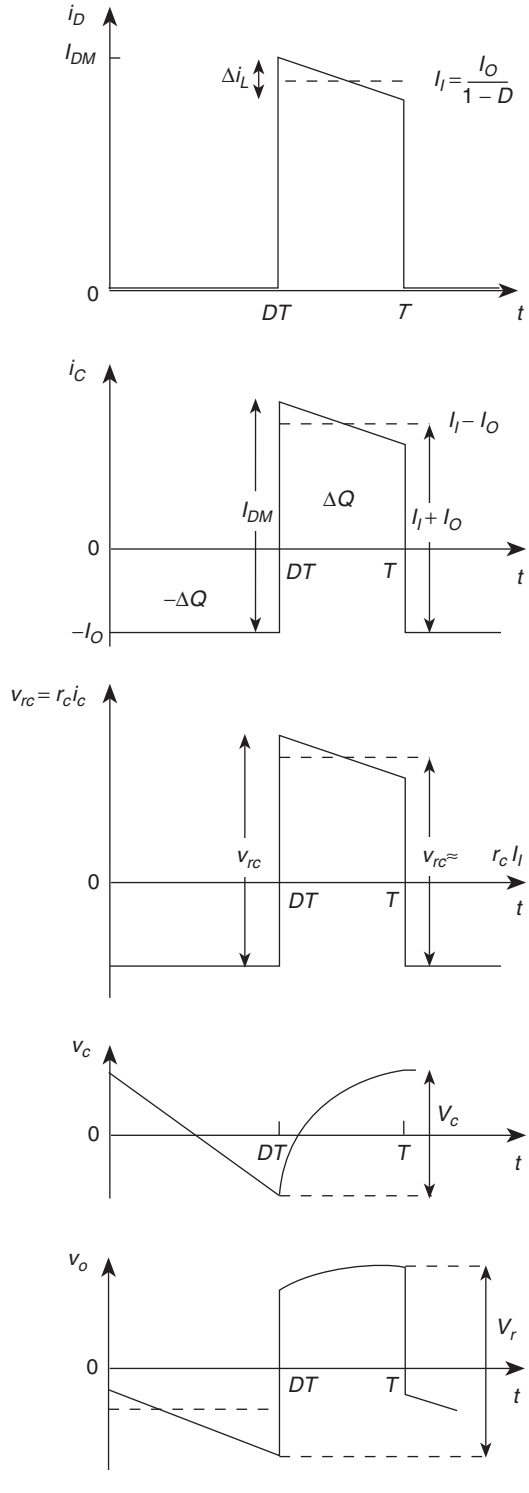


Figure 3.7 Waveforms illustrating the ripple voltage in the PWM boost converter.

The peak-to-peak value of the output ripple voltage V_r is usually specified. Hence, the maximum peak-to-peak value of the ac component of the voltage across the capacitance C is found to be

$$V_{Cpp} \approx V_r - V_{rcpp}. \tag{3.40}$$

On the other hand, this voltage is approximately given by

$$V_{Cpp} = \frac{\Delta Q_{max}}{C_{min}} = \frac{I_{Omax} D_{max} T}{C_{min}} = \frac{V_O D_{max}}{f_s R_{Lmin} C_{min}}, \tag{3.41}$$

where ΔQ_{max} is the charge decrease during the time interval from zero to DT. Rearrangement of (3.41) gives the minimum filter capacitance

$$C_{min} = \frac{I_{Omax} D_{max}}{f_s V_{Cpp}} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}}. \tag{3.42}$$

3.2.8 Power Losses and Efficiency of Boost Converter for CCM

An equivalent circuit of the boost converter with parasitic resistances is shown in Figure 3.8, where r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The conduction losses will be evaluated assuming that the inductor current i_L is ripple-free and equals the dc input current I_I. Hence, the switch current can be approximated by

$$i_S = \begin{cases} I_I = \dfrac{I_O}{1-D}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{3.43}$$

resulting in its rms value

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_0^{DT} dt} = \frac{I_O\sqrt{D}}{1-D} \tag{3.44}$$

and the MOSFET conduction loss

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} I_O^2}{(1-D)^2} = \frac{D r_{DS} P_O}{(1-D)^2 R_L}. \tag{3.45}$$

Note that the transistor conduction loss increases rapidly with increasing duty cycle D at a fixed load current I_O.

Assuming that the transistor output capacitance C_o is linear, the switching loss is expressed by

$$P_{sw} = f_s C_o V_{SM}^2 = f_s C_o V_O^2 = f_s C_o R_L P_O. \tag{3.46}$$

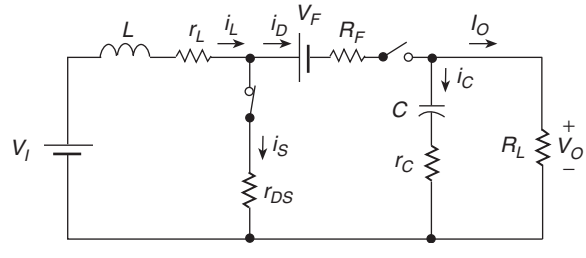


Figure 3.8 Equivalent circuit of the boost converter with parasitic resistances and the diode offset voltage.

Hence, one obtains the total power dissipation in the MOSFET (excluding the drive power)

$$P_{FET} = P_{rDS} + \frac{1}{2}P_{sw} = \frac{Dr_{DS}I_O^2}{(1-D)^2} + \frac{1}{2}f_s C_o V_O^2 = \left[\frac{Dr_{DS}}{(1-D)^2 R_L} + \frac{1}{2}f_s C_o R_L\right] P_O. \quad (3.47)$$

Likewise, the diode current can be approximated by

$$i_D = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ I_I = \dfrac{I_O}{1-D}, & \text{for } DT < t \le T, \end{cases} \quad (3.48)$$

yielding its rms value

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_{DT}^T dt} = \frac{I_O}{\sqrt{1-D}} \quad (3.49)$$

and the power loss in R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F I_O^2}{1-D} = \frac{R_F P_O}{(1-D)R_L}. \quad (3.50)$$

The diode power loss due to R_F increases rapidly with increasing duty cycle D at fixed load current I_O.

The average value of the diode current is

$$I_D = \frac{1}{T}\int_0^T i_D\, dt = \frac{I_O}{T(1-D)}\int_{DT}^T dt = I_O, \quad (3.51)$$

which gives the power loss associated with the voltage V_F,

$$P_{VF} = V_F I_D = V_F I_O = \frac{V_F P_O}{V_O}. \quad (3.52)$$

Thus, the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = V_F I_O + \frac{R_F I_O^2}{1-D} = \left[\frac{V_F}{V_O} + \frac{R_F}{(1-D)R_L}\right] P_O. \quad (3.53)$$

The inductor current is

$$i_L \approx I_I = \frac{I_O}{1-D}, \quad (3.54)$$

leading to its rms value

$$I_{Lrms} = I_I = \frac{I_O}{1-D} \quad (3.55)$$

and the inductor loss

$$P_{rL} = r_L I_{Lrms}^2 = \frac{r_L I_O^2}{(1-D)^2} = \frac{r_L P_O}{(1-D)^2 R_L}. \quad (3.56)$$

The inductor loss increases rapidly with increasing duty cycle D at fixed load current I_O.

The current through the capacitor C is approximately given by

$$i_C = \begin{cases} -I_O, & \text{for } 0 < t \le DT, \\ I_I - I_O = \dfrac{DI_O}{1-D}, & \text{for } DT < t \le T. \end{cases} \quad (3.57)$$

Hence, one obtains the rms current through the filter capacitor

$$I_{Crms} = \sqrt{\frac{1}{T}\int_0^T i_C^2\, dt} = I_O\sqrt{\frac{D}{1-D}} \quad (3.58)$$

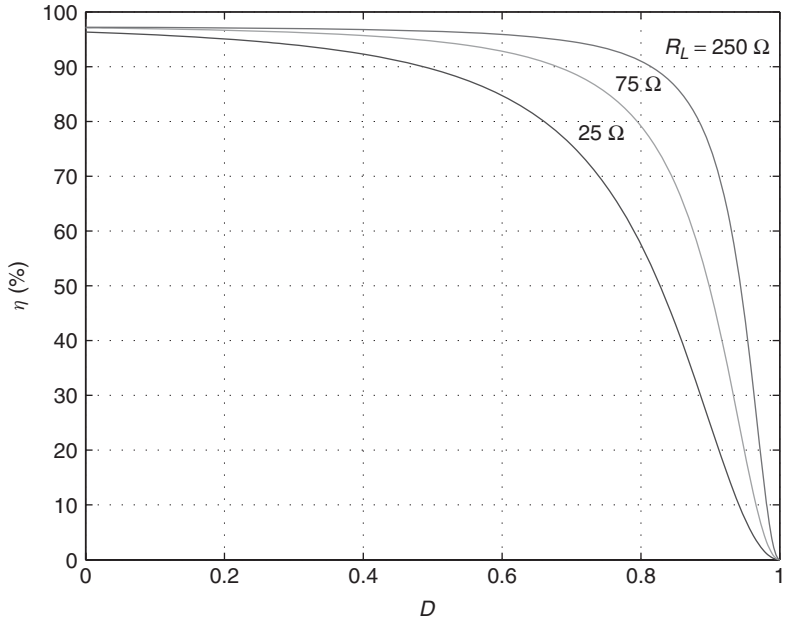


Figure 3.9 Efficiency of the boost converter η versus D for $V_O = 28\,\text{V}$, $r_{DS} = 0.5\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 25\,\text{m}\Omega$, $r_L = 0.3\,\Omega$, $r_C = 40\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$.

and the power loss in the filter capacitor

$$P_{rC} = r_C I_{Crms}^2 = \frac{Dr_C I_O^2}{1-D} = \frac{Dr_C P_O}{(1-D)R_L}. \tag{3.59}$$

The overall power loss of the boost converter is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} \\ &= \left[\frac{r_L + Dr_{DS}}{(1-D)^2 R_L} + \frac{R_F + Dr_C}{(1-D)R_L} + \frac{V_F}{V_O} + f_s C_o R_L\right] P_O, \end{aligned} \tag{3.60}$$

yielding the converter efficiency

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} = \frac{1}{1 + \dfrac{r_L + Dr_{DS}}{(1-D)^2 R_L} + \dfrac{R_F + Dr_C}{(1-D)R_L} + \dfrac{V_F}{V_O} + f_s C_o R_L}. \tag{3.61}$$

Figure 3.9 shows the efficiency of the boost converter η as a function of the duty cycle D for $V_O = 28\,\text{V}$, $r_{DS} = 0.5\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 25\,\text{m}\Omega$, $r_L = 0.3\,\Omega$, $r_C = 40\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$. It can be seen that the efficiency η decreases with increasing D and is higher for higher load resistances R_L.

3.2.9 DC Voltage Transfer Function of Lossy Boost Converter for CCM

The dc component of the output current is

$$I_O = \frac{1}{T}\int_0^T i_D\,dt = \frac{1}{T}\int_{DT}^T I_I\,dt = (1-D)I_I, \tag{3.62}$$

leading to the dc current transfer function of the boost converter

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = 1 - D. \tag{3.63}$$

This equation holds true for both lossless and lossy converters. The efficiency of the converter can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = M_{V\,DC}(1 - D), \tag{3.64}$$

from which the voltage transfer function of the lossy boost converter is

$$M_{V\,DC} = \frac{\eta}{1 - D} = \frac{1}{(1 - D)\left[1 + \dfrac{r_L + Dr_{DS}}{(1 - D)^2 R_L} + \dfrac{R_F + Dr_C}{(1 - D)R_L} + \dfrac{V_F}{V_O} + f_s C_o R_L\right]}. \tag{3.65}$$

Figure 3.10 depicts $M_{V\,DC}$ as a function of D. The duty cycle of the lossy boost converter is

$$D = 1 - \frac{\eta}{M_{V\,DC}} = 1 - \frac{\eta V_I}{V_O}. \tag{3.66}$$

Thus, the duty cycle D increases as the efficiency decreases at a fixed value of $M_{V\,DC}$.

Substitution of (3.66) into (3.61) yields the converter efficiency

$$\eta = \frac{N_\eta}{D_\eta}, \tag{3.67}$$

where

$$N_\eta = R_L - M_{V\,DC}(R_F + r_C - r_{DS}) + \Bigg\{[M_{V\,DC}(R_F + r_C - r_{DS}) - R_L]^2 - 4M_{V\,DC}^2 R_L(r_L + r_{DS})\left(1 + \frac{V_F}{V_O} - \frac{r_C}{R_L} + f_s C_o R_L\right)\Bigg\}^{\frac{1}{2}} \tag{3.68}$$

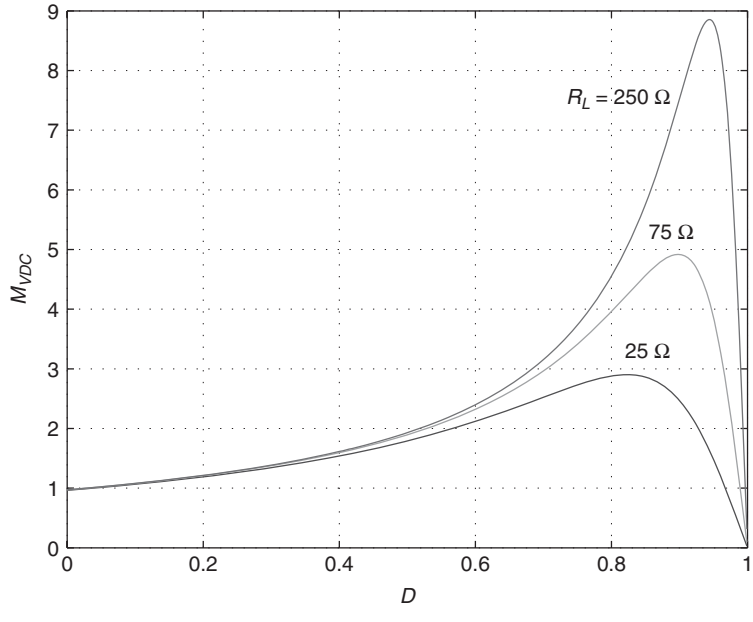


Figure 3.10 DC voltage transfer function $M_{V\,DC}$ of the lossy boost converter as a function of D for CCM at $V_O = 28\,\text{V}$, $r_{DS} = 0.5\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 25\,\text{m}\Omega$, $r_L = 0.3\,\Omega$, $r_C = 40\,\text{m}\Omega$, and $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$.

and

$$D_\eta = 2R_L\left(1 + \frac{V_F}{V_O} - \frac{r_C}{R_L} + f_s C_o R_L\right). \tag{3.69}$$

3.2.10 Design of Boost Converter for CCM

Design a PWM boost converter to meet the following specifications: V_I is the US single-phase rectified line, $V_O = 400\,\text{V}$, $I_{Omax} = 0.225\,\text{A}$, $I_{Omin} = 5\,\%$ of I_{Omax}, and $V_r/V_O < 1\,\%$.

Solution. Assume that the converter is operated in CCM. The rms voltage of the US utility line changes from 90 V (low line) to 132 V (high line) for normal operation. Hence, the minimum, nominal, and maximum values of the dc voltages at the output of a full-bridge front-end rectifier are

$$V_{Imin} = \sqrt{2}V_{rms(min)} = \sqrt{2} \times 90 = 127\,\text{V}, \tag{3.70}$$

$$V_{Inom} = \sqrt{2}V_{rms(nom)} = \sqrt{2} \times 110 = 156\,\text{V}, \tag{3.71}$$

and

$$V_{Imax} = \sqrt{2}V_{rms(max)} = \sqrt{2} \times 132 = 187\,\text{V}. \tag{3.72}$$

The minimum load current is

$$I_{Omin} = \frac{I_{Omax}}{20} = \frac{0.225}{20} = 11.25\,\text{mA}. \tag{3.73}$$

The maximum and minimum values of the output power are

$$P_{Omax} = V_O I_{Omax} = 400 \times 0.225 = 90\,\text{W} \tag{3.74}$$

and

$$P_{Omin} = V_O I_{Omin} = 400 \times 0.01125 = 4.5\,\text{W}. \tag{3.75}$$

The minimum and the maximum load resistances are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{400}{0.225} = 1.778\,\text{k}\Omega \tag{3.76}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{400}{0.01125} = 35.6\,\text{k}\Omega. \tag{3.77}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{400}{187} = 2.14, \tag{3.78}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{400}{156} = 2.56, \tag{3.79}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{400}{127} = 3.15. \tag{3.80}$$

Assume that the efficiency η of the converter is 90 %. Hence, the minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = 1 - \frac{\eta}{M_{V\,DCmin}} = 1 - \frac{0.9}{2.14} = 0.579, \tag{3.81}$$

$$D_{nom} = 1 - \frac{\eta}{M_{V\,DCnom}} = 1 - \frac{0.9}{2.56} = 0.649, \tag{3.82}$$

and

$$D_{max} = 1 - \frac{\eta}{M_{V\,DCmax}} = 1 - \frac{0.9}{3.15} = 0.714. \tag{3.83}$$

Let us assume the switching frequency $f_s = 100\,\text{kHz}$. The minimum inductance that ensures CCM operation at any duty cycle D is

$$L_{min} = \frac{2}{27}\,\frac{R_{Lmax}}{f_s} = \frac{2}{27}\,\frac{35.6 \times 10^3}{0.1 \times 10^6} = 26.37\,\text{mH}. \tag{3.84}$$

Since $D_{min} = 0.579 > 1/3$, the minimum inductance required for CCM operation can be calculated as

$$L_{min} = \frac{R_{Lmax} D_{min}(1 - D_{min})^2}{2f_s} = \frac{35.6 \times 10^3 \times 0.579 \times (1 - 0.579)^2}{2 \times 100 \times 10^3} = 18.23\,\text{mH}. \tag{3.85}$$

Pick $L = 20\,\text{mH}$. One can design this inductor so that its dc ESR is $r_{L(dc)} = 2.1\,\Omega$.

For $D > 0.5$, the maximum inductor peak-to-peak current of the ac component occurs at D_{min}. Hence,

$$\Delta i_{Lmax} = \frac{V_O D_{min}(1 - D_{min})}{f_s L} = \frac{400 \times 0.579 \times (1 - 0.579)}{10^5 \times 20 \times 10^{-3}} = 48.74\,\text{mA}. \tag{3.86}$$

The current and voltage stresses of the MOSFET and the diode are

$$\begin{aligned} I_{SMmax} = I_{DMmax} &= \frac{I_{Omax}}{1 - D_{max}} + \frac{V_O D_{max}(1 - D_{max})}{2f_s L} \\ &= \frac{0.225}{1 - 0.714} + \frac{400 \times 0.714 \times (1 - 0.714)}{2 \times 10^5 \times 20 \times 10^{-3}} = 0.8071\,\text{A} \end{aligned} \tag{3.87}$$

and

$$V_{SM} = V_{DM} = V_O = 400\,\text{V}. \tag{3.88}$$

One can select an MTP4N50 power MOSFET with $V_{DSS} = 500\,\text{V}$, $I_{SM} = 4\,\text{A}$, $r_{DS} = 1\,\Omega$, $Q_g = 27\,\text{nC}$, and $C_o = 100\,\text{pF}$. An MUR1560 ultrafast recovery diode is also chosen, which has $V_{DM} = 600\,\text{V}$, $I_{DM} = 15\,\text{A}$, $V_F = 0.7\,\text{V}$, and $R_F = 17.1\,\text{m}\Omega$.

The ripple voltage is

$$V_r = 0.01 V_O = 0.01 \times 400 = 4\,\text{V}. \tag{3.89}$$

Let us assume that the ripple voltage is equally divided between the capacitance and the ESR. Thus

$$V_{rcpp} = V_{Cpp} = \frac{V_r}{2} = \frac{4}{2} = 2\,\text{V}. \tag{3.90}$$

Hence, the maximum ESR is

$$r_{Cmax} = \frac{V_{rcpp}}{I_{DMmax}} = \frac{2}{0.8071} = 2.478\,\Omega, \tag{3.91}$$

and the minimum filter capacitance is

$$C_{min} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}} = \frac{0.714 \times 400}{10^5 \times 1778 \times 2} = 0.8\,\mu\text{F}. \tag{3.92}$$

Pick a metallized polyester capacitor with $C = 1\,\mu\text{F}/630\,\text{V}/1\,\Omega$.

The minimum corner frequency of the output filter is

$$f_{omin} = \frac{1}{2\pi C R_{Lmax}} = \frac{1}{2 \times \pi \times 10^{-6} \times 35.6 \times 10^3} = 4.47\,\text{Hz}, \tag{3.93}$$

and the maximum corner frequency of the output filter is

$$f_{Omax} = \frac{1}{2\pi CR_{Lmin}} = \frac{1}{2 \times \pi \times 10^{-6} \times 1778} = 89.5\,\text{Hz}. \tag{3.94}$$

The rms values of the inductor current is

$$I_{Lrms} \approx I_{Imax} = \frac{I_{Omax}}{1 - D_{max}} = \frac{0.225}{1 - 0.714} = 0.787\,\text{A}, \tag{3.95}$$

resulting in the inductor power loss

$$P_{rL} = r_L I_{Lrms}^2 = 2.1 \times 0.787^2 = 1.3\,\text{W}. \tag{3.96}$$

The rms values of the switch current is

$$I_{Srms} = \frac{\sqrt{D_{max}} I_{Omax}}{1 - D_{max}} = \frac{\sqrt{0.714} \times 0.225}{1 - 0.714} = 0.6648\,\text{A}, \tag{3.97}$$

which leads to the MOSFET conduction loss

$$P_{rDS} = r_{DS} I_{Srms}^2 = 1 \times 0.6648^2 = 0.442\,\text{W}. \tag{3.98}$$

The output capacitance of the MOSFET is $C_o = 100\,\text{pF}$. Hence, the switching loss is

$$P_{sw} = f_s C_o V_{SM}^2 = f_s C_o V_O^2 = 10^5 \times 100 \times 10^{-12} \times 400^2 = 1.6\,\text{W}. \tag{3.99}$$

The total power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 0.442 + 0.8 = 1.242\,\text{W}. \tag{3.100}$$

The diode power loss due to the diode offset voltage V_F is

$$P_{VF} = V_F I_{Omax} = 0.7 \times 0.225 = 0.1575\,\text{W}. \tag{3.101}$$

The diode rms current is

$$I_{Drms} = \frac{I_{Omax}}{\sqrt{1 - D_{max}}} = \frac{0.225}{\sqrt{1 - 0.714}} = 0.421\,\text{A}, \tag{3.102}$$

resulting in the power loss due to the diode forward resistance R_F,

$$P_{RF} = R_F I_{Drms}^2 = 0.0171 \times 0.421^2 = 3\,\text{mW}. \tag{3.103}$$

Thus, the diode conduction loss is

$$P_D = P_{VF} + P_{RF} = 0.158 + 0.003 = 0.161\,\text{W}. \tag{3.104}$$

The capacitor rms current is

$$I_{Crms} = I_{Omax} \sqrt{\frac{D_{max}}{1 - D_{max}}} = 0.225 \sqrt{\frac{0.714}{1 - 0.714}} = 0.3555\,\text{A}. \tag{3.105}$$

Assuming the ESR of the filter capacitor $r_C = 1\,\Omega$, the power loss in the capacitor is

$$P_{rC} = r_C I_{Crms}^2 = 1 \times 0.3555^2 = 0.1263\,\text{W}. \tag{3.106}$$

The total power loss is

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} = 0.442 + 1.6 + 0.161 + 1.3 + 0.1263 = 3.63\,\text{W}, \tag{3.107}$$

and the converter efficiency at full load is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{90}{90 + 3.63} = 96.12\,\%. \tag{3.108}$$

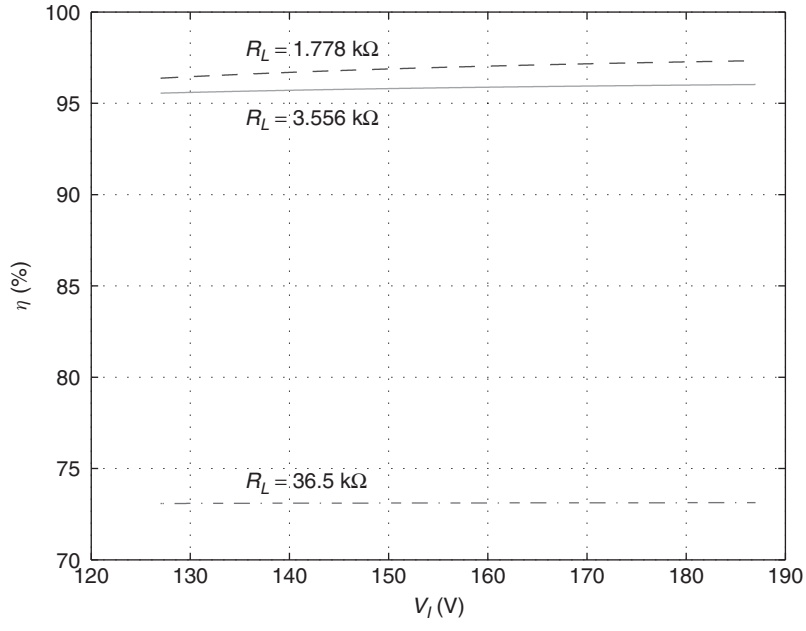


Figure 3.11 Efficiency η of the designed boost converter as a function of V_I at fixed values of R_L for CCM.

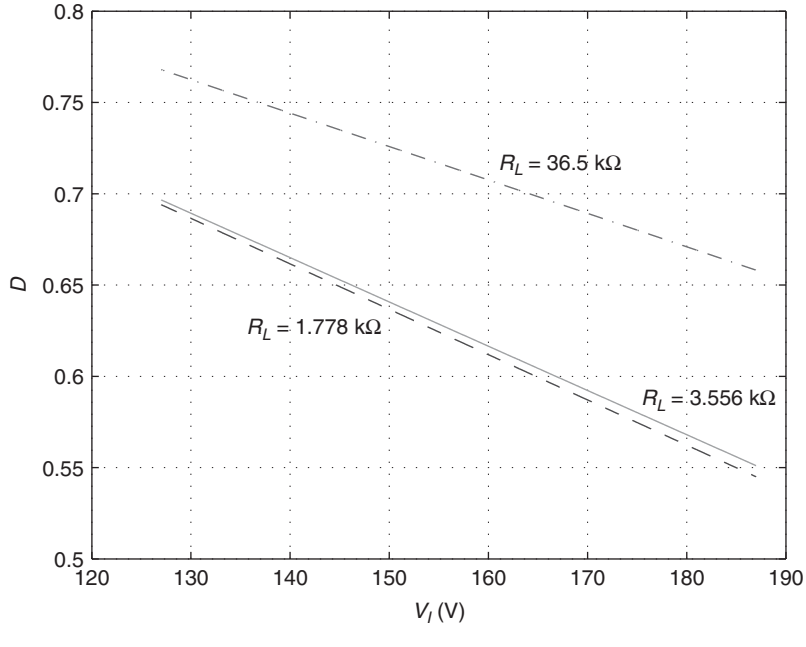


Figure 3.12 Duty cycle D of the boost converter designed as a function of V_I at fixed values of R_L for CCM.

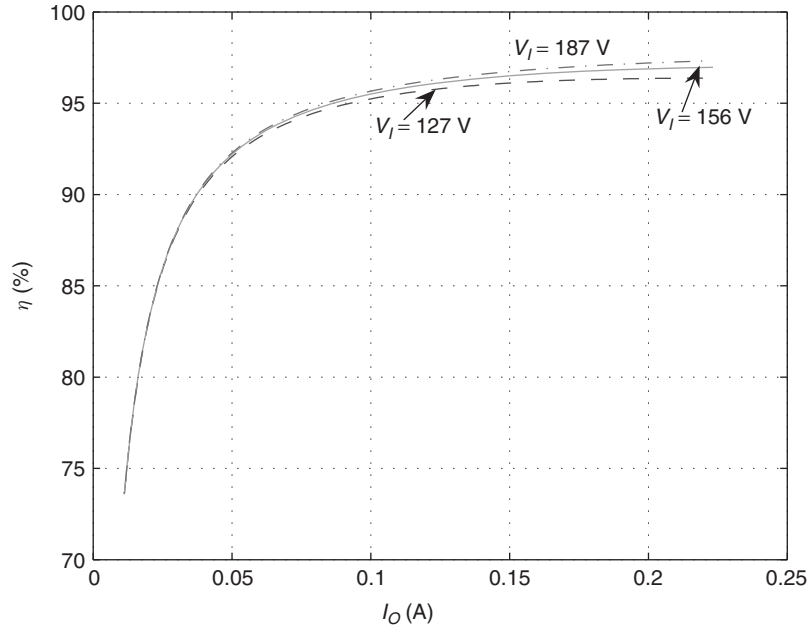


Figure 3.13 Efficiency η of the designed boost converter as a function of load current I_O at fixed values of V_I for CCM.

Assuming the magnitude of the gate-to-source voltage $V_{GSm} = 7\,\text{V}$, the gate-drive power is calculated as

$$P_G = f_s Q_g V_{GSm} = 10^5 \times 27 \times 10^{-9} \times 7 = 18.9\,\text{mW}. \tag{3.109}$$

Using (3.67)–(3.69), the efficiency η of the designed boost converter can be computed over the entire range of V_I and I_O (or R_L) for CCM. Using the calculated efficiency η, the duty cycle D can be calculated from (3.66). Figures 3.11 and 3.12 show the efficiency η and the duty cycle D of the designed boost converter versus the dc input voltage V_I at fixed load resistances R_L. Plots of the efficiency η and the duty cycle D as functions of I_O at fixed values of V_I are shown in Figures 3.13 and 3.14. Figures 3.15 and 3.16 show the efficiency η and the duty cycle D of the designed converter as functions of R_L at fixed values of V_I. The efficiency η increases as I_O increases (or R_L decreases). The maximum efficiency η_{max} occurs at the maximum load current I_{Omax}, and the minimum efficiency η_{min} occurs at the minimum load I_{Omin}, which is an advantage of the boost converter. The duty cycle D increases as V_I and I_O decrease.

3.3 DC Analysis of PWM Boost Converter for DCM

Equivalent circuits for the PWM boost converter operating in the DCM are depicted in Figure 3.17. Idealized current and voltage waveforms are shown in Figure 3.18. For the time interval $0 < t \leq DT$, the switch is ON and therefore the diode is OFF. The voltage across

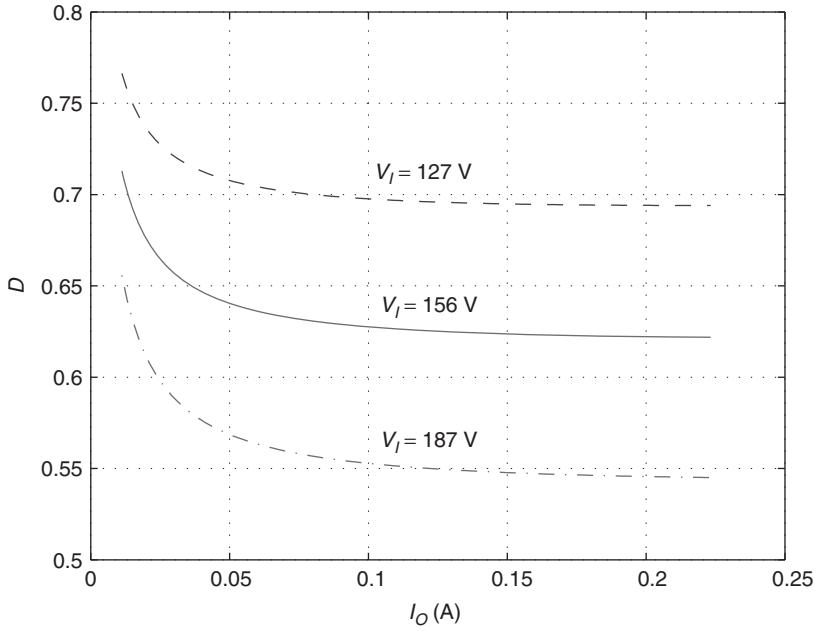


Figure 3.14 Duty cycle D of the designed boost converter as a function of load current I_O at fixed values of V_I for CCM.

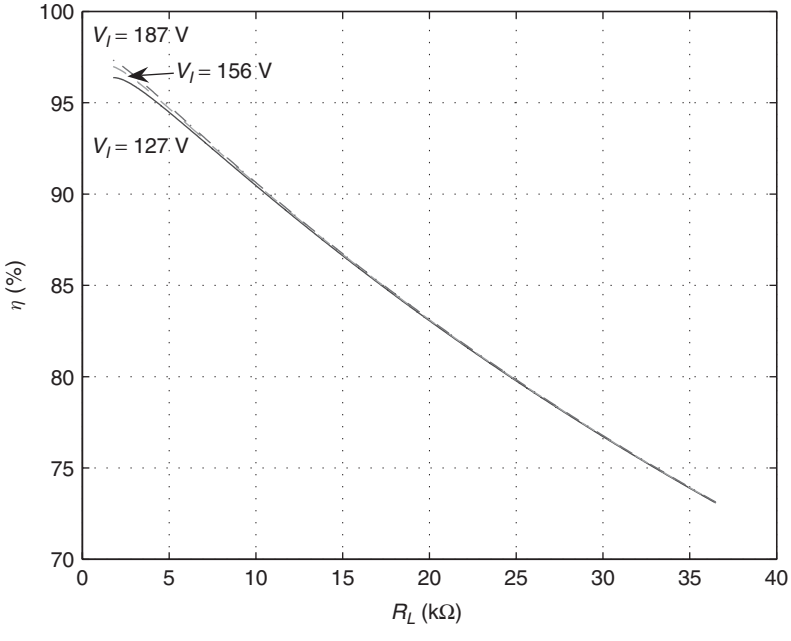


Figure 3.15 Efficiency η of the designed boost converter as a function of load resistance R_L at fixed values of V_I for CCM.

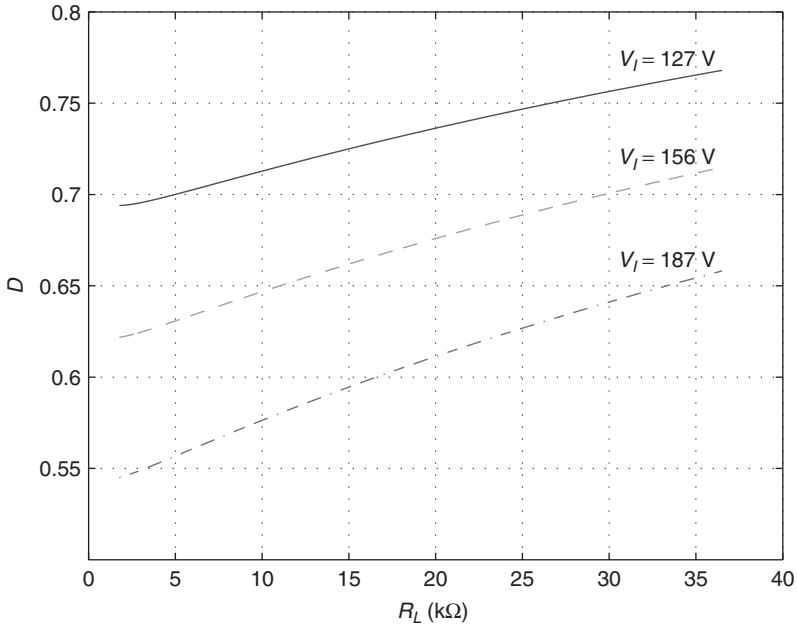


Figure 3.16 Duty cycle D of the designed boost converter as a function of load resistance R_L at fixed values of V_I for CCM.

the inductor is V_I and the inductor current increases linearly from zero. For the time interval $DT < t \leq (D + D_1)T$, the switch is OFF and the diode is ON. At time $t = (D + D_1)T$, the inductor and diode current reaches zero, turning the diode off. For the time interval $(D + D_1)T < t \leq T$, both the switch and the diode are OFF. Since the current through the inductor is constant (equal to zero), the voltage across the inductor is zero. At time $t = T$, the switch is turned on and the inductor current starts to increase from zero.

3.3.1 Time Interval $0 < t \leq DT$

During this time interval, the switch is ON and the diode is OFF. The equivalent circuit is shown in Figure 3.17(b). The switch voltage v_S and the diode current i_D are zero. The voltage across the inductor L is

$$v_L = V_I = L\frac{di_L}{dt}, \qquad i_L(0) = 0, \tag{3.110}$$

and the inductor and switch current is

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\, dt = \frac{1}{L}\int_0^t V_I\, dt = \frac{V_I}{L}t. \tag{3.111}$$

Hence, the peak switch and inductor current is

$$I_{SM} = \Delta i_L = i_L(DT) = \frac{V_I DT}{L} = \frac{V_I D}{f_s L}. \tag{3.112}$$

The voltage across the diode is

$$v_D = -V_O. \tag{3.113}$$

This time interval ends when the switch is turned off by the driver.

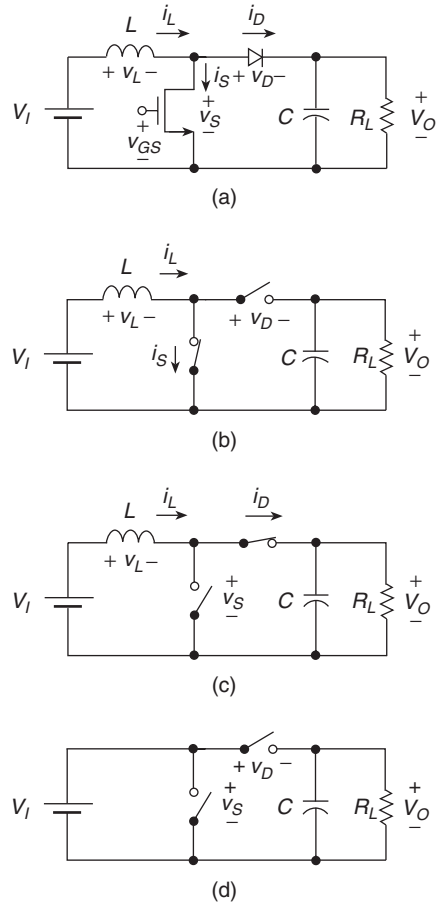


Figure 3.17 PWM boost converter and its ideal equivalent circuits for DCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON. (d) Equivalent circuit when both the switch and the diode are OFF.

3.3.2 Time Interval $DT < t \leq (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 3.17(c). The switch is OFF and the diode is ON. Hence, $i_S = 0$ and $v_D = 0$. The voltage across the inductor L is given by

$$v_L = V_I - V_O = L\frac{di_L}{dt} < 0. \tag{3.114}$$

Using (3.112), the diode and inductor current is

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t}(V_I - V_O)\,dt + i_L(DT) \\ &= \frac{V_I - V_O}{L}(t - DT) + i_L(DT) = \frac{V_I - V_O}{L}(t - DT) + \frac{V_I DT}{L}. \end{aligned} \tag{3.115}$$

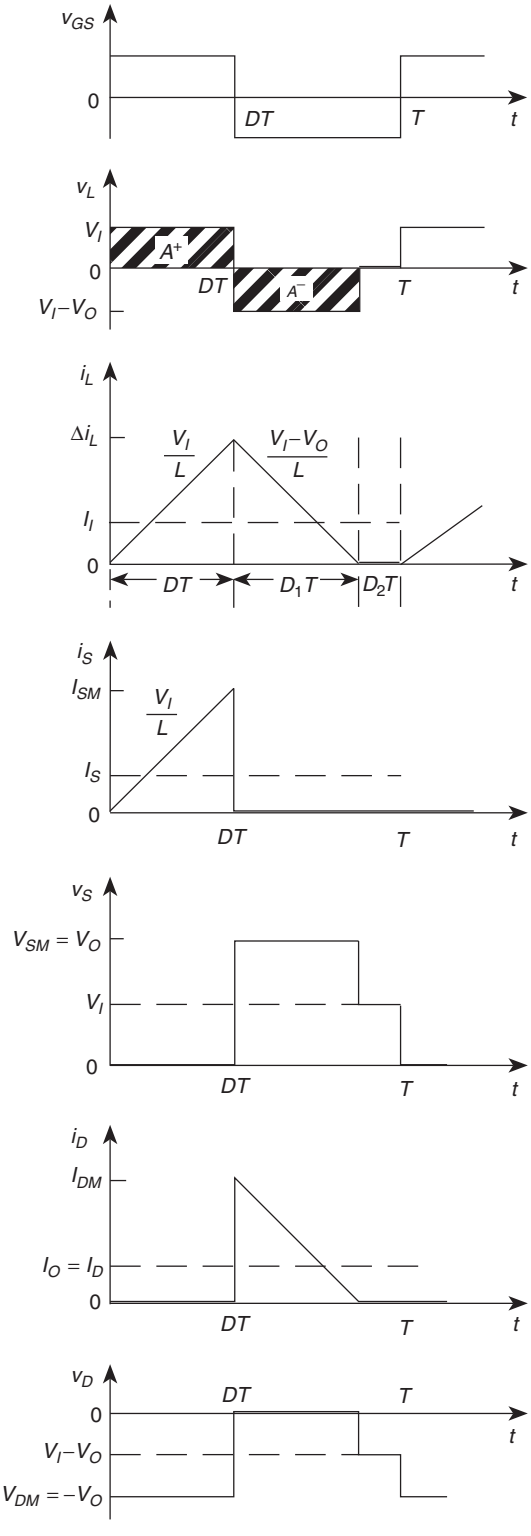


Figure 3.18 Idealized current and voltage waveforms in the PWM boost converter for DCM.

The peak diode and inductor current is given by

$$I_{DM} = \Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^{DT} (V_I - V_O)\,dt = \frac{(V_O - V_I)D_1T}{L}$$
$$= \frac{(V_O - V_I)D_1}{f_sL}. \tag{3.116}$$

The voltage across the switch is

$$v_S = V_O. \tag{3.117}$$

When the diode current reaches zero, this time interval ends.

3.3.3 Time Interval $(D + D_1)T < t \leq T$

During this time interval, both the switch and the diode are OFF. The equivalent circuit is shown in Figure 3.17(d). The inductor current i_L, the inductor voltage v_L, the switch current i_S, and the diode current i_D are zero. The voltage across the switch is

$$v_S = V_I, \tag{3.118}$$

and the voltage across the diode is

$$v_D = V_I - V_O. \tag{3.119}$$

This time ends when the switch is turned on by the driver.

3.3.4 Device Stresses for DCM

The maximum switch and diode voltage stresses for steady state are

$$V_{SMmax} = V_{DMmax} = V_O. \tag{3.120}$$

The maximum steady-state switch and diode current stresses occur at full power and are

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{V_{Imin}D_{max}}{f_sL}. \tag{3.121}$$

3.3.5 DC Voltage Transfer Function for DCM

Referring to Figure 3.18 and using the volt-second balance,

$$V_IDT = (V_O - V_I)D_1T, \tag{3.122}$$

leading to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = 1 + \frac{D}{D_1}. \tag{3.123}$$

From (3.112) and (3.123), the peak-to-peak current is

$$\Delta i_L = i_L(DT) = \frac{V_IDT}{L} = \frac{V_OD}{f_sLM_{V\,DC}}. \tag{3.124}$$

Using (3.123) and (3.124), the dc input current is obtained as an average value of the inductor current

$$I_I = \frac{1}{T}\int_0^T i_L\,dt = \frac{(D+D_1)\Delta i_L}{2} = \frac{(D+D_1)DV_O}{2f_sLM_{V\,DC}} = \frac{D^2V_O}{2f_sL(M_{V\,DC}-1)}, \tag{3.125}$$

from which

$$I_O = \frac{I_I}{M_{V\,DC}} = \frac{V_OD^2}{2f_sLM_{V\,DC}(M_{V\,DC}-1)}. \tag{3.126}$$

Hence,

$$D = \sqrt{\frac{2f_sLI_OM_{V\,DC}(M_{V\,DC}-1)}{V_O}} = \sqrt{\frac{2f_sLM_{V\,DC}(M_{V\,DC}-1)}{R_L}}. \tag{3.127}$$

At the CCM/DCM boundary, $M_{V\,DCB} = 1/(1-D_B)$, as in CCM. Therefore, the boundary occurs at

$$\frac{2f_sLI_O}{V_O} = \frac{2f_sL}{R_L} = D_B(1-D_B)^2. \tag{3.128}$$

As the normalized load current is increased from zero to $4f_sLI_O/(27V_O)$, the boundary duty cycle D_B increases from zero to 1/3 and then decreases to 0. Figures 3.19 and 3.20 show plots of the duty cycle D versus the normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of $M_{V\,DC}$ for both CCM and DCM.

From (3.127), one obtains

$$M_{V\,DC}^2 - M_{V\,DC} - \frac{D^2R_L}{2f_sL} = 0, \tag{3.129}$$

which produces the dc voltage transfer function of the boost converter for DCM,

$$\begin{aligned} M_{V\,DC} = \frac{V_O}{V_I} &= \frac{1+\sqrt{1+\dfrac{2D^2V_O}{f_sLI_O}}}{2} \\ &= \frac{1+\sqrt{1+\dfrac{2D^2R_L}{f_sL}}}{2} \quad \text{for } \frac{R_L}{2f_sL} \geq \frac{M_{V\,DC}^3}{M_{V\,DC}-1} \quad \text{or } \frac{2f_sLI_O}{V_O} \\ &\leq \frac{M_{V\,DC}-1}{M_{V\,DC}^3}. \end{aligned} \tag{3.130}$$

It can be seen that $M_{V\,DC}$ depends on D, R_L, L, and f_s. Figures 3.21 and 3.22 show plots of $M_{V\,DC}$ versus $I_O/(V_O/2f_sL)$ and $R_L/(2f_sL)$ at fixed values of D.

Rearrangement of (3.130) produces the inductance required for given values of $M_{V\,DC}$, D, R_L, and f_s:

$$L = \frac{D^2R_L}{2M_{V\,DC}(M_{V\,DC}-1)f_s}. \tag{3.131}$$

From (3.123) and (3.130), one obtains D_1 in terms of D, R_L, L, and f_s:

$$D_1 = \frac{D}{M_{V\,DC}-1} = \sqrt{\frac{2f_sLM_{V\,DC}}{R_L(M_{V\,DC}-1)}} = \frac{2D}{\sqrt{1+\dfrac{2D^2R_L}{f_sL}}-1}. \tag{3.132}$$

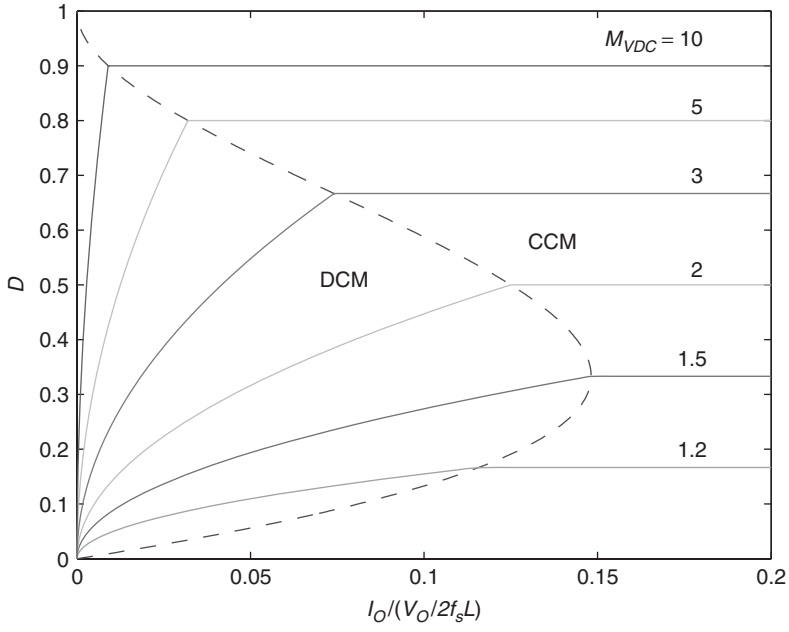


Figure 3.19 Duty cycle D as a function of normalized load current $I_O/(V_O/2f_sL)$ at various values of $M_{V\,DC}$ for the lossless boost converter.

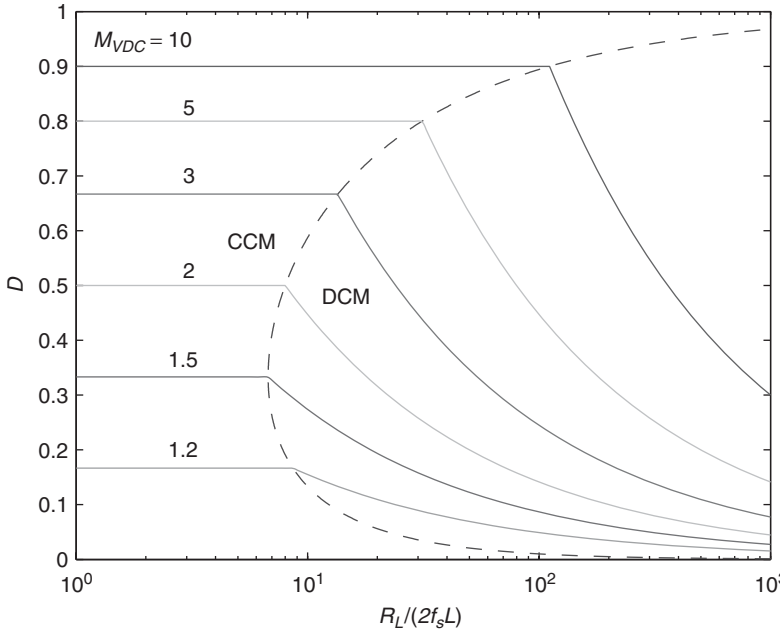


Figure 3.20 Duty cycle D as a function of normalized load resistance $R_L/(2f_sL)$ at various values of $M_{V\,DC}$ for the lossless boost converter.

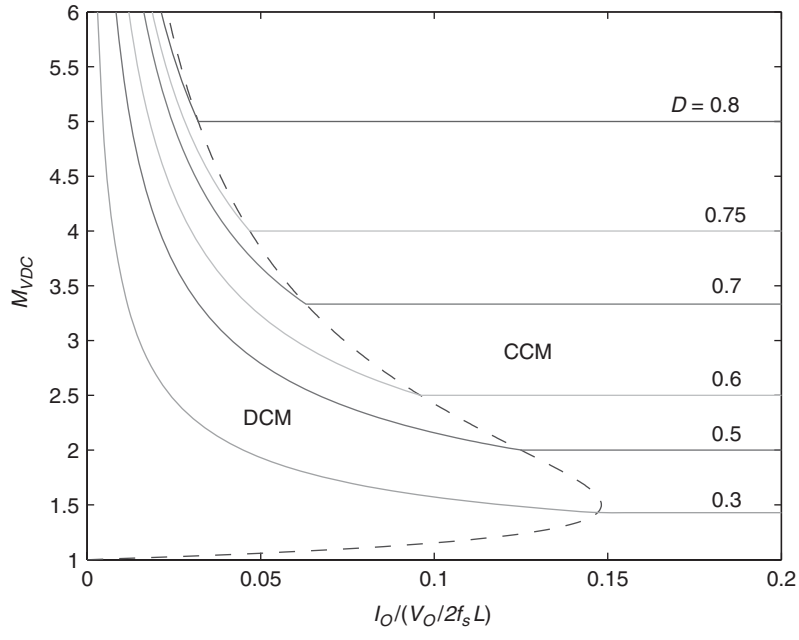


Figure 3.21 DC voltage transfer function $M_{V\,DC}$ as a function of normalized load current $I_O/(V_O/2f_sL)$ at various values of D for the lossless boost converter.

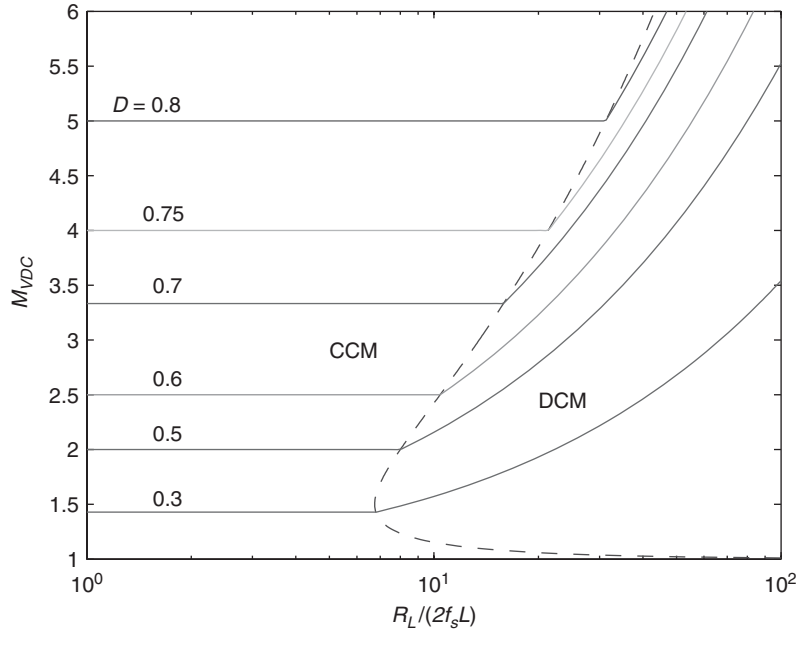


Figure 3.22 DC voltage transfer function $M_{V\,DC}$ as a function of normalized load resistance $R_L/(2f_sL)$ at various values of D for the lossless boost converter.

3.3.6 Maximum Inductance for DCM

The dc output current at the CCM/DCM boundary occurs at $D = D_{Bmin}$ for $D < 1/3$ and at $D = D_{Bmax}$ for $D > 1/3$. Therefore,

$$I_{OBmin} = \begin{cases} \dfrac{V_O D_{Bmin}(1 - D_{Bmin})^2}{2 f_s L_{max}}, & \text{for } D < \dfrac{1}{3}, \\ \dfrac{V_O D_{Bmax}(1 - D_{Bmax})^2}{2 f_s L_{max}}, & \text{for } D \geq \dfrac{1}{3}, \end{cases} \tag{3.133}$$

and

$$L_{max} = \begin{cases} \dfrac{R_{Lmin} D_{Bmin}(1 - D_{Bmin})^2}{2 f_s}, & \text{for } D < \dfrac{1}{3}, \\ \dfrac{R_{Lmin} D_{Bmax}(1 - D_{Bmax})^2}{2 f_s}, & \text{for } D \geq \dfrac{1}{3}. \end{cases} \tag{3.134}$$

If $D_{Bmin} < 1/3$ and $D_{Bmax} > 1/3$,

$$L_{max} = \frac{R_{Lmin}}{2 f_s} \times \min\left\{ D_{Bmin}(1 - D_{Bmin})^2, D_{Bmax}(1 - D_{Bmax})^2 \right\}. \tag{3.135}$$

3.3.7 Power Losses and Efficiency of Boost Converter for DCM

Substitution of (3.130) into (3.124) yields

$$\begin{aligned} \Delta i_L = I_{SM} = I_{DM} = \frac{V_I D}{f_s L} = \frac{D V_O}{f_s L M_{V\,DC}} &= V_O \sqrt{\frac{2(M_{V\,DC} - 1)}{f_s L R_L M_{V\,DC}}} \\ &= \frac{2 D V_O}{f_s L} \frac{1}{\left(1 + \sqrt{1 + \dfrac{2 D^2 R_L}{f_s L}} \right)}. \end{aligned} \tag{3.136}$$

The rms value of the switch current is

$$\begin{aligned} I_{Srms} = \sqrt{\frac{1}{T} \int_0^{DT} i_S^2 \, dt} = \Delta i_L \sqrt{\frac{D}{3}} &= V_O \sqrt{\frac{2}{3 R_L} \sqrt{\frac{2(M_{V\,DC} - 1)^3}{f_s L R_L M_{V\,DC}}}} \\ &= \frac{2 D \sqrt{D} V_O}{\sqrt{3} f_s L} \frac{1}{\left(1 + \sqrt{1 + \dfrac{2 D^2 R_L}{f_s L}} \right)}, \end{aligned} \tag{3.137}$$

resulting in the MOSFET conduction loss

$$\begin{aligned} P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} \Delta i_L^2}{3} = \frac{2 r_{DS}}{3} \sqrt{\frac{2(M_{V\,DC} - 1)^3}{f_s L R_L M_{V\,DC}}} P_O = \frac{4 r_{DS} D^3 V_O^2}{3 f_s^2 L^2} \\ \times \frac{1}{\left(1 + \sqrt{1 + \dfrac{2 D^2 R_L}{f_s L}} \right)^2} = \frac{4 r_{DS} R_L D^3}{3 f_s^2 L^2} \frac{1}{\left(1 + \sqrt{1 + \dfrac{2 D^2 R_L}{f_s L}} \right)^2} P_O. \end{aligned} \tag{3.138}$$

The switching loss in the converter is

$$P_{sw} = f_s C_o V_O^2 = f_s C_o R_L P_O. \tag{3.139}$$

Likewise, the rms value of the diode current is

$$I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} i_D^2\, dt} = \Delta i_L \sqrt{\frac{D_1}{3}} = V_O \sqrt{\frac{2}{3R_L}\sqrt{\frac{2(M_{V\,DC}-1)}{f_s L R_L M_{V\,DC}}}}$$

$$= 2V_O \sqrt{\frac{D}{3f_s L R_L}} \frac{1}{\sqrt{1+\sqrt{1+\dfrac{2D^2R_L}{f_s L}}}}, \tag{3.140}$$

which gives the diode conduction loss associated with R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{D_1 R_F \Delta i_L^2}{3} = \frac{2R_F}{3}\sqrt{\frac{2(M_{V\,DC}-1)}{f_s L R_L M_{V\,DC}}} P_O$$

$$= \frac{4DR_F V_O^2}{3f_s L R_L} \frac{1}{\left(1+\sqrt{1+\dfrac{2D^2R_L}{f_s L}}\right)} = \frac{4DR_F}{3f_s L} \frac{1}{\left(1+\sqrt{1+\dfrac{2D^2R_L}{f_s L}}\right)} P_O. \tag{3.141}$$

The average current through the diode is $I_D = I_O$, yielding the diode conduction loss associated with V_F,

$$P_{VF} = I_D V_F = I_O V_F = \frac{V_F}{V_O} P_O. \tag{3.142}$$

Therefore, the total diode conduction loss is

$$P_D = P_{VF} + P_{RF} = \left[\frac{V_F}{V_O} + \frac{2R_F}{3}\sqrt{\frac{2(M_{V\,DC}-1)}{f_s L R_L M_{V\,DC}}}\right] P_O$$

$$= \left(\frac{V_F}{V_O} + \frac{4DR_F}{3f_s L} \frac{1}{\sqrt{1+\frac{2D^2R_L}{f_s L}}+1}\right) P_O. \tag{3.143}$$

The rms value of the inductor current is

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^{(D+D_1)T} i_L^2\, dt} = \Delta i_L \sqrt{\frac{D+D_1}{3}} = V_O \sqrt{\frac{2}{3R_L}\sqrt{\frac{2M_{V\,DC}(M_{V\,DC}-1)}{f_s L R_L}}}$$

$$= V_O \sqrt{\frac{2D}{3f_s L R_L}}, \tag{3.144}$$

resulting in the conduction loss in the inductor ESR,

$$P_{rL} = r_L I_{Lrms}^2 = \frac{r_L (D+D_1)\Delta i_L^2}{3} = \frac{2r_L}{3}\sqrt{\frac{2M_{V\,DC}(M_{V\,DC}-1)}{f_s L R_L}} P_O$$

$$= \frac{2Dr_L V_O^2}{3f_s L R_L} = \frac{2Dr_L}{3f_s L} P_O. \tag{3.145}$$

The total power loss is

$$\begin{aligned}
P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} \\
&= \left[\frac{2r_{DS}}{3} \sqrt{\frac{2(M_{V\,DC}-1)^3}{f_s L R_L M_{V\,DC}}} + \frac{2R_F}{3} \sqrt{\frac{2(M_{V\,DC}-1)}{f_s L M_{V\,DC} R_L}} \right. \\
&\quad \left. + \frac{2r_L}{3} \sqrt{\frac{2M_{V\,DC}(M_{V\,DC}-1)}{f_s L R_L}} + \frac{V_F}{V_O} + f_s C_o R_L \right] P_O \\
&= \left[\frac{4r_{DS} R_L D^3}{3 f_s^2 L^2} \frac{1}{\left(1 + \sqrt{1 + \dfrac{2D^2 R_L}{f_s L}}\right)^2} + \frac{4DR_F}{3 f_s L} \frac{1}{\left(1 + \sqrt{1 + \dfrac{2D^2 R_L}{f_s L}}\right)} \right. \\
&\quad \left. + \frac{2Dr_L}{3 f_s L} + \frac{V_F}{V_O} + f_s C_o R_L \right] P_O, \qquad (3.146)
\end{aligned}$$

and the efficiency can be found to be

$$\begin{aligned}
\eta &= \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \frac{P_{LS}}{P_O}} \\
&= \left[1 + \frac{2r_{DS}}{3} \sqrt{\frac{2(M_{V\,DC}-1)^3}{f_s L R_L M_{V\,DC}}} + \frac{2R_F}{3} \sqrt{\frac{2(M_{V\,DC}-1)}{f_s L M_{V\,DC} R_L}} \right. \\
&\quad \left. + \frac{2r_L}{3} \sqrt{\frac{2M_{V\,DC}(M_{V\,DC}-1)}{f_s L R_L}} + \frac{V_F}{V_O} + f_s C_o R_L \right]^{-1} \\
&= \left[1 + \frac{4r_{DS} R_L D^3}{3 f_s^2 L^2} \frac{1}{\left(1 + \sqrt{1 + \frac{2D^2 R_L}{f_s L}}\right)^2} + \frac{4DR_F}{3 f_s L} \frac{1}{\left(1 + \sqrt{1 + \frac{2D^2 R_L}{f_s L}}\right)} \right. \\
&\quad \left. + \frac{2Dr_L}{3 f_s L} + \frac{V_F}{V_O} + f_s C_o R_L \right]^{-1}. \qquad (3.147)
\end{aligned}$$

Using (3.125), the dc input power is

$$P_I = V_I I_I = \frac{D^2 V_I V_O}{2 f_s L (M_{V\,DC} - 1)}, \qquad (3.148)$$

the dc output power is

$$P_O = \frac{V_O^2}{R_L}, \qquad (3.149)$$

and the converter efficiency is

$$\eta = \frac{P_O}{P_I} = \frac{2 f_s L M_{V\,DC}(M_{V\,DC} - 1)}{D^2 R_L}. \qquad (3.150)$$

Hence, the duty cycle for the lossy boost converter in DCM is

$$D = \sqrt{\frac{2 f_s L M_{V\,DC}(M_{V\,DC} - 1)}{\eta R_L}} = \sqrt{\frac{2 f_s L I_O M_{V\,DC}(M_{V\,DC} - 1)}{\eta V_O}}, \qquad (3.151)$$

and the dc voltage transfer function for the lossy boost converter in DCM is

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{1 + \sqrt{1 + \dfrac{2\eta D^2 V_O}{f_s L I_O}}}{2}$$
$$= \frac{1 + \sqrt{1 + \dfrac{2\eta D^2 R_L}{f_s L}}}{2} \quad \text{for } \frac{R_L}{2f_s L} \geq \frac{M_{V\,DC}^3}{M_{V\,DC} - 1} \quad \text{or } \frac{2f_s L I_O}{V_O}$$
$$\leq \frac{M_{V\,DC} - 1}{M_{V\,DC}^3}. \tag{3.152}$$

3.3.8 Design of Boost Converter for DCM

Example 3.1

A boost converter has the following parameters: $V_I = 8$ to 18 V, $V_O = 24$ V, $P_{Omax} = 48$ W, $P_{Omin} = 0$, $r_L = 0.05\,\Omega$, $r_C = 0.01\,\Omega$, $r_{DS} = 0.055\,\Omega$, $C_o = 100$ pF, $R_F = 0.025\,\Omega$, $V_F = 0.3$ V, $f_s = 100$ kHz, and $V_r/V_O \leq 1\,\%$. Find component values, component stresses, and the efficiency at full power.

Solution. At full power, the maximum load current is

$$I_{Omax} = \frac{P_{Omax}}{V_O} = \frac{48}{24} = 2\,\text{A}, \tag{3.153}$$

and the minimum load resistance is

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{24}{2} = 12\,\Omega. \tag{3.154}$$

The minimum and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{24}{18} = 1.333 \tag{3.155}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{24}{8} = 3. \tag{3.156}$$

Hence, the minimum and maximum values of the duty cycle at the CCM/DCM boundary are

$$D_{Bmin} = 1 - \frac{1}{M_{V\,DCmin}} = 1 - \frac{1}{1.333} = 0.25 \tag{3.157}$$

and

$$D_{Bmax} = 1 - \frac{1}{M_{V\,DCmax}} = 1 - \frac{1}{3} = 0.67. \tag{3.158}$$

The maximum inductances required for DCM operation at D_{Bmax} and D_{Bmin} are

$$L_{1max} = \frac{R_{Lmin} D_{Bmax}(1 - D_{Bmax})^2}{2f_s} = \frac{12 \times 0.67 \times (1 - 0.67)^2}{2 \times 10^5} = 4.444\,\mu\text{H} \tag{3.159}$$

and

$$L_{2max} = \frac{R_{Lmin} D_{Bmin}(1 - D_{Bmin})^2}{2f_s} = \frac{12 \times 0.25 \times (1 - 0.25)^2}{2 \times 10^5} = 8.438\,\mu\text{H}, \tag{3.160}$$

resulting in the maximum inductance required for DCM operation under any operating conditions

$$L_{max} = \min\{L_{1max}, L_{2max}\} = L_{1max} = 4.444\,\mu\text{H}. \tag{3.161}$$

Let $L = 3.3\,\mu\text{H} < L_{max}$. Hence, assuming $\eta = 0.9$, the maximum duty cycle at R_{Lmin} is

$$D_{max} = \sqrt{\frac{2f_s L M_{V\,DCmax}(M_{V\,DCmax} - 1)}{\eta R_{Lmin}}}$$

$$= \sqrt{\frac{2 \times 10^5 \times 3.3 \times 10^{-6} \times 3 \times (3-1)}{0.9 \times 12}} = 0.606, \tag{3.162}$$

and

$$D_{1min} = \frac{D_{max}}{M_{V\,DCmax} - 1} = \frac{0.606}{3-1} = 0.303, \tag{3.163}$$

yielding

$$D_{max} + D_{1min} = 0.606 + 0.303 = 0.909 < 1. \tag{3.164}$$

The minimum duty cycle at R_{Lmin} is

$$D_{min} = \sqrt{\frac{2f_s L M_{V\,DCmin}(M_{V\,DCmin} - 1)}{\eta R_{Lmin}}}$$

$$= \sqrt{\frac{2 \times 10^5 \times 3.3 \times 10^{-6} \times 1.333 \times (1.333-1)}{0.9 \times 12}} = 0.165 \tag{3.165}$$

and

$$D_{1max} = \frac{D_{min}}{M_{V\,DCmin} - 1} = \frac{0.165}{1.333 - 1} = 0.494 \tag{3.166}$$

producing

$$D_{min} + D_{1max} = 0.165 + 0.494 = 0.66 < 1. \tag{3.167}$$

The maximum peak switch, diode, and inductor current is

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{D_{max} V_{Imin}}{f_s L} = \frac{0.606 \times 8}{10^5 \times 3.3 \times 10^{-6}} = 14.69\,\text{A}. \tag{3.168}$$

The maximum switch and diode voltage stress is

$$V_{SM} = V_{DM} = V_O = 24\,\text{V}. \tag{3.169}$$

The ripple voltage on the output voltage is

$$V_r = 0.01 V_O = 0.01 \times 24 = 0.24\,\text{V}. \tag{3.170}$$

The peak-to-peak ripple voltage across $r_C = 0.01\,\Omega$ is

$$V_{rC} = r_C I_{DMmax} = 0.01 \times 14.69 = 0.1469\,\text{V}. \tag{3.171}$$

Thus, the ripple voltage across the filter capacitance C is

$$V_{Cpp} = V_r - V_{rC} = 0.24 - 0.1469 = 0.0931\,\text{V}. \tag{3.172}$$

Hence, the minimum capacitance is

$$C_{min} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}} = \frac{0.606 \times 24}{10^5 \times 12 \times 0.0931} = 130.18\,\mu\text{F}. \tag{3.173}$$

Pick $C = 150\,\mu\text{F}/0.01\,\Omega/36\,\text{V}$.

The component power losses will be calculated at $V_{Imin} = 8\,\text{V}$, $R_{Lmin} = 12\,\Omega$, $P_{Omax} = 48\,\text{W}$, and $I_{Omax} = 2\,\text{A}$. The conduction loss in the power MOSFET is

$$P_{rDS} = \frac{2r_{DS}}{3}\sqrt{\frac{2(M_{V\,DCmax}-1)^3}{f_s L R_{Lmin} M_{V\,DCmax}}}P_{Omax}$$

$$= \frac{2\times 0.055}{3}\sqrt{\frac{2\times(3-1)^3}{10^5\times 3.3\times 10^{-6}\times 12\times 3}}\times 48 = 2.043\,\text{W}. \tag{3.174}$$

The switching loss is

$$P_{sw} = f_s C_o V_O^2 = 10^5\times 100\times 10^{-12}\times 24^2 = 5.76\,\text{mW}. \tag{3.175}$$

The power loss in the diode forward resistance is

$$P_{RF} = \frac{2R_F}{3}\sqrt{\frac{2(M_{V\,DCmax}-1)}{f_s L R_{Lmin} M_{V\,DCmax}}}P_{Omax}$$

$$= \frac{2\times 0.025}{3}\sqrt{\frac{2\times(3-1)}{10^5\times 3.3\times 10^{-6}\times 12\times 3}}\times 48 = 0.464\,\text{W}, \tag{3.176}$$

and the power loss in the diode offset voltage source V_F is

$$P_{VF} = V_F I_{Omax} = 0.3\times 2 = 0.6\,\text{W}, \tag{3.177}$$

resulting in the diode conduction loss

$$P_D = P_{RF} + P_{VF} = 0.464 + 0.6 = 1.064\,\text{W}. \tag{3.178}$$

The power loss in the inductor is

$$P_{rL} = \frac{2r_L}{3}\sqrt{\frac{2M_{V\,DCmax}(M_{V\,DCmax}-1)}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2\times 0.05}{3}\sqrt{\frac{2\times 3\times(3-1)}{10^5\times 3.3\times 10^{-6}\times 12}}\times 48 = 2.785\,\text{W}. \tag{3.179}$$

The overall power loss is

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} = 2.043 + 0.006 + 1.064 + 2.785 = 5.898\,\text{W}. \tag{3.180}$$

The efficiency of the converter boost for DCM is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{48}{48 + 5.898} = 89.06\,\%. \tag{3.181}$$

Assuming the gate charge $Q_g = 50\,\text{nC}$ and $V_{DSpp} = 8\,\text{V}$, the MOSFET gate-drive power is

$$P_G = f_s Q_g V_{GSm} = 100\times 10^3\times 50\times 10^{-9}\times 8 = 40\,\text{mW}. \tag{3.182}$$

Figures 3.23 and 3.24 depict the efficiency η and the duty cycle D of the designed boost converter as functions of V_I at fixed load resistances R_L for DCM. Figures 3.25 and 3.26 show the efficiency η and the duty cycle D and of the designed converter as functions of I_O and R_L at fixed values of V_I. Figures 3.27 and 3.28 depict the efficiency η and the duty cycle D of the designed boost converter as functions of R_L at fixed values of V_I. The duty cycle D decreases as V_I increases and I_O decreases (or R_L increases). The efficiency η increases as V_I increases, and decreases as I_O increases (or R_L decreases).

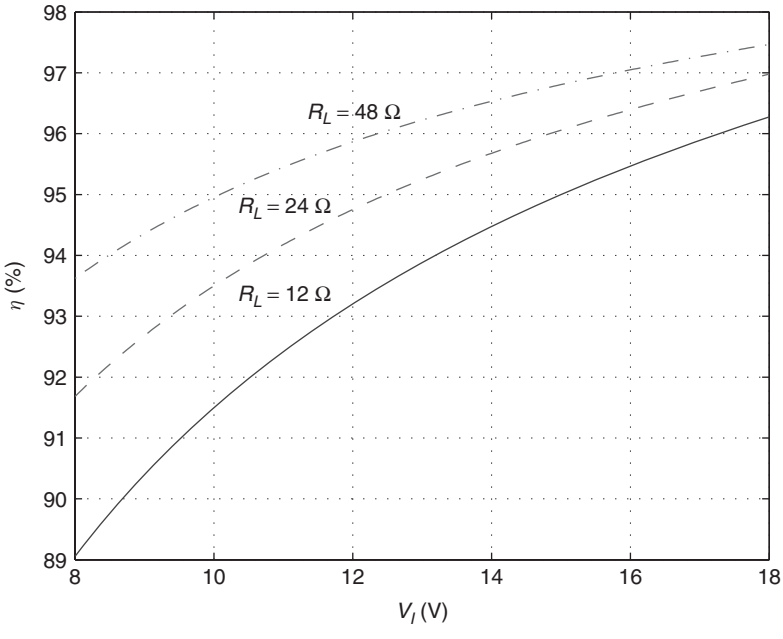


Figure 3.23 Efficiency η as a function of V_I at fixed values of R_L for the boost converter in DCM.

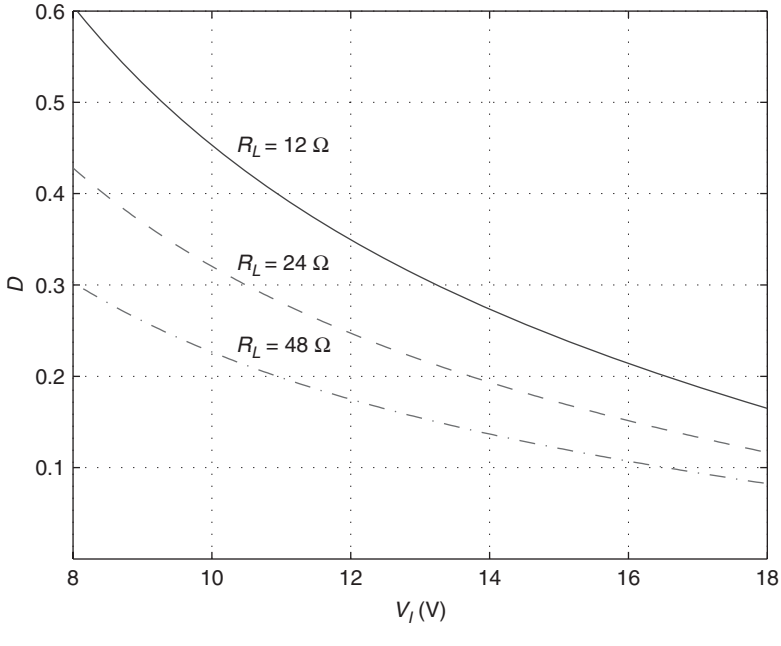


Figure 3.24 Duty cycle D as a function of V_I at fixed values of R_L for the boost converter in DCM.

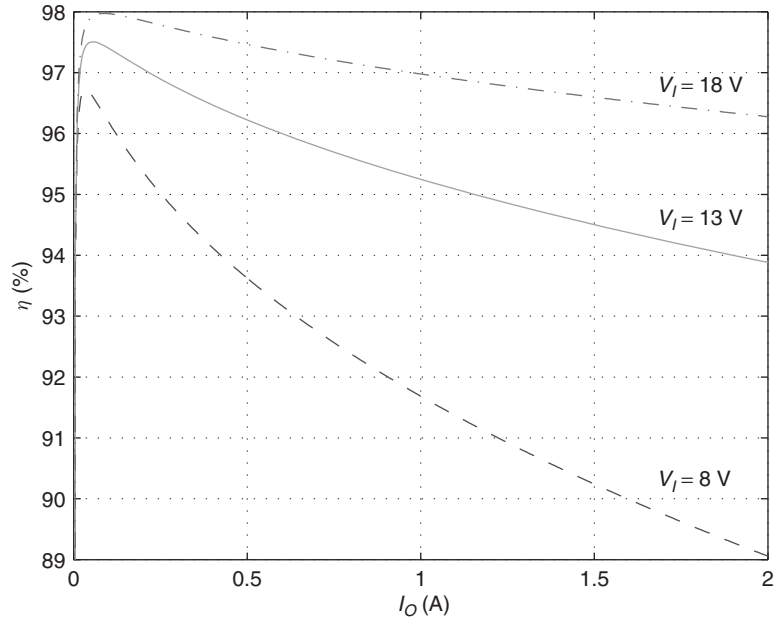


Figure 3.25 Efficiency η as a function of I_O at fixed values of V_I for the designed boost converter in DCM.

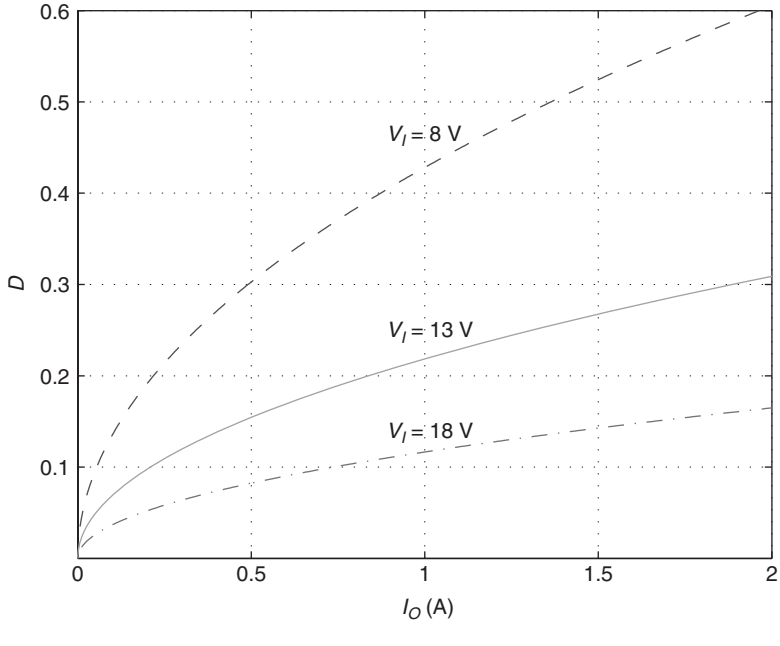


Figure 3.26 Duty cycle D as a function of I_O at fixed values of V_I for the boost converter in DCM.

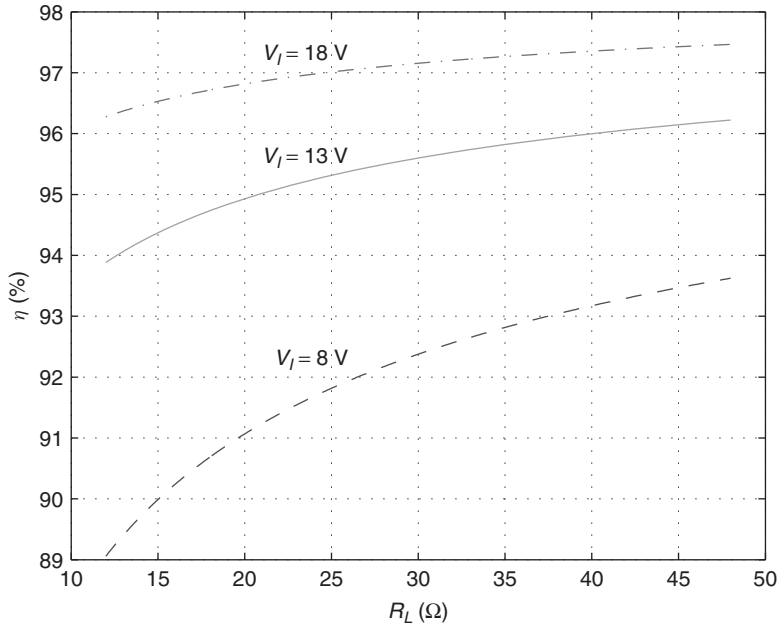


Figure 3.27 Efficiency η as a function of R_L at fixed values of V_I of the designed boost converter in DCM.

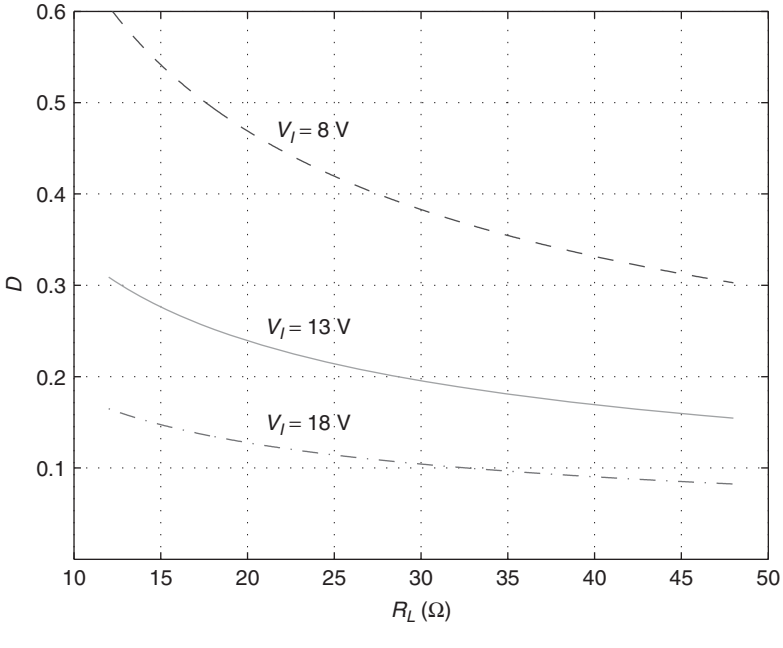


Figure 3.28 Duty cycle D as a function of R_L at fixed values of V_I for DCM at fixed values of V_I.

Example 3.2

A boost converter has the following parameters: $V_I = 10\,\text{V}$, $V_O = 20\,\text{V}$, $P_{Omax} = 40\,\text{W}$, $P_{Omin} = 0$, $r_L = 0.1\,\Omega$, $r_C = 0.1\,\Omega$, $r_{DS} = 0.055\,\Omega$, $C_o = 100\,\text{pF}$, $R_F = 0.025\,\Omega$, $V_F = 0.3\,\text{V}$, $f_s = 50\,\text{kHz}$, and $V_r/V_O \leq 5.5\,\%$. Find component values, component stresses, and the efficiency at full power.

Solution. At full power, the maximum load current for $M_{V\,DC} = 2$ is

$$I_{Omax} = \frac{P_{Omax}}{V_O} = \frac{40}{20} = 2\,\text{A}, \tag{3.183}$$

and the minimum load resistance is

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{20}{2} = 10\,\Omega. \tag{3.184}$$

The dc voltage transfer function is

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{20}{10} = 2. \tag{3.185}$$

Hence, the duty cycle at the CCM/DCM boundary for $M_{V\,DC} = 2$ is

$$D_B = 1 - \frac{1}{M_{V\,DC}} = 1 - \frac{1}{2} = 0.5. \tag{3.186}$$

The maximum inductance required for DCM operation at D_B is

$$L_{max} = \frac{R_{Lmin} D_B (1 - D_B)^2}{2 f_s} = \frac{10 \times 0.5 \times (1 - 0.5)^2}{2 \times 50 \times 10^3} = 12.5\,\mu\text{H}. \tag{3.187}$$

Assuming $D_{max} = 0.4$ at full power, one obtains

$$D_{1min} = \frac{D_{max}}{M_{V\,DC} - 1} = \frac{0.4}{2 - 1} = 0.4 \tag{3.188}$$

and

$$L = \frac{D_{max}^2 R_{Lmin}}{2 f_s M_{V\,DC}(M_{V\,DC} - 1)} = \frac{0.4^2 \times 10}{2 \times 50 \times 10^3 \times 2 \times (2 - 1)} = 8\,\mu\text{H}. \tag{3.189}$$

Thus, $L < L_{max}$.

The maximum peak switch, diode, and inductor current is

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{D_{max} V_I}{f_s L} = \frac{0.4 \times 10}{5 \times 10^4 \times 8 \times 10^{-6}} = 10\,\text{A}. \tag{3.190}$$

The maximum switch and diode voltage stress is

$$V_{SM} = V_{DM} = V_O = 20\,\text{V}. \tag{3.191}$$

The peak-to-peak ripple voltage across $r_C = 0.1\,\Omega$ is

$$V_{rC} = r_C I_{DM} = 0.1 \times 10 = 1\,\text{V}. \tag{3.192}$$

The ripple voltage on the output voltage is

$$V_r = 0.055 V_O = 0.055 \times 20 = 1.1\,\text{V}. \tag{3.193}$$

Thus, the ripple voltage across the filter capacitance C is

$$V_{Cpp} = V_r - V_{rC} = 1.1 - 1 = 0.1\,\text{V}. \tag{3.194}$$

Hence, the minimum capacitance is

$$C_{min} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}} = \frac{0.4 \times 20}{5 \times 10^4 \times 10 \times 0.1} = 160\,\mu\text{F}. \tag{3.195}$$

Pick $C = 220\,\mu\text{F}/0.1\,\Omega/36\,\text{V}$.

The component power losses will be calculated at $V_I = 10\,\text{V}$, $R_{Lmin} = 10\,\Omega$, $P_{Omax} = 40\,\text{W}$, and $I_{Omax} = 2\,\text{A}$. The conduction loss in the power MOSFET is

$$P_{rDS} = \frac{2r_{DS}}{3}\sqrt{\frac{2(M_{V\,DC}-1)^3}{f_s L R_{Lmin} M_{V\,DC}}} P_{Omax}$$

$$= \frac{2 \times 0.055}{3}\sqrt{\frac{2 \times (2-1)^3}{50 \times 10^3 \times 8 \times 10^{-6} \times 10 \times 2}} \times 40 = 0.733\,\text{W}. \tag{3.196}$$

The switching loss is

$$P_{sw} = f_s C_o V_O^2 = 50 \times 10^3 \times 100 \times 10^{-12} \times 20^2 = 2\,\text{mW}. \tag{3.197}$$

The power loss in the diode forward resistance is

$$P_{RF} = \frac{2R_F}{3}\sqrt{\frac{2(M_{V\,DC}-1)}{f_s L R_{Lmin} M_{V\,DC}}} P_{Omax} = \frac{2 \times 0.025}{3}\sqrt{\frac{2 \times (2-1)}{50 \times 10^3 \times 8 \times 10^{-6} \times 10 \times 2}} \times 40$$

$$= 0.333\,\text{W}, \tag{3.198}$$

and the power loss in the diode offset voltage source V_F is

$$P_{VF} = V_F I_{Omax} = 0.3 \times 2 = 0.6\,\text{W}, \tag{3.199}$$

resulting in the diode conduction loss

$$P_D = P_{RF} + P_{VF} = 0.333 + 0.6 = 0.933\,\text{W}. \tag{3.200}$$

The power loss in the inductor is

$$P_{rL} = \frac{2r_L}{3}\sqrt{\frac{2M_{V\,DC}(M_{V\,DC}-1)}{f_s L R_{Lmin}}} P_{Omax} = \frac{2 \times 0.1}{3}\sqrt{\frac{2 \times 2 \times (2-1)}{50 \times 10^3 \times 8 \times 10^{-6} \times 10}} \times 40$$

$$= 2.667\,\text{W}. \tag{3.201}$$

The overall power loss is

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} = 0.733 + 0.002 + 0.933 + 2.667 = 4.335\,\text{W}. \tag{3.202}$$

The efficiency of the converter is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{40}{40 + 4.335} = 90.22\,\%. \tag{3.203}$$

3.4 Bidirectional Buck and Boost Converters

Figure 3.29(a) shows the classical boost converter topology with a negative common rail. In the converter of Figure 3.29(b), the inductor and the diode are moved to the negative rail, resulting in the boost converter topology with a positive common rail. Figure 3.29(c)

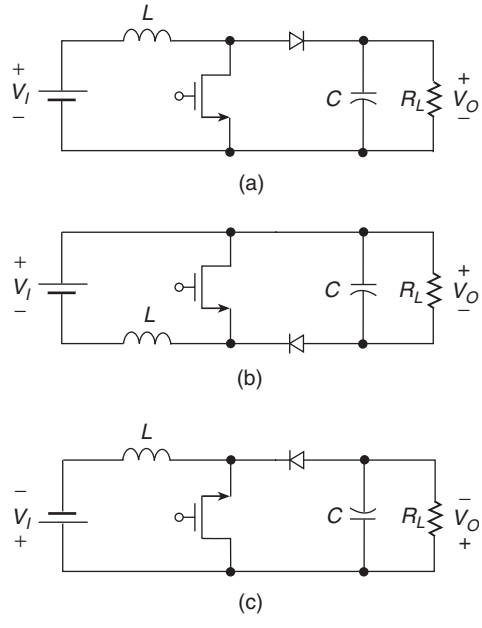


Figure 3.29 Derivation of the boost converter topology with a positive common rail. (a) Boost converter with a negative common rail. (b) Boost converter with the inductor and diode moved to the negative rail. (c) Boost converter with a positive common rail at the bottom.

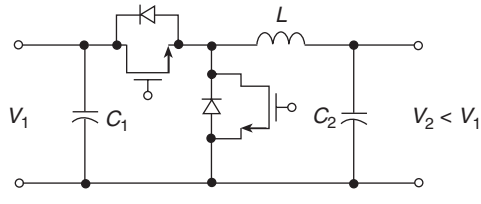


Figure 3.30 Bidirectional buck and boost PWM converters.

shows the boost converter topology of Figure 3.29(b) flipped so that the positive common rail is at the bottom.

A bidirectional buck and boost PWM converter [21] is shown in Figure 3.30. In this circuit, both switches are composed of a transistor and an antiparallel diode. They can conduct current in both directions, but can support the voltage in only one direction. In other words, the switches are bidirectional for the current and unidirectional for the voltage. These are two-quadrant switches, which permit energy flow in both directions, from left to right, and vice versa.

If a dc voltage source V_1 is connected in parallel with the capacitor C_1 and a load is connected in parallel with the capacitor C_2, the buck converter is obtained. In this case, the energy flows from left to right. The horizontal MOSFET channel is used as a controllable switch and its antiparallel diode is permanently OFF, whereas the vertical diode is used as a passive (naturally commutated) switch. The channel of the vertical MOSFET can be held permanently OFF or can be turned on by a driver, when the vertical diode is ON.

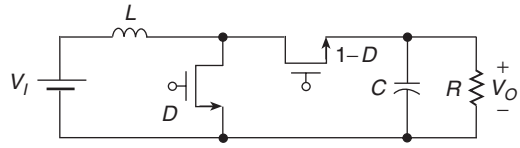


Figure 3.31 Synchronous boost PWM converter.

In contrast, if a dc voltage source V_2 is connected in parallel with the capacitor C_2 and a load is connected in parallel with the capacitor C_1, the boost converter is obtained. Then, the energy flows from right to left. The channel of the vertical MOSFET is used as a controllable switch and its antiparallel diode is always OFF, whereas the horizontal diode is used as a passive switch. The channel of the horizontal MOSFET can be kept in the off-state during the whole cycle, or it can be turned on when the horizontal diode is ON. Figure 3.31 shows a synchronous boost converter.

3.5 Tapped-inductor Boost Converters

A tapped-inductor common-transistor boost converter [21] is shown in Figure 3.32(a). It is a high step-up converter. The voltage transfer function of the tapped inductor is

$$n = \frac{v}{v_p} = \frac{N_p + N_s}{N_p} = 1 + \frac{N_s}{N_p}. \tag{3.204}$$

When the MOSFET is ON and the diode is OFF,

$$v_p = V_I. \tag{3.205}$$

When the MOSFET is OFF and the diode is ON,

$$v = V_I - V_O = nv_p, \tag{3.206}$$

resulting in

$$v_p = \frac{V_I - V_O}{n}. \tag{3.207}$$

Using the volt-second balance for the N_p winding across which the voltage is v_S,

$$V_I DT = -\frac{V_I - V_O}{n}(1 - D)T. \tag{3.208}$$

Hence, the dc voltage transfer function of the tapped-inductor common-transistor configuration operating in CCM is given by

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{nD}{1 - D} + 1. \tag{3.209}$$

Plots of $M_{V\,DC}$ as a function of D for CCM are shown in Figure 3.33. The magnetizing inductance L_m on the terminals of the winding N_p is given by

$$L_m = \left(\frac{N_p}{N_p + N_s}\right)^2 L, \tag{3.210}$$

where L is the total inductance of winding $L_p + L_s$.

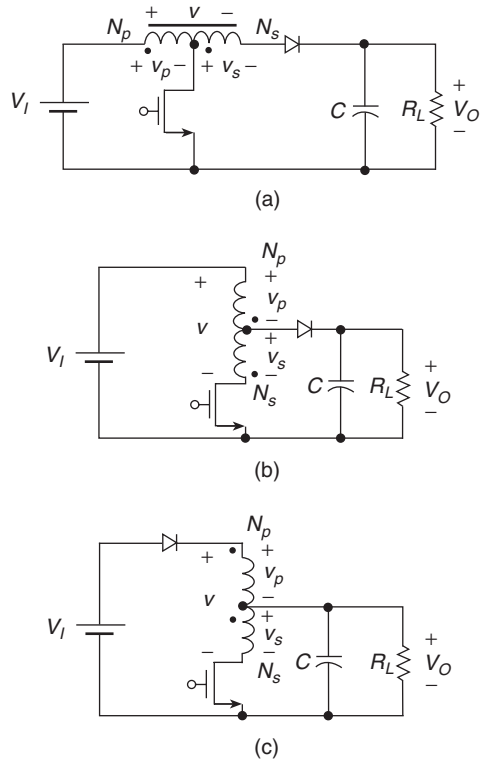


Figure 3.32 Tapped-inductor boost converters. (a) Tapped-inductor common-transistor boost converter. (b) Tapped-inductor common-diode boost converter. (c) Tapped-inductor common-load boost converter.

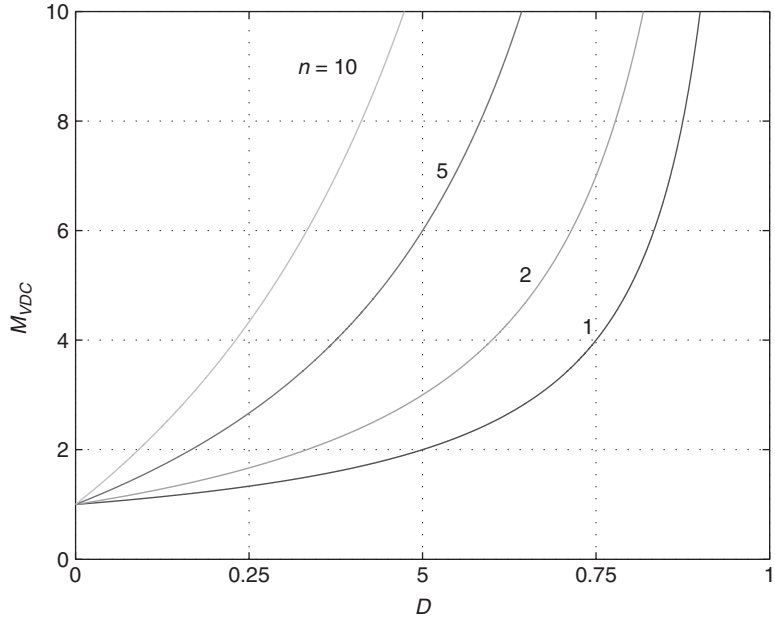


Figure 3.33 DC voltage transfer function of tapped-inductor common-transistor boost converter for CCM.

3.5.1 Tapped-inductor Common-diode Boost Converter

A tapped-inductor common-diode boost converter is shown in Figure 3.32(b). When the MOSFET is OFF and the diode is ON,

$$v = V_I = nv_p \tag{3.211}$$

resulting in

$$v_p = \frac{V_I}{n}. \tag{3.212}$$

When the MOSFET is OFF and the diode is ON,

$$v_p = V_I - V_O. \tag{3.213}$$

Using the volt-second balance for the inductance L_p across which the voltage is v_p,

$$\frac{V_I}{n}DT = (V_O - V_I)(1 - D)T, \tag{3.214}$$

we obtain the dc voltage transfer function of the tapped-inductor common-diode in CCM,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{n(1 - D)} + 1. \tag{3.215}$$

Figure 3.34 shows plots of $M_{V\,DC}$ as a function of D for CCM.

3.5.2 Tapped-inductor Common-load Boost Converter

A tapped-inductor common-load boost converter is shown in Figure 3.32(c). It is an inverse Watkins–Johnson converter [28]. When the MOSFET is ON and the diode is OFF,

$$v_p = V_I - V_O = \frac{v}{n} \tag{3.216}$$

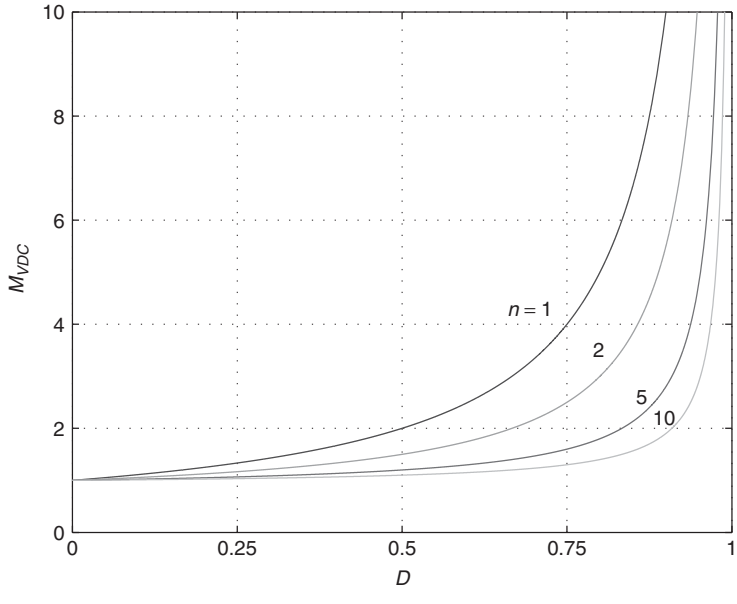


Figure 3.34 DC voltage transfer function of tapped-inductor common-diode boost converter for CCM.

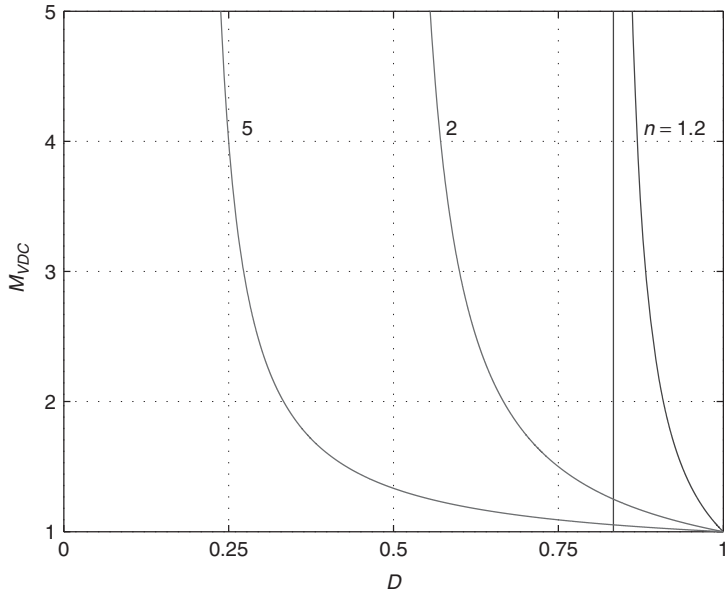


Figure 3.35 DC voltage transfer function of tapped-inductor common-load inverse Watkins–Johnson boost converter for CCM.

resulting in

$$v = nv_p = n(V_I - V_O). \tag{3.217}$$

When the MOSFET is OFF and the diode is ON,

$$v_s = V_O = v - v_p = v - \frac{v}{n} = v\frac{n-1}{n}, \tag{3.218}$$

leading to

$$v = V_O\frac{n}{n-1}. \tag{3.219}$$

Applying the volt-second balance,

$$n(V_I - V_O)DT = -V_O\frac{n}{n-1}(1-D)T. \tag{3.220}$$

Hence, we obtain the dc voltage transfer function of the tapped-inductor common-load boost converter

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D(n-1)}{nD-1}, \quad \text{for } D > \frac{1}{n}. \tag{3.221}$$

Plots of $M_{V\,DC}$ as a function of D for the tapped-inductor common-diode boost converter operating in CCM are shown in Figure 3.35.

3.6 Duality

In order to use the duality principles for dc–dc converters, it is useful to introduce the following simplifications:

1. An inductor in series with a parallel combination of filter capacitor and a load resistance (or an inductor in series with a load resistance) can be replaced by a dc current sink.

2. A filter capacitor in parallel with a resistor can be replaced by a voltage source.
3. A dc source in series with an inductor can be replaced by a dc current source.

The duality principles for dc–dc converter are as follows:

1. Replace a dc voltage source by a dc current source.
2. Replace a series switch by a parallel switch, and vice versa.
3. Replace a parallel diode by a series diode, and vice versa.
4. Replace a dc current sink by a dc voltage source.
5. Replace a dc voltage sink by a dc current source.
6. Replace the on-duty cycle D by the off-duty cycle $D' = 1 - D$.

Figure 3.36 shows the derivation of the boost converter from the buck converter, or vice versa, using the duality principles.

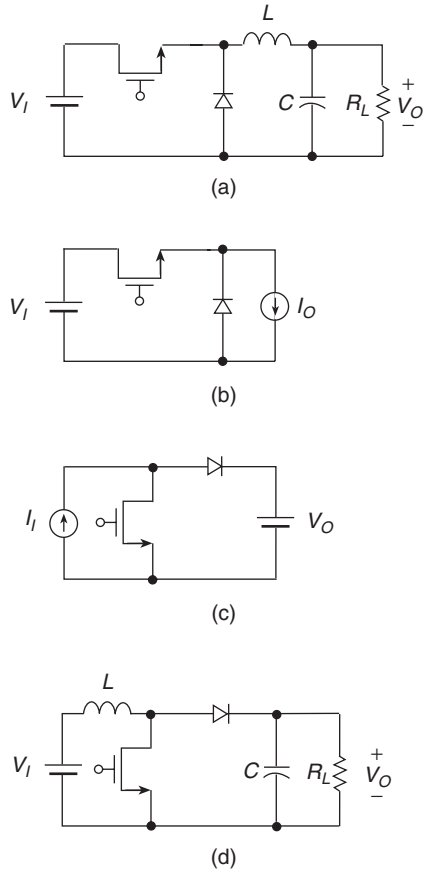


Figure 3.36 Derivation of the boost converter from the buck converter, or vice versa, using the duality principles.

3.7 Power Factor Correction

3.7.1 Power Factor

The *power factor* describes the effectiveness of energy transmission from a source to a load. The loads can be nonlinear and reactive. Nonlinear loads generate current harmonics, which are injected into the utility power system, degrading it. Reactive components of the load impedance cause a phase shift between current and voltage. Universal ac–dc power supplies of electronic systems should be designed to accept any level of utility voltage used in the world, which range from 92 to 264 Vrms. A low utility line voltage in the US is 92 Vrms and a high utility line voltage in Europe is 264 Vrms. Universal power supplies must satisfy the IEC555-2 line harmonic standard and the VDE 0871B conducted emission standard.

Conventional peak rectifiers contain a large output filter capacitor. The diodes in these rectifiers conduct current for a very short portion of a cycle. The conduction angle of the diode current is very small because the filter capacitor remains charged at or near the peak ac voltage during each cycle. As a result, the rectifier diodes are reverse biased most of the time and no current flows. The unidirectional diode currents are reflected to the input of the front-end rectifier and form the line current waveform i_s composed of very narrow positive and negative pulses, as shown in Figure 3.37. Therefore, the input current waveform of peak rectifiers with capacitive filters consists of haversine pulses and contains a lot of harmonics, resulting in a very low power factor.

The power factor is defined as

$$PF = \frac{P}{|S|} = \frac{\text{Real power}}{\text{Apparent power}} = \frac{\text{Average power}}{(\text{RMS current})(\text{RMS voltage})} = \frac{\sum_{n=1}^{\infty} P_n}{I_{rms} V_{rms}}$$

$$= \frac{\sum_{n=1}^{\infty} I_{rms(n)} V_{rms(n)} \cos \phi_n}{\sqrt{\sum_{n=1}^{\infty} I_{rms(n)}^2 \sum_{n=1}^{\infty} V_{rms(n)}^2}}, \tag{3.222}$$

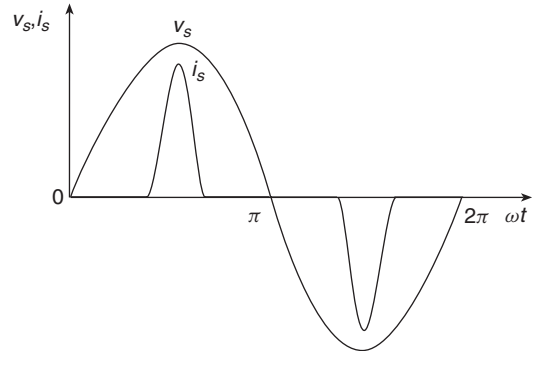


Figure 3.37 Line voltage and current loaded by a full-wave peak rectifier.

where the real power, called the average power or the time average power, is given by

$$P = \frac{1}{2\pi}\int_0^{2\pi} pd(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} vid(\omega t) \quad \text{(W)} \tag{3.223}$$

and the apparent power is

$$|S| = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v^2 d(\omega t)}\sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)} = V_{rms}I_{rms} \quad \text{(VA)}. \tag{3.224}$$

Here $p = vi$ is the instantaneous power, and $\mathbf{S} = \mathbf{VI}^* = |S|e^{\phi}$ is the complex power.

Let us assume that the utility line voltage is purely sinusoidal,

$$v_s = \sqrt{2}V_{rms1}\sin\,\omega t. \tag{3.225}$$

In general, the utility line current is not sinusoidal and can be represented by a Fourier series,

$$i_s = \sqrt{2}I_{rms1}\sin\,(\omega t + \phi_1) + \sqrt{2}I_{rms2}\sin\,(2\omega t + \phi_2) + \sqrt{2}I_{rms3}\sin\,(3\omega t + \phi_3)\ldots. \tag{3.226}$$

The rms value of the line ac current is

$$I_{rms} = \sqrt{I_{rms1}^2 + I_{rms2}^2 + I_{rms3}^2 + \cdots}. \tag{3.227}$$

The *total harmonic distortion* is defined by

$$THD = \frac{\sqrt{I_{rms2}^2 + I_{rms3}^2 + I_{rms4}^2 + \cdots}}{I_{rms1}}. \tag{3.228}$$

The power factor for a sinusoidal voltage and a nonsinusoidal current is defined as

$$\begin{aligned} PF &= \frac{P}{V_{rms}I_{rms}} = \frac{V_{rms1}I_{rms1}\cos\,\phi_1}{V_{rms_1}I_{rms}} = \frac{I_{rms1}}{I_{rms}}\cos\,\phi_1 \\ &= \frac{I_{rms1}}{\sqrt{I_{rms1}^2 + I_{rms2}^2 + I_{rms3}^2 + \cdots}}\cos\,\phi_1 = \frac{1}{\sqrt{1 + THD^2}}\cos\,\phi_1 = F_{DF}F_{DA}, \end{aligned} \tag{3.229}$$

where the *distortion factor* or the *current distortion factor* is

$$F_{DF} = \frac{I_{rms1}}{I_{rms}} = \frac{1}{\sqrt{1 + THD^2}} \tag{3.230}$$

and the *displacement angle* or the *displacement factor* is

$$F_{DA} = \cos\,\phi_1. \tag{3.231}$$

The distortion factor F_{DF} as a function of THD is shown in Figure 3.38. Usually, for line rectifiers, $\phi_1 = 0$ and the power factor becomes

$$PF = \frac{I_{rms1}}{I_{rms}} = \frac{I_{rms1}}{\sqrt{I_{rms1}^2 + I_{rms2}^2 + I_{rms3}^2 + \cdots}} = \frac{1}{\sqrt{1 + THD^2}}. \tag{3.232}$$

PF ranges from 0 to 1. For perfect energy transmission from a source to a load, a unity power factor ($PF = 1$) is required. In this case, the load presented by an electric current to the utility line behaves like a linear resistance. When the rms values of current harmonics are zero, $THD = 0$ and $PF = 1$ (at $\cos\,\phi_1 = 1$). The total harmonic distortion THD in terms of the power factor PF is

$$THD = \sqrt{\frac{1}{PF^2} - 1}. \tag{3.233}$$

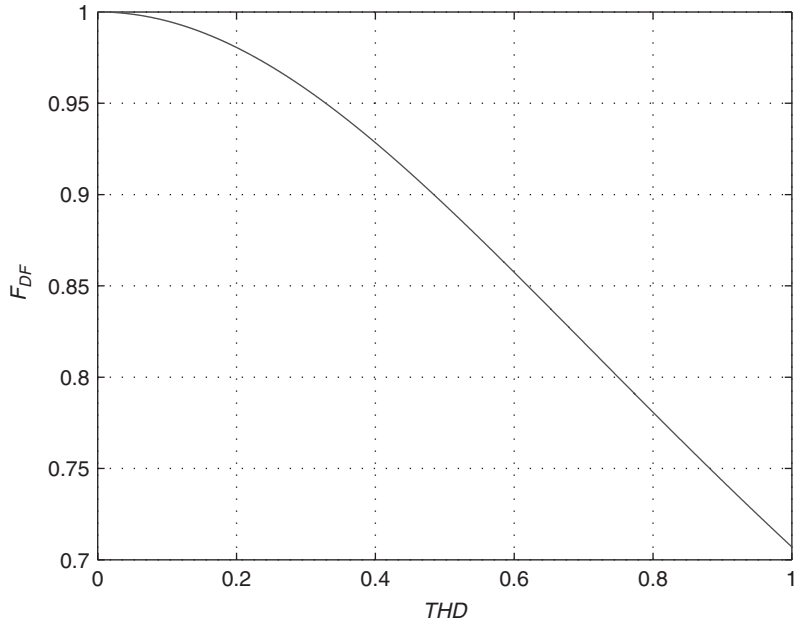


Figure 3.38 Distortion factor F_{DF} as a function of *THD*.

The rms value of input current of an ac–dc power converter with output power P_O and efficiency η is

$$I_{rms} = \frac{P_O}{V_{rms}\eta PF}. \tag{3.234}$$

As off-line ac–dc converters deliver increasing amounts of power, power factor correction (PFC) becomes of great interest to both manufacturers and users. The line current, although in phase with the ac line voltage, is often nonsinusoidal with high peak values, placing high stress on circuit breakers, fuses, wall sockets, installation wires, and transformers. Since wall sockets are being pushed to their limit, safety becomes an important issue. In the US, a typical office has a 15 A/110 V wall plug, which cannot be run at more than 80 % of its rating. The maximum current drawn form the line is 12 Arms. Line voltages sag and become distorted. Also, there is an increased power loss in the transmission line resistance because a larger rms current is required for a given real power P at $PF < 1$. Since power companies want to minimize the power loss in the transmission lines, they want customers to have a power factor as close to 1 as possible. For this reason, they will provide penalties or price incentives to encourage users to reduce the cost of energy transmission. A typical value of the power factor for single-phase 110/220 Vrms lines is 0.65, but it can go as low as 0.49, depending on the front-end rectifier and the line impedance, which ranges from 0.1 to 1.5 Ω. The apparent power becomes much larger than the real power when the power factor is poor. Rising power quality requirements and the proliferation of electronic equipment are demanding that off-line converters incorporate PFC. There are passive and active power factor correctors. Passive PFCs use a large input choke. If a choke inductance is large enough, a PFC of 0.9 is possible. However, such chokes tend to be very large and heavy, reducing the power density.

3.7.2 Boost Power Factor Corrector

The circuit of a single-phase boost power factor corrector is depicted in Figure 3.39. It consists of a front-end rectifier and a boost PWM dc–dc converter. The rectifier does not contain a large filter capacitor to reduce the line-frequency voltage ripple. It usually contains a small filter capacitor at the output to reduced a switching-frequency current component generated by the boost converter. Current and voltage waveforms in the boost power factor corrector are shown in Figure 3.40. The rectifier output voltage $|v_s|$ is a full-wave rectified sinusoid. The minimum value of the peak rectified voltage for the low US utility line is

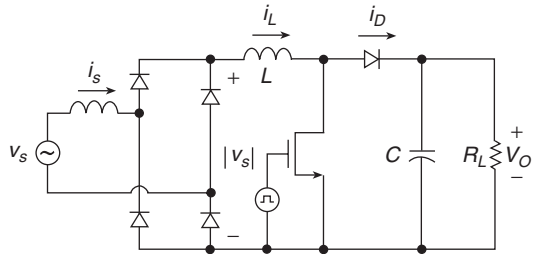


Figure 3.39 Boost power factor corrector.

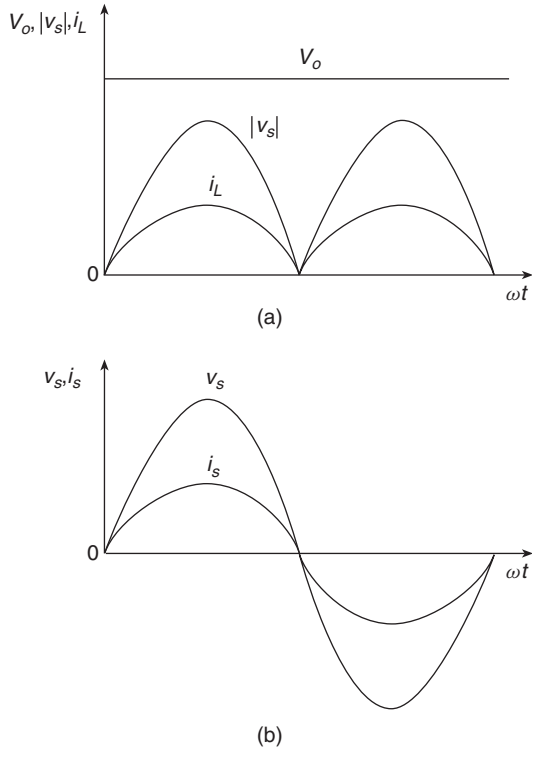


Figure 3.40 Waveforms in the boost power factor corrector for a cycle of the line frequency. (a) Waveforms of the rectified line voltage $|v_s|$, output voltage V_O, and inductor current i_L. (b) Waveform of the line voltage v_s and line current i_s.

$V_{pk(min)} = \sqrt{2} \times 92 = 130\,\text{V}$ and the maximum value of the peak rectified voltage for the high European utility line is $V_{pk(max)} = \sqrt{2} \times 264 = 373\,\text{V}$. The time-dependent rectified voltage $|v_s|$ is converted into a dc voltage V_O. A control circuit forces the inductor current i_L of the boost converter to follow a full-wave rectified sinusoidal reference voltage $|v_s|$. Since the boost converter is a step-up converter, the output voltage V_O must be higher than the maximum value of the voltage $|v_s|$, that is, $V_O > 373\,\text{V}$. Various dc voltages are derived from the dc voltage V_O, using dc–dc converters.

The line voltage is sinusoidal and given by

$$v_s = V_m \sin\,\omega t. \tag{3.235}$$

The voltage at the output of the front-end rectifier is

$$|v_s| = V_m |\sin\,\omega t|. \tag{3.236}$$

The duty cycle is

$$M(t) = \frac{V_O}{|v_s|} = \frac{V_O}{V_m |\sin\,\omega t|} = \frac{1}{1 - D(t)}, \tag{3.237}$$

resulting in the duty cycle

$$D(t) = 1 - \frac{|v_s|}{V_O} = 1 - \frac{V_m |\sin\,\omega t|}{V_O}. \tag{3.238}$$

The maximum value of the duty cycle is 1 and occurs at $\omega t = 0, \pi$, and 2π. The minimum value of the duty cycle is $D_{min} = 1 - V_{sm}/V_O$ and occurs at $\omega t = \pi/2$ and $3\pi/2$. The inductor current is shaped to have a full-wave rectified waveform,

$$i_L = I_{Lm} |\sin\,\omega t|. \tag{3.239}$$

The input current of the rectifier is

$$i_s = I_{sm} \sin\,\omega t = I_{Lm} \sin\,\omega t. \tag{3.240}$$

Thus, the input impedance of the boost converter at the utility line frequency is a linear resistance, yielding $THD = 0$ and $F_{DF} = 1$. The line current is in phase with the line voltage, yielding $F_{DA} = \cos\,\phi_1 = 1$. Thus, $PF = 1$.

The diode current is

$$i_D = [1 - D(t)] i_L = \left[1 - 1 + \frac{V_{sm} |\sin\,\omega t|}{V_O}\right] I_{Lm} |\sin\,\omega t| = \frac{V_{sm} I_{Lm}}{V_O} \sin^2\,\omega t. \tag{3.241}$$

Since

$$\sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos\,2\omega t, \tag{3.242}$$

we obtain

$$i_D = \frac{1}{2} \frac{V_{sm} I_{Lm}}{V_O} - \frac{1}{2} \frac{V_{sm} I_{Lm}}{V_O} \cos\,2\omega t = \frac{1}{2} \frac{V_{sm} I_{sm}}{V_O} - \frac{1}{2} \frac{V_{sm} I_{sm}}{V_O} \cos\,2\omega t = I_D - i_d. \tag{3.243}$$

The dc component of the diode current I_D flows through the load and nearly all of the second harmonic of the diode current i_d flows through the output filter capacitor C. The ac component of the voltage across the filter capacitor is

$$\begin{aligned} v_{AC} &= \frac{1}{\omega C} \int_0^{\omega t} i_d\, d(\omega t) = -\frac{1}{2} \frac{V_{sm} I_{Lm}}{\omega C V_O} \int_0^{\omega t} \cos\,2\omega t d(\omega t) \\ &= -\frac{V_{sm} I_{Lm}}{4\omega C V_O} \sin\,2\omega t = -V_{Cm(AC)} \sin\,2\omega t, \end{aligned} \tag{3.244}$$

where amplitude of the second harmonic of the output voltage is

$$V_{Cm(AC)} = \frac{V_{sm}I_{Lm}}{4\omega CV_O} = \frac{V_{sm}I_{sm}}{4\omega CV_O}. \tag{3.245}$$

Hence, the filter capacitance is

$$C_{min} = \frac{V_{sm}I_{sm}}{4\omega V_O V_{Cm(AC)}} = \frac{P_{s(max)}}{2\omega V_O V_{Cm(AC)}}, \tag{3.246}$$

where the maximum power drawn from the line is

$$P_{s(max)} = \tfrac{1}{2}V_{sm}I_{sm}. \tag{3.247}$$

The boost active power factor corrector is widely used in electronic ballasts for fluorescent lamps, shown in Figure 3.41 [29]. Active power factor correctors are commonly used in many applications, such as switch-mode power supplies (SMPS).

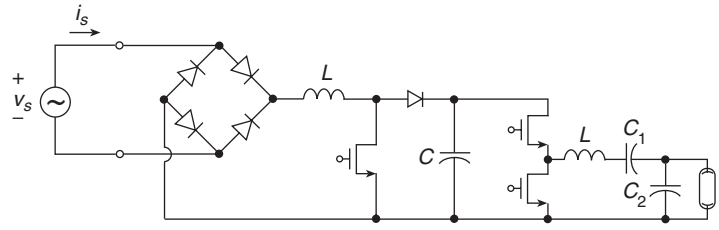


Figure 3.41 Electronic ballast with boost active power factor corrector for fluorescent lamps [29].

3.8 Summary

- The boost converter is a step-up circuit.
- It has only a transformerless version.
- It can be operated in either CCM or DCM.
- Its advantage is that the input current has a continuous (nonpulsating) waveform.
- It is easy to drive the MOSFET in the boost converter because the gate is referenced to ground.
- If losses are neglected, the dc voltage transfer function for CCM is $M_{V\,DC} = V_O/V_I = 1/(1-D)$. It increases from 1 to ∞ as D is increased from 0 to 1.
- The dc voltage transfer function of the lossy converter is lower than that of the lossless converter at the same duty cycle D. The difference is especially significant at the duty cycle D close to 1.
- As D is increased from 0 to 1, the dc voltage transfer function of the lossy boost converter initially increases, reaches its maximum value, and then decreases back to 0.
- The converter should not be used at D close to 1 because of its poor efficiency.
- The peak-to-peak current through the filter capacitor is very high; it is equal to the peak-to-peak value of the diode current I_{DM}.
- It is easy to drive the MOSFET because the gate is referenced to ground.

- The dc voltage transfer function $M_{V\,DC}$ depends on the inductance L for DCM, and it is independent of L for CCM.
- For the boost converter operating in CCM, the maximum efficiency occurs at full load I_{Omax} (or R_{Lmin}).
- For the boost converter operating in CCM, the minimum efficiency occurs at full load I_{Omax} (or R_{Lmin}) and at the minimum dc input voltage V_{Imin}.

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3.10 Review Questions

3.1 What is the range of the dc voltage transfer function for the lossless and lossy boost PWM converter?

3.2 How does the efficiency of the boost converter depend on the duty cycle?

3.3 Is it easy to obtain a low ripple voltage in the boost PWM converter?

3.4 Is the current flowing into the filter capacitor and the load continuous in the boost PWM converter?

3.5 Is the input current of the boost PWM converter pulsating?

3.6 Are both halves of the $B-H$ curve of the inductor core used in the boost PWM converter?

3.7 Is the corner frequency f_o dependent on the load resistance R_L in the boost converter?

3.8 Is the efficiency high at heavy or light loads for the boost converter?

3.11 Problems

3.1 Derive an expression for the dc voltage transfer function $M_{V\,DC}$ of a lossless boost converter using the steady-state condition for the inductor current.

3.2 A boost PWM converter has the following data: $V_I = 125$ to $350\,\text{V}$, $V_O = 380\,\text{V}$, $P_O = 6.8$ to $68\,\text{W}$, and $f_s = 50\,\text{kHz}$. Compute the voltage and current stresses of the transistor and the diode.

3.3 A boost PWM converter has the following data: $V_I = 8$ to $16\,\text{V}$, $V_O = 24\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, and $f_s = 200\,\text{kHz}$. Calculate the minimum inductance required for the converter to operate in CCM. Assume $\eta = 90\,\%$.

3.4 A boost PWM converter has the following data: $V_I = 8$ to $12\,\text{V}$, $V_O = 24\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, and $f_s = 200\,\text{kHz}$. Calculate the minimum inductance required for the converter to operate in CCM. Assume $\eta = 90\,\%$.

3.5 A boost PWM converter is operated in CCM at $V_I = 14\,\text{V}$ and $V_O = 28\,\text{V}$. Find the required duty cycle D for the converter efficiency (a) $\eta = 100\,\%$ and (b) $\eta = 80\,\%$.

3.6 A boost PWM converter employs a power MOSFET with an on-resistance $r_{DS} = 0.02\,\Omega$. The load current is $I_O = 10\,\text{A}$. Calculate the transistor conduction loss at $D = 0.1$, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, and 0.9.

3.7 A boost PWM converter employs a diode with a forward resistance $R_F = 0.02\,\Omega$. The load current is $I_O = 10\,\text{A}$. Calculate the diode conduction loss due to the forward resistance R_F at $D = 0.1$, 0.2, 0.5, 0.8, and 0.9.

3.8 A boost PWM converter employs an inductor with a dc resistance $r_L = 0.02\,\Omega$. The load current is $I_O = 10\,\text{A}$. Calculate the inductor loss at $D = 0.1$, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, and 0.9.

3.9 For the boost converter with $V_I = 8$ to $16\,\text{V}$, $V_O = 24\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, and $f_s = 200\,\text{kHz}$, find the maximum inductance required to maintain the converter in DCM.

3.10 Design a boost PWM converter with the following specifications: $V_{Imin} = 90\sqrt{2}\,\text{V}$, $V_{Imax} = 240\sqrt{2}\,\text{V}$, $V_O = 400\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, $V_r/V_O \leq 1\,\%$, $r_L = 2.5\,\Omega$, $r_{DS} = 1\,\Omega$, $C_o = 100\,\text{pF}$, $R_F = 25\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, $r_C = 50\,\text{m}\Omega$, and $f_s = 50\,\text{kHz}$. Find L, C, and η.

3.11 Design a boost PWM converter to meet the following specifications: $V_{Imin} = 25\,\text{V}$, $V_{Inom} = 28\,\text{V}$, $V_{Imax} = 31\,\text{V}$, $V_O = 270\,\text{V}$, $R_{Lmin} = 462\,\Omega$, $R_{Lmax} = 518\,\Omega$, $f_s = 25\,\text{kHz}$, $V_r/V_O \leq 1\,\%$, $V_F = 1.5\,\text{V}$, $R_F = 0.188\,\Omega$, $r_{DS} = 0.3\,\Omega$, $C_o = 400\,\text{pF}$, $r_L = 0.21\,\Omega$, and $r_C = 0.1\,\Omega$. Find L, C, I_{SM}, V_{SM}, and η.

3.12 Design a boost converter to meet the following specifications: $V_I = 24 \pm 4\,\text{V}$, $V_O = 48\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, $V_r/V_O \leq 1\,\%$, $f_s = 100\,\text{kHz}$, $r_{DS} = 0.2\,\Omega$, $r_{L(dc)} = 0.25\,\Omega$, $R_F = r_C = 25\,\text{m}\Omega$, $V_F = 0.8\,\text{V}$, and $C_o = 250\,\text{pF}$. Find L, C, I_{SM}, V_{SM}, and η.

3.13 Design a boost converter to meet the following specifications: $V_I = 10$ to $24\,\text{V}$, $V_O = 28\,\text{V}$, $I_O = 0.5$ to $1\,\text{A}$, $V_r/V_O \leq 1\,\%$, $f_s = 100\,\text{kHz}$, $r_{DS} = 0.2\,\Omega$, $r_{L(dc)} = 0.11\,\Omega$, $r_C = 25\,\text{m}\Omega$, $R_F = 25\,\text{m}\Omega$, $V_F = 0.3\,\text{V}$, and $C_o = 150\,\text{pF}$. Find L, C, I_{SM}, V_{SM}, and η.

3.14 Design a boost converter to meet the following specifications: V_I is the US single-phase rectified utility line, $V_O = 400\,\text{V}$, $I_O = 0$ to $0.225\,\text{A}$, $V_r/V_O \leq 1\,\%$, $f_s = 100\,\text{kHz}$, $r_{DS} = 1\,\Omega$, $C_o = 150\,\text{pF}$, $Q_g = 27\,\text{nC}$, $r_L = 2.1\,\Omega$, $r_C = 0.25\,\Omega$, $R_F = 17.1\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and $C_o = 150\,\text{pF}$. Find L, C, I_{SM}, V_{SM}, and η.

4

Buck-boost PWM DC–DC Converter

4.1 Introduction

This chapter covers the buck-boost PWM switching-mode converter [1]–[27]. The circuit of the converter is described. The current and voltage waveforms for various components are derived. The device stresses are found. The dc voltage transfer function is determined. An expression for the minimum inductance is derived from the condition for the CCM/DCM boundary. A design equation for the filter capacitor is developed from the ripple voltage requirement. Power losses in all devices and the overall efficiency are estimated. Illustrative design examples are given for both CCM and DCM. Finally, the buck-boost converter is derived from the buck and boost converters.

4.2 DC Analysis of PWM Buck-boost Converter for CCM

4.2.1 Circuit Description

The circuit of the PWM buck-boost dc–dc converter [1]–[27] is shown in Figure 4.1(a). It consists of a power MOSFET used as a controllable switch, an inductor L, a diode, a filter capacitor C, and a load resistor R_L. The switch is turned on and off at the switching frequency $f_s = 1/T$ with the ON duty ratio $D = t_{on}/T$, where t_{on} is the time interval when the switch is ON. It is difficult to drive the transistor because source is not connected to ground. Therefore, the driver is floating as neither end is connected to ground.

Two modes of operation exist: CCM and DCM. Figure 4.1(b)–(c) shows equivalent circuits of the buck-boost converter for CCM when the switch is ON and the diode is OFF, and when the switch is OFF and the diode is ON, respectively. The principle of operation

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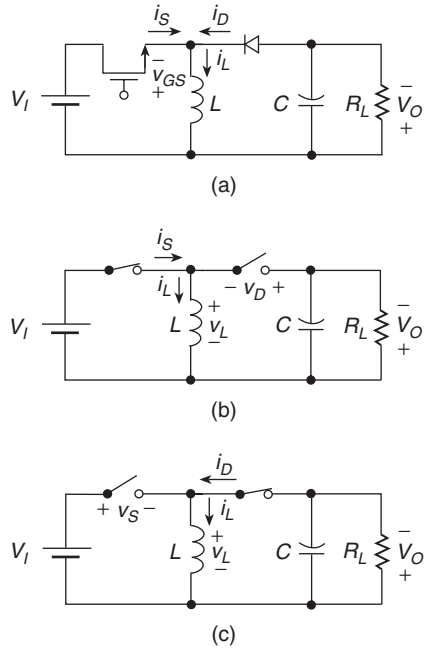


Figure 4.1 PWM buck-boost converter and its ideal equivalent circuits for CCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON.

of the buck-boost converter is explained by the idealized waveforms of the currents and voltages shown in Figure 4.2. During the time interval $0 < t \leq DT$, the switch is ON and the diode is OFF as indicated in Figure 4.1(b). The voltage across the diode is $-(V_I + V_O)$ and maintains the diode in the off-state. The voltage across the inductor is V_I and gives rise to a linear increase in the inductor current with a slope of V_I/L. During the time interval $DT < t \leq T$, the switch is OFF and the diode is ON as shown in Figure 4.1(c). The voltage across the inductor is $-V_O$ and causes the inductor current to decrease linearly with a slope of $-V_O/L$. The voltage across the switch is $V_I + V_O$. At time $t = T$, the switch is turned on again and the next cycle begins.

4.2.2 Assumptions

The analysis of the buck-boost PWM converter of Figure 4.1(a) is based on the following assumptions:

1. The power MOSFET and the diode are ideal switches.
2. The transistor output capacitance and the diode capacitance as well as lead inductances (and thus switching losses) are zero.
3. Passive components are linear, time-invariant, and frequency-independent.
4. The output impedance of the input voltage source V_I is zero for both dc and ac components.

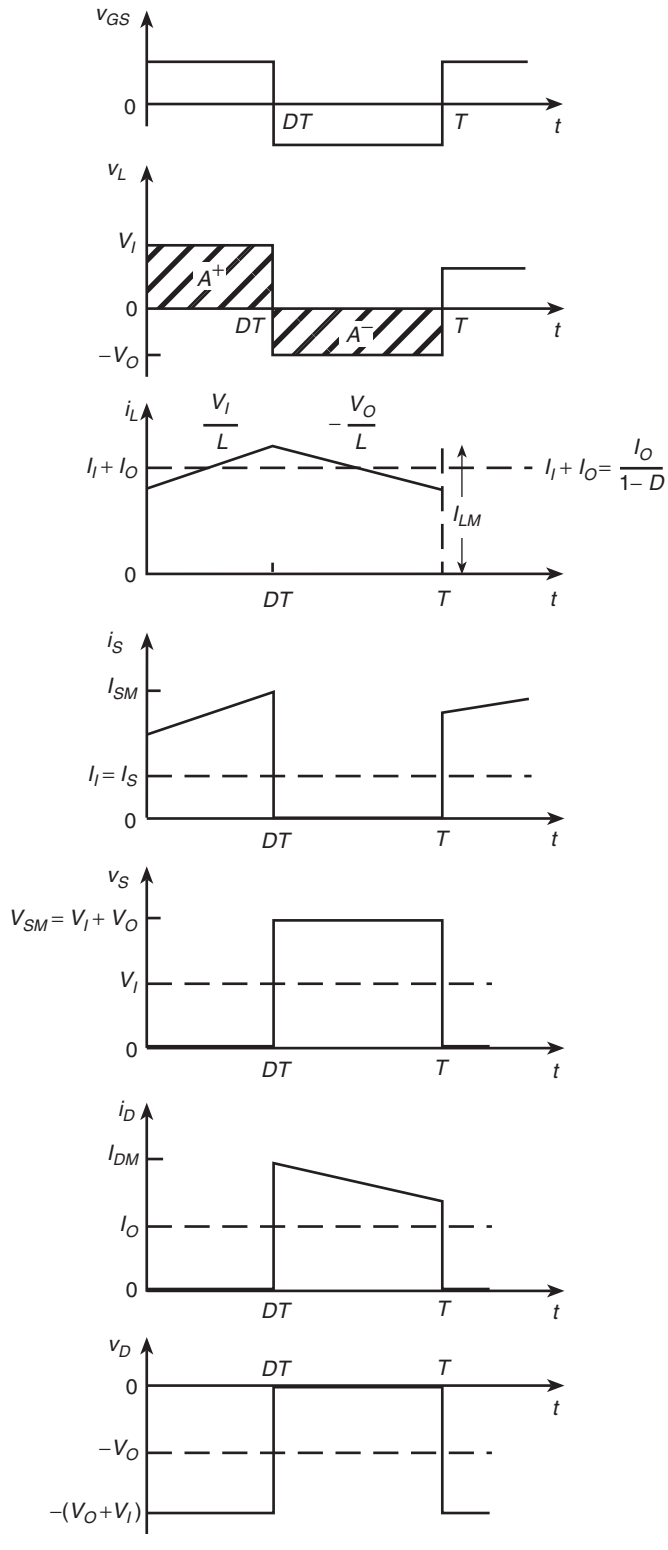


Figure 4.2 Idealized current and voltage waveforms for the PWM buck-boost converter for CCM.

4.2.3 Time Interval $0 < t \leq DT$

During the time interval $0 < t \leq DT$, the switch is ON and the diode is OFF. An ideal equivalent circuit for this time interval is shown in Figure 4.1(b). When the switch is ON, the voltage across the diode v_D is approximately equal to $-(V_I + V_O)$, causing the diode to be reverse biased. The voltage across the switch v_S and the diode current i_D are zero. The voltage across the inductor L is given by

$$v_L = V_I = L\frac{di_L}{dt}. \tag{4.1}$$

Hence, one obtains the current through the inductor L and the switch,

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\,dt + i_L(0) = \frac{1}{L}\int_0^t V_I\,dt + i_L(0) = \frac{V_I}{L}t + i_L(0), \tag{4.2}$$

where $i_L(0)$ is the initial current in the inductor L at time $t = 0$. The peak inductor current becomes

$$i_L(DT) = \frac{V_I DT}{L} + i_L(0) = \frac{V_I D}{f_s L} + i_L(0), \tag{4.3}$$

and the peak-to-peak value of the ripple current through the inductor L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_I DT}{L} = \frac{V_I D}{f_s L}. \tag{4.4}$$

It will shortly be shown that the dc voltage transfer function is $M_{V\,DC} = V_O/V_I = I_I/I_O = D/(1-D)$. Hence, we can find the diode voltage

$$v_D = -(V_I + V_O) = -V_O\left(\frac{1}{M_{V\,DC}} + 1\right) = -\frac{V_O}{D}. \tag{4.5}$$

The average value of the inductor current I_L is equal to the sum of the dc input current I_I and the dc output current I_O. Hence, one arrives at the peak value of the switch current

$$I_{SM} = I_{L(peak)} = I_I + I_O + \frac{\Delta i_L}{2} = \frac{I_O}{1-D} + \frac{\Delta i_L}{2}. \tag{4.6}$$

The increase in the magnetic energy tored in the inductor L is

$$\Delta W_{L(in)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(0)]. \tag{4.7}$$

This time interval is terminated at $t = DT$ when the switch is turned off by an external driver. The inductor current i_L is a continuous function of time. Since $i_L(DT)$ is nonzero when the switch turns on, the inductor acts as a current source, thus turning the diode on.

4.2.4 Time Interval $DT < t \leq T$

During the time interval $DT < t \leq T$, the switch is OFF and the diode is ON. Figure 4.1(c) shows an ideal equivalent circuit for this time interval. The switch current i_S and the diode voltage v_D are zero. The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}. \tag{4.8}$$

Hence, one obtains the current through the inductor L and the diode

$$i_D = i_L = \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t} (-V_O)\,dt + i_L(DT)$$
$$= -\frac{V_O}{L}(t - DT) + i_L(DT) = -\frac{V_O}{L}(t - DT) + \frac{V_I D}{f_s L} + i_L(0), \tag{4.9}$$

where $i_L(DT)$ is the initial current of the inductor L at $t = DT$. The peak-to-peak value of the ripple current through the inductor L is

$$\Delta i_L = i_L(DT) - i_L(T) = \frac{V_O T(1 - D)}{L} = \frac{V_O(1 - D)}{f_s L}. \tag{4.10}$$

Since $V_O/V_I = D/(1 - D)$, the voltage across the switch is given by

$$v_S = V_{SM} = V_I + V_O = \frac{V_O}{D}, \tag{4.11}$$

resulting in a maximum value of the peak voltage across the switch and the diode

$$V_{SMmax} = V_{DMmax} = V_{Imax} + V_O = \frac{V_O}{D_{min}}. \tag{4.12}$$

The peak diode and switch currents are

$$I_{DM} = I_{L(peak)} = I_I + I_O + \frac{\Delta i_L}{2} = \frac{I_O}{1 - D} + \frac{\Delta i_L}{2}. \tag{4.13}$$

The maximum values of the peak currents are

$$I_{DMmax} = I_{SMmax} \approx I_{Imax} + I_{Omax} + \frac{\Delta i_{Lmax}}{2} = \frac{I_{Omax}}{1 - D_{max}} + \frac{\Delta i_{Lmax}}{2}. \tag{4.14}$$

Note that the maximum dc input current occurs at D_{max}, whereas the maximum peak-to-peak ripple current of the inductor occurs at D_{min}. The OFF time interval ends at $t = T$ when the switch is turned on by an external driver.

The decrease in the magnetic energy stored in inductor L during the interval $DT < t \leq T$ is

$$\Delta W_{L(out)} = \tfrac{1}{2}L[i_L^2(DT) - i_L^2(T)]. \tag{4.15}$$

For steady-state operation, the increase in the magnetic energy stored in the inductor $\Delta E_{L(in)}$ is equal to the decrease in the stored magnetic energy in the inductor $\Delta E_{L(out)}$.

4.2.5 DC Voltage Transfer Function for CCM

Referring to Figure 4.2 and using a volt-second balance, $A^+ = A^-$, we can write

$$DTV_I = (1 - D)TV_O, \tag{4.16}$$

which can be rearranged as

$$V_O = \frac{DV_I}{1 - D}, \tag{4.17}$$

resulting in the dc voltage transfer function of the lossless converter,

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{1 - D}. \tag{4.18}$$

The range of $M_{V\,DC}$ for the lossless buck-boost converter is

$$0 \le M_{V\,DC} < \infty. \tag{4.19}$$

For the lossless buck-boost converter, $M_{V\,DC}$ increases from 0 to ∞ as D increases from 0 to 1. It follows from (4.17) that the output voltage V_O is independent of the load resistance R_L and depends only on the dc input voltage V_I. It will shortly be shown that $M_{V\,DC}$ is significantly altered by losses, especially when the value of D is c1ose to 1. From (4.18),

$$D = \frac{M_{V\,DC}}{M_{V\,DC} + 1}. \tag{4.20}$$

The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = \frac{V_I}{(1-D)^2}. \tag{4.21}$$

In practice, V_O should be held constant. If V_I increases, D should be decreased by a control circuit so that V_O remains constant, and vice versa. The dc current transfer function is

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{1-D}{D}, \tag{4.22}$$

and its value decreases from ∞ to 0 as D is increased from 0 to 1.

Using (4.11),

$$\frac{V_O}{V_{SM}} = \frac{V_O}{V_I + V_O} = \frac{1}{1 + \dfrac{V_I}{V_O}} = D, \tag{4.23}$$

and using (4.22),

$$\frac{I_O}{I_{SM}} \approx \frac{I_O}{I_I + I_O} = \frac{1}{1 + \dfrac{I_I}{I_O}} = 1 - D. \tag{4.24}$$

Thus, the switch and diode utilization in the buck-boost converter is characterized by the output-power capability

$$c_p \equiv \frac{P_O}{V_{SM} I_{SM}} = \frac{V_O I_O}{V_{SM} I_{SM}} \approx D(1-D) = \frac{M_{V\,DC}}{(M_{V\,DC} + 1)^2}. \tag{4.25}$$

As D is increased from 0 to 1, c_p increases from 0, reaches a maximum equal to 0.25 at $D = 0.5$, and then decreases back to 0.

4.2.6 Device Stresses for CCM

The dc input power is $P_I = I_I V_I$ and the dc output power is $P_O = I_O V_O$. Neglecting power losses, $P_O = P_I$, that is, $V_O I_O = V_I I_I$. Hence,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{M_{I\,DC}} = \frac{D}{1-D}. \tag{4.26}$$

Therefore,

$$V_{Imax} = V_O \frac{1 - D_{min}}{D_{min}}. \tag{4.27}$$

The maximum switch and diode peak voltages in the steady state in CCM are

$$V_{SMmax} = V_{DMmax} = V_{Imax} + V_O = \frac{V_O}{D_{min}}. \tag{4.28}$$

The maximum inductor current ripple is given by

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L}. \tag{4.29}$$

From (4.26), the dc component of the input current is

$$I_I = M_{V\,DC} I_O = \frac{D}{1 - D} I_O. \tag{4.30}$$

The maximum value of the dc input current occurs at I_{Omax} and V_{Imin}, that is, at $M_{V\,DCmax}$ and D_{max}. Hence,

$$I_{Imax} = M_{V\,DCmax} I_{Omax} = \frac{D_{max}}{1 - D_{max}} I_{Omax}. \tag{4.31}$$

The average inductor current I_L is equal to the sum of the average switch current I_S and the average diode current I_D. In turn, the average switch current I_S is equal to the average input current I_I and the average diode current I_D is equal to the average output current I_O. Thus,

$$I_L = I_S + I_D = I_I + I_O = \frac{I_O}{1 - D}. \tag{4.32}$$

Hence, the maximum switch and diode peak currents in the steady state in CCM are

$$I_{SMmax} = I_{DMmax} = I_{Imax} + I_{Omax} + \frac{\Delta i_{Lmin}}{2} = \frac{I_{Omax}}{1 - D_{max}} + \frac{V_O(1 - D_{max})}{2 f_s L}. \tag{4.33}$$

Note that $\Delta i_L = \Delta i_{Lmin}$ when $I_I = I_{Imax}$.

4.2.7 Boundary between CCM and DCM

Figure 4.3 depicts the inductor current waveform at the CCM/DCM boundary. This waveform can be described by

$$i_L = \frac{V_I}{L} t, \qquad \text{for } 0 < t \le DT. \tag{4.34}$$

From (4.18), $V_I = V_O(1 - D)/D$. Therefore,

$$\Delta i_{Lmax} = i_L(DT) = \frac{V_I DT}{L} = \frac{V_O(1 - D_{min})}{f_s L_{min}}. \tag{4.35}$$

The dc inductor current at the be CCM/DCM boundary is

$$I_{LB} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O(1 - D_{min})}{2 f_s L_{min}}. \tag{4.36}$$

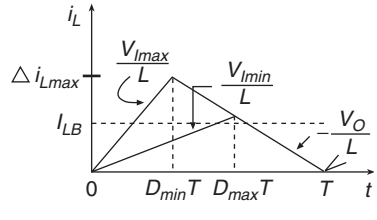


Figure 4.3 Waveforms of the inductor current at the CCM/DCM boundary at V_{Imin} and V_{Imax}.

From (4.32),

$$I_L = \frac{I_O}{1 - D}, \tag{4.37}$$

which results in the dc output current at the boundary,

$$I_{OB} = I_{LB}(1 - D_{min}) = \frac{V_O(1 - D_{min})^2}{2f_sL}. \tag{4.38}$$

The load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_sL}{(1 - D_{min})^2}. \tag{4.39}$$

Hence, the minimum value of the inductance L is found to be

$$L_{min} = \frac{V_O(1 - D_{min})^2}{2f_sI_{OB}} = \frac{R_{Lmax}(1 - D_{min})^2}{2f_s}. \tag{4.40}$$

Figure 4.4 and 4.5 show the normalized load current $I_{OB}/(V_O/2f_sL) = (1 - D)^2$ and load resistance $R_{LB}/(2f_sL) = 1/(1 - D)^2$ as functions of D at the CCM/DCM boundary.

4.2.8 Ripple Voltage in Buck-boost Converter for CCM

The output part of the buck-boost converter is shown in Figure 4.6, where the filter capacitor is modeled by its capacitance C and its ESR denoted by r_C. Figure 4.7 displays current and voltage waveforms for the converter output circuit. The dc component of the inductor current equals the dc load current I_O. The ac component of the inductor current flows

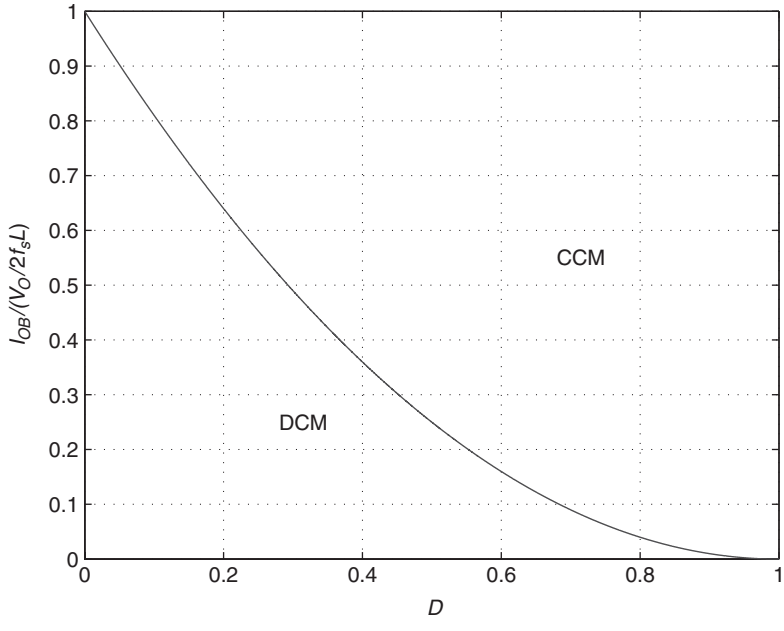


Figure 4.4 Normalized load current $I_{OB}/(V_O/2f_sL)$ as a function of D at the CCM/DCM boundary for the buck-boost converter.

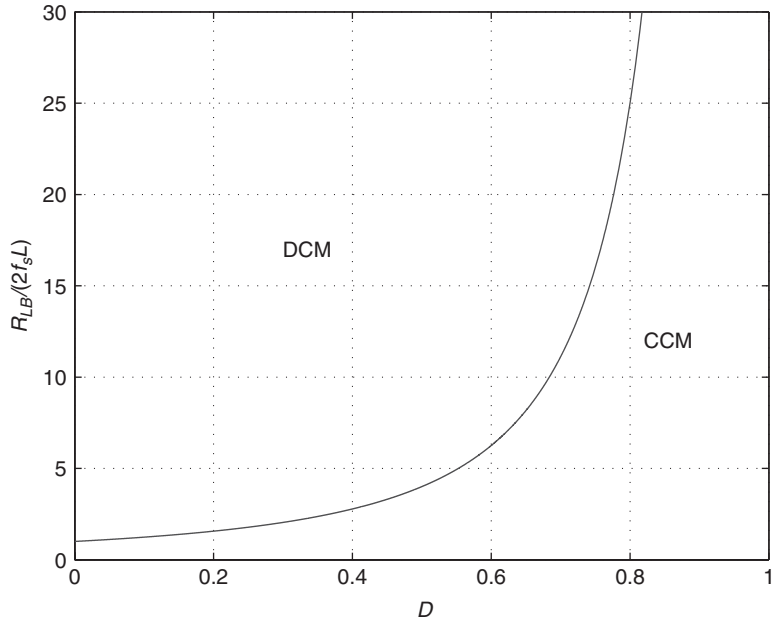


Figure 4.5 Normalized load resistance $R_{LB}/(2f_sL)$ as a function of D at the CCM/DCM boundary for the buck-boost converter.

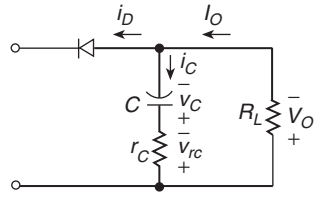


Figure 4.6 Output circuit of the buck-boost converter for deriving the output voltage ripple.

through the capacitor C and the load resistance R_L. In most practical applications, the current through the capacitor is approximately equal to the ac component of the inductor current.

The peak-to-peak value of the capacitor current may be written as

$$I_{Cpp} = I_{DM} \approx I_I + I_O = \frac{I_O}{1-D}, \tag{4.41}$$

resulting in the peak-to-peak value of the voltage across r_C,

$$V_{rcpp} = r_C I_{Cpp} = r_C I_{DMmax} \approx \frac{r_C I_{Omax}}{1-D_{max}}. \tag{4.42}$$

The peak-to-peak value of the output ripple voltage V_r is usually given. Hence, the maximum peak-to-peak value of the ac component of the voltage across the capacitance C is found to be

$$V_{Cpp} \approx V_r - V_{rcpp}. \tag{4.43}$$

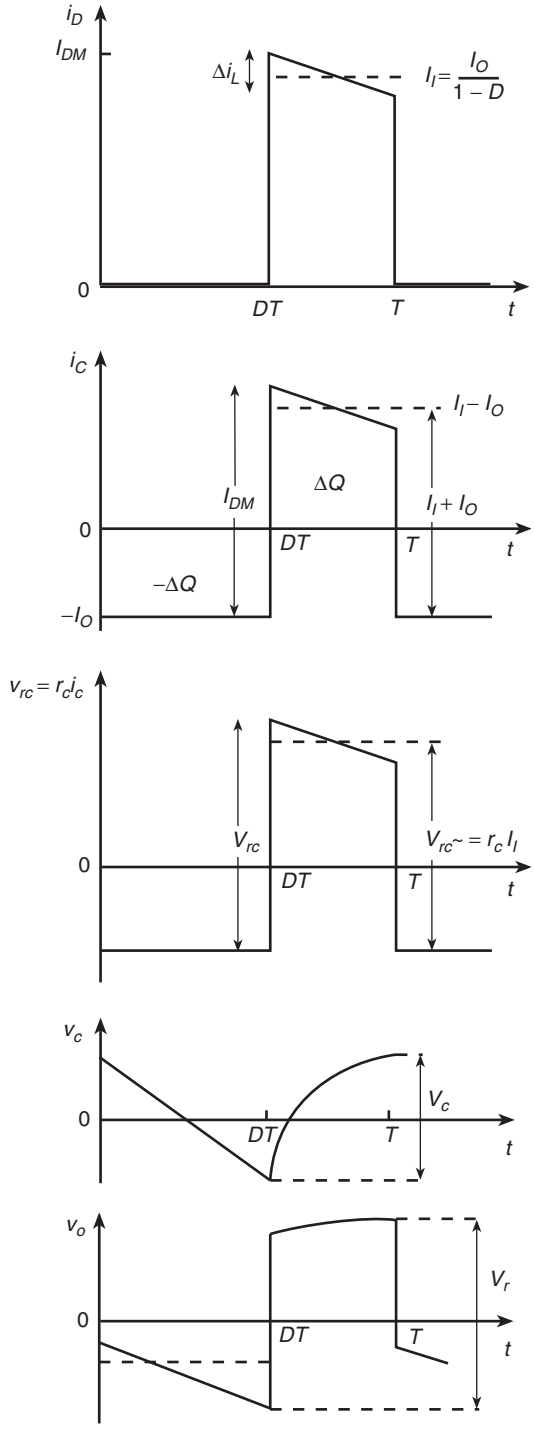


Figure 4.7 Waveforms associated with the ripple voltage for the PWM buck-boost converter for CCM.

On the other hand, this voltage is approximately given by

$$V_{Cpp} = \frac{\Delta Q_{max}}{C_{min}} = \frac{I_{Omax} D_{max} T}{C_{min}} = \frac{V_O D_{max}}{f_s R_{Lmin} C_{min}}, \tag{4.44}$$

where ΔQ_{max} is the maximum decrease in charge during the time interval from zero to DT. Rearrangement of (4.44) gives

$$C_{min} = \frac{I_{Omax} D_{max}}{f_s V_{Cpp}} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}}. \tag{4.45}$$

4.2.9 Power Losses and Efficiency of the Buck-boost Converter for CCM

An equivalent circuit of the buck-boost converter with parasitic resistances is shown in Figure 4.8. In this figure, r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The conduction losses will be evaluated assuming that the inductor current i_L is ripple-free and equals the dc current $I_I + I_O$. Hence, the switch current can be approximated by

$$i_S = \begin{cases} I_L = I_I + I_O = \dfrac{I_O}{1-D}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{4.46}$$

resulting in its rms value,

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_0^{DT} dt} = \frac{I_O\sqrt{D}}{1-D}, \tag{4.47}$$

and the MOSFET conduction loss,

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} I_O^2}{(1-D)^2} = \frac{D r_{DS} P_O}{(1-D)^2 R_L}. \tag{4.48}$$

Assuming that the transistor output capacitance C_o is linear, the switching loss is expressed as

$$\begin{aligned} P_{sw} &= f_s C_o V_{SM}^2 = f_s C_o (V_I + V_O)^2 \\ &= \frac{f_s C_o V_O^2}{D^2} = \frac{f_s C_o V_O^2 (1 + M_{V\,DC})^2}{M_{V\,DC}^2} = \frac{f_s C_o R_L P_O}{D^2} \\ &= \frac{f_s C_o R_L (1 + M_{V\,DC})^2 P_O}{M_{V\,DC}^2}. \end{aligned} \tag{4.49}$$

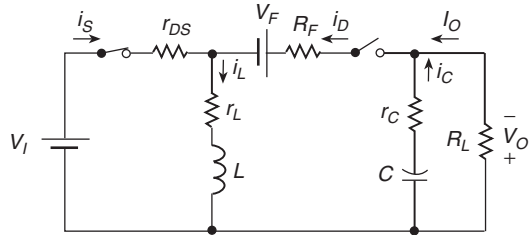


Figure 4.8 Equivalent circuit of the buck-boost converter with parasitic resistances and diode offset voltage to determine power losses.

Hence, one obtains the total power dissipation in the MOSFET (excluding the drive power)

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \frac{Dr_{DS}I_O^2}{(1-D)^2} + \frac{1}{2}f_s C_o (V_I + V_O)^2$$
$$= \left[\frac{Dr_{DS}}{(1-D)^2 R_L} + \frac{f_s C_o R_L}{2D^2}\right] P_O$$
$$= \left[\frac{Dr_{DS}}{(1-D)^2 R_L} + \frac{f_s C_o R_L (1+M_{V\,DC})^2}{2M_{V\,DC}^2}\right] P_O. \tag{4.50}$$

Similarly, the diode current may be approximated by

$$i_D = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ I_L = I_I + I_O = \dfrac{I_O}{1-D}, & \text{for } DT < t \le T, \end{cases} \tag{4.51}$$

which yields its rms value,

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_{DT}^T dt} = \frac{I_O}{\sqrt{1-D}}, \tag{4.52}$$

and the power loss in R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F I_O^2}{1-D} = \frac{R_F P_O}{(1-D)R_L}. \tag{4.53}$$

The average value of the diode current is

$$I_D = \frac{1}{T}\int_0^T i_D\, dt = \frac{I_O}{(1-D)T}\int_{DT}^T dt = I_O, \tag{4.54}$$

which gives the power loss associated with the voltage V_F as

$$P_{VF} = V_F I_D = V_F I_O = \frac{V_F P_O}{V_O}. \tag{4.55}$$

Thus, the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = V_F I_O + \frac{R_F I_O^2}{1-D} = \left[\frac{V_F}{V_O} + \frac{R_F}{(1-D)R_L}\right] P_O. \tag{4.56}$$

The inductor current is

$$i_L \approx I_I + I_O = \frac{I_O}{1-D}, \tag{4.57}$$

leading to its rms value,

$$I_{Lrms} \approx I_I + I_O = \frac{I_O}{1-D}, \tag{4.58}$$

and the inductor conduction loss,

$$P_{rL} = r_L I_{Lrms}^2 = \frac{r_L I_O^2}{(1-D)^2} = \frac{r_L P_O}{(1-D)^2 R_L}. \tag{4.59}$$

The current through the filter capacitor is

$$i_C = \begin{cases} -I_O, & \text{for } 0 < t \le DT, \\ I_I = \dfrac{DI_O}{1-D}, & \text{for } DT < t \le T, \end{cases} \tag{4.60}$$

and the rms current through the filter capacitor is found to be

$$I_{Crms} = \sqrt{\frac{1}{T}\int_0^T i_C^2\, dt} = I_O\sqrt{\frac{D}{1-D}} = I_L\sqrt{D(1-D)} = I_S\sqrt{\frac{1-D}{D}}, \tag{4.61}$$

and the power loss in the filter capacitor

$$P_{rC} = r_C I_{Crms}^2 = \frac{Dr_C I_O^2}{1-D} = \frac{Dr_C P_O}{(1-D)R_L}. \tag{4.62}$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} \\ &= \frac{Dr_{DS}I_O^2}{(1-D)^2} + f_s C_o(V_I + V_O)^2 + V_F I_O + \frac{R_F I_O^2}{1-D} + \frac{r_L I_O^2}{(1-D)^2} + \frac{Dr_C I_O^2}{1-D} \\ &= \left[\frac{Dr_{DS} + r_L}{(1-D)^2 R_L} + \frac{f_s C_o R_L (1 + M_{V\,DC})^2}{M_{V\,DC}^2} + \frac{V_F}{V_O} + \frac{R_F + Dr_C}{R_L(1-D)}\right] P_O. \end{aligned} \tag{4.63}$$

Thus, the converter efficiency is

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} \\ &= \frac{1}{1 + \dfrac{r_L + Dr_{DS}}{(1-D)^2 R_L} + \dfrac{R_F + Dr_C}{(1-D)R_L} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o R_L (1 + M_{V\,DC})^2}{M_{V\,DC}^2}}. \end{aligned} \tag{4.64}$$

Figure 4.9 shows the efficiency of the buck-boost converter η as a function of the duty cycle D at various load resistances for $V_O = 12\,\text{V}$, $r_{DS} = 0.11\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 20\,\text{m}\Omega$, $r_L = 0.05\,\Omega$, $r_C = 6\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$. When the duty cycle D is close to zero, the conduction losses are low, but the switching loss is high because V_I is high at a fixed value of V_O. Hence, the efficiency decreases to zero. When the duty cycle D is close to 1, the conduction losses are high, reducing the efficiency to zero. Therefore, operation at very low and high values of D should be avoided.

4.2.10 DC Voltage Transfer Function of Lossy Buck-boost Converter for CCM

The dc component of the input current is

$$I_I = \frac{1}{T}\int_0^T i_S\, dt = \frac{1}{T}\int_0^{DT} I_L\, dt = DI_L = D(I_I + I_O), \tag{4.65}$$

where $I_L = I_I + I_O$. Similarly, the dc component of the output current is

$$I_O = \frac{1}{T}\int_0^T i_D\, dt = \frac{1}{T}\int_{DT}^T I_L\, dt = (1-D)I_L = (1-D)(I_I + I_O). \tag{4.66}$$

Hence, one obtains the dc current transfer function of the buck-boost converter,

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{1-D}{D} = \frac{1}{D} - 1. \tag{4.67}$$

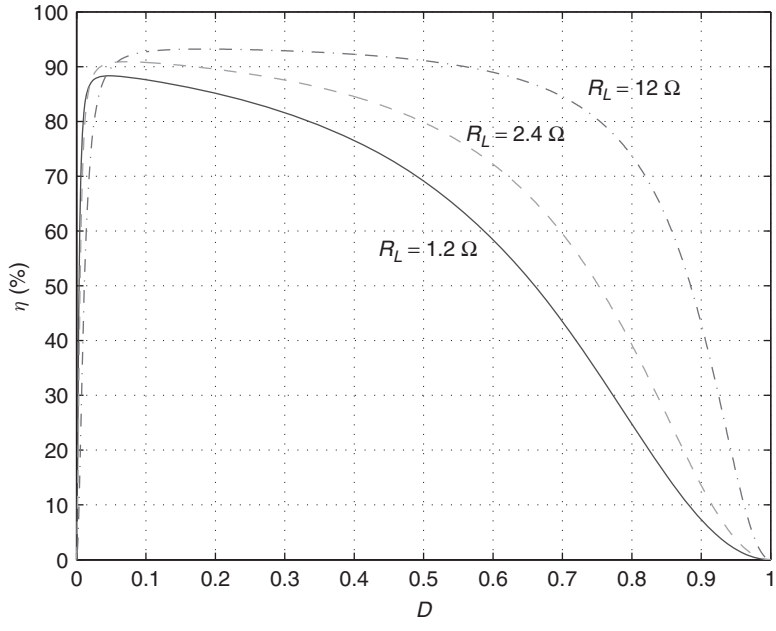


Figure 4.9 Efficiency of the buck-boost converter η versus duty cycle D at various load resistances for $V_O = 12\,\text{V}$, $r_{DS} = 0.11\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 20\,\text{m}\Omega$, $r_L = 0.05\,\Omega$, $r_C = 6\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$.

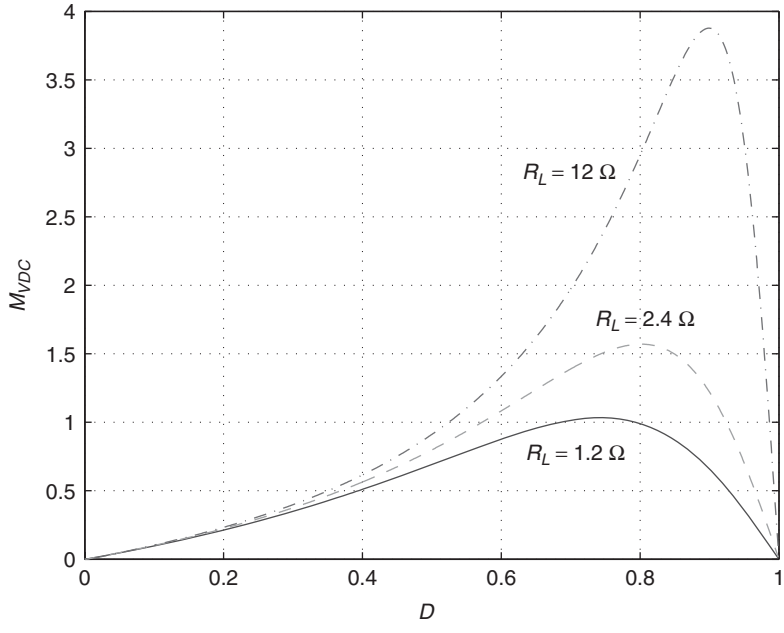


Figure 4.10 The dc voltage transfer function $M_{V\,DC}$ of the lossy buck-boost converter for $V_O = 12\,\text{V}$, $r_{DS} = 0.11\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 20\,\text{m}\Omega$, $r_L = 0.05\,\Omega$, $r_C = 6\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$.

This equation holds true for both lossless and lossy converter. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = \frac{(1-D)M_{V\,DC}}{D}, \tag{4.68}$$

from which the voltage transfer function of the lossy buck-boost converter is

$$\begin{aligned} M_{V\,DC} &= \frac{\eta}{M_{I\,DC}} = \frac{\eta D}{1-D} = \eta M_{V\,DC(lossless)} \\ &= \frac{D}{(1-D)\left[1 + \dfrac{r_L + D r_{DS}}{(1-D)^2 R_L} + \dfrac{R_F + D r_C}{(1-D)R_L} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o R_L}{D^2}\right]}. \end{aligned} \tag{4.69}$$

Figure 4.10 portrays $M_{V\,DC}$ as a function of D at various load resistances for $V_O = 12\,\text{V}$, $r_{DS} = 0.11\,\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 20\,\text{m}\Omega$, $r_L = 0.05\,\Omega$, $r_C = 6\,\text{m}\Omega$, $f_s = 100\,\text{kHz}$, and $C_o = 100\,\text{pF}$. It can be seen that $M_{V\,DC}$ first increases with D, reaches its maximum value, and then decreases to zero. This is because the efficiency is very low at D close to 1. From (4.69), the on-duty cycle is

$$D = \frac{M_{V\,DC}}{M_{V\,DC} + \eta} = \frac{1}{1 + \dfrac{\eta}{M_{V\,DC}}} = \frac{1}{1 + \dfrac{\eta V_I}{V_O}}. \tag{4.70}$$

Notice that the duty cycle D at a given dc voltage transfer function is greater for the lossy converter than for the lossless converter. The switch must be closed for a greater portion of the cycle in the lossy converter to transfer energy equal to the output energy and the losses.

Substitution of (4.70) into (4.64) gives the efficiency of the buck-boost converter,

$$\eta = \frac{N_\eta}{D_\eta}, \tag{4.71}$$

where

$$\begin{aligned} N_\eta = 1 - M_{V\,DC}\left(\frac{2r_L + r_{DS} + R_F + r_C}{R_L}\right) + \left\{\left[1 - M_{V\,DC}\left(\frac{2r_L + r_{DS} + R_F + r_C}{R_L}\right)\right]^2 \right. \\ \left. - \frac{4M_{V\,DC}^2 (r_L + r_{DS})}{R_L}\left[1 + \frac{r_L + R_F}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L (1 + M_{V\,DC})^2}{M_{V\,DC}^2}\right]\right\}^{\frac{1}{2}} \end{aligned} \tag{4.72}$$

and

$$D_\eta = 2\left[1 + \frac{r_L + R_F}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L (1 + M_{V\,DC})^2}{M_{V\,DC}^2}\right]. \tag{4.73}$$

4.2.11 Design of Buck-boost Converter for CCM

Design a PWM buck-boost converter that meets the following specifications: $V_I = 28\,\text{V} \pm 4\,\text{V}$, $V_O = 12\,\text{V}$, $I_O = 1$ to $10\,\text{A}$, and $V_r/V_O \le 1\,\%$.

Solution. The maximum and minimum values of the output power are

$$P_{Omax} = V_O I_{Omax} = 12 \times 10 = 120\,\text{W} \tag{4.74}$$

and

$$P_{Omin} = V_O I_{Omin} = 12 \times 1 = 12\,\text{W}. \tag{4.75}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{10} = 1.2\,\Omega \tag{4.76}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{12}{1} = 12\,\Omega. \tag{4.77}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{12}{32} = 0.375, \tag{4.78}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{12}{28} = 0.429, \tag{4.79}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{12}{24} = 0.5. \tag{4.80}$$

Assume the converter efficiency $\eta = 85\,\%$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{M_{V\,DCmin}}{M_{V\,DCmin} + \eta} = \frac{0.375}{0.375 + 0.85} = 0.306, \tag{4.81}$$

$$D_{nom} = \frac{M_{V\,DCnom}}{M_{V\,DCnom} + \eta} = \frac{0.429}{0.429 + 0.85} = 0.335, \tag{4.82}$$

and

$$D_{max} = \frac{M_{V\,DCmax}}{M_{V\,DCmax} + \eta} = \frac{0.5}{0.5 + 0.85} = 0.370. \tag{4.83}$$

Selecting the switching frequency $f_s = 100\,\text{kHz}$, the minimum inductance is

$$L_{min} = \frac{R_{Lmax}(1 - D_{min})^2}{2f_s} = \frac{12 \times (1 - 0.306)^2}{2 \times 10^5} = 28.9\,\mu\text{H}. \tag{4.84}$$

Pick $L = 30\,\mu\text{H}$.

The peak-to-peak value of the ac component of the inductor current is

$$\Delta i_{Lmin} = \frac{V_O(1 - D_{max})}{f_s L} = \frac{12 \times (1 - 0.370)}{10^5 \times 30 \times 10^{-6}} = 2.52\,\text{A}. \tag{4.85}$$

The maximum dc input current occurs at $V_{Imin} = 24\,\text{V}$, which corresponds to the maximum dc voltage transfer function $M_{V\,DCmax} = 0.5$. This current is given by

$$I_{Imax} = M_{V\,DCmax} I_{Omax} = 0.5 \times 10 = 5\,\text{A}. \tag{4.86}$$

The current and voltage stresses of the semiconductor devices are

$$I_{SMmax} = I_{DMmax} = I_{Imax} + I_{Omax} + \frac{\Delta i_{Lmin}}{2} = 5 + 10 + \frac{2.52}{2} = 16.26\,\text{A} \tag{4.87}$$

and

$$V_{SMmax} = V_{DMmax} = V_O + V_{Imax} = 12 + 32 = 44\,\text{V}. \tag{4.88}$$

Let us select an International Rectifier IRF142 power MOSFET whose $V_{DSS} = 100\,\text{V}$, $I_{SM} = 24\,\text{A}$, $r_{DS} = 0.11\,\Omega$, $Q_g = 38\,\text{nC}$, and $C_o = 100\,\text{pF}$. Choose also an MUR2510 ultrafast recovery diode whose $I_{F(AV)} = 25\,\text{A}$, $V_{DM} = 100\,\text{V}$, $V_F = 0.7\,\text{V}$, and $R_F = 20\,\text{m}\Omega$.

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{12}{100} = 120\,\text{mV}. \tag{4.89}$$

Assume that $V_{rcpp} = 100\,\text{mV}$. Hence, one obtains the maximum value of the ESR of the filter capacitor,

$$r_{Cmax} = \frac{V_{rcpp}}{I_{DMmax}} = \frac{100 \times 10^{-3}}{16.26} = 6.15\,\text{m}\Omega. \tag{4.90}$$

The ripple voltage across the filter capacitance is

$$V_{Cpp} = V_r - V_{rcpp} = 120 - 100 = 20\,\text{mV}, \tag{4.91}$$

and the filter capacitance is

$$C_{min} = \frac{D_{max}}{f_s R_{Lmin}} \frac{V_O}{V_{Cpp}} = \frac{0.370}{10^5 \times 1.2} \frac{12}{0.02} = 1850\,\mu\text{F}. \tag{4.92}$$

Pick $C = 2.2\,\text{mF}/25\,\text{V}/6\,\text{m}\Omega$.

The power losses and the efficiency will be calculated for full load $I_{Omax} = 10\,\text{A}$ and minimum dc input voltage $V_{Imin} = 24\,\text{V}$, corresponding to $D_{max} = 0.370$. The rms value of the inductor current is

$$I_{Lrms} = \frac{I_{Omax}}{1 - D_{max}} = \frac{10}{1 - 0.370} = 15.87\,\text{A}. \tag{4.93}$$

Assuming the dc ESR of the inductor $r_L = 50\,\text{m}\Omega$, one arrives at the loss in the ESR of the inductor

$$P_{rL} = r_L I_{Lrms}^2 = 0.05 \times 15.87^2 = 12.59\,\text{W}. \tag{4.94}$$

The switch rms current is

$$I_{Srms} = \frac{I_{Omax}\sqrt{D_{max}}}{1 - D_{max}} = \frac{10\sqrt{0.370}}{1 - 0.370} = 9.655\,\text{A}, \tag{4.95}$$

which gives the MOSFET conduction loss,

$$P_{rDS} = r_{DS} I_{Srms}^2 = 0.11 \times 9.655^2 = 10.25\,\text{W}. \tag{4.96}$$

The switching loss is

$$P_{sw} = f_s C_o V_{SMmin}^2 = f_s C_o (V_{Imin} + V_O)^2 = 10^5 \times 100 \times 10^{-12} \times (24 + 12)^2 = 12.96\,\text{mW}. \tag{4.97}$$

The total power loss in the MOSFET (without the gate-drive power) is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 10.25 + \frac{0.01296}{2} = 10.26\,\text{W}. \tag{4.98}$$

The rms diode current is

$$I_{Drms} = \frac{I_{Omax}}{\sqrt{1 - D_{max}}} = \frac{10}{\sqrt{1 - 0.370}} = 12.6\,\text{A}. \tag{4.99}$$

Thus, the power loss due to R_F is

$$P_{RF} = R_F I_{Drms}^2 = 0.02 \times 12.6^2 = 3.175\,\text{W}, \tag{4.100}$$

and the power loss due to V_F is

$$P_{VF} = V_F I_{Omax} = 0.7 \times 10 = 7\,\text{W}, \tag{4.101}$$

resulting in the diode conduction loss

$$P_D = P_{VF} + P_{RF} = 7 + 3.175 = 10.175\,\text{W}. \tag{4.102}$$

The rms current of the filter capacitor is

$$I_{Crms} = I_{Omax}\sqrt{\frac{D_{max}}{1 - D_{max}}} = 10\sqrt{\frac{0.370}{1 - 0.370}} = 7.66\,\text{A}. \tag{4.103}$$

Hence, the power loss in the ESR of the filter capacitor is

$$P_{rC} = r_C I_{Crms}^2 = 0.006 \times 7.66^2 = 0.352\,\text{W}. \tag{4.104}$$

The total power loss is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rC} \\ &= 10.25 + 0.013 + 10.175 + 12.59 + 0.352 = 33.38\,\text{W}. \end{aligned} \tag{4.105}$$

Hence, the converter efficiency is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{120}{120 + 33.38} = 78.2\,\%. \tag{4.106}$$

Assuming that the peak-to-peak gate-to-source voltage is $V_{GSpp} = 14\,\text{V}$, the gate-drive power is

$$P_G = f_s V_{GSpp} Q_g = 10^5 \times 14 \times 38 \times 10^{-9} = 53.2\,\text{mW}. \tag{4.107}$$

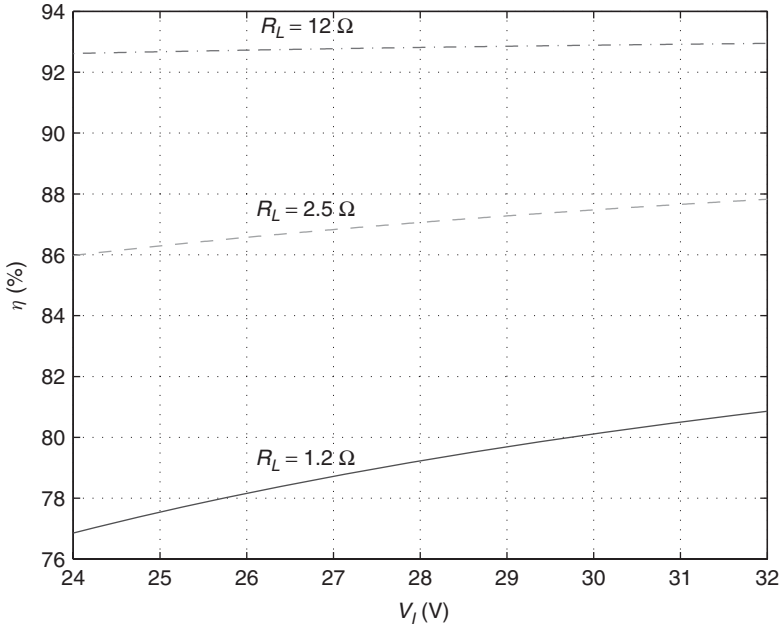


Figure 4.11 Efficiency η as a function of the dc input voltage V_I at fixed load resistances R_L for the buck-boost converter in CCM.

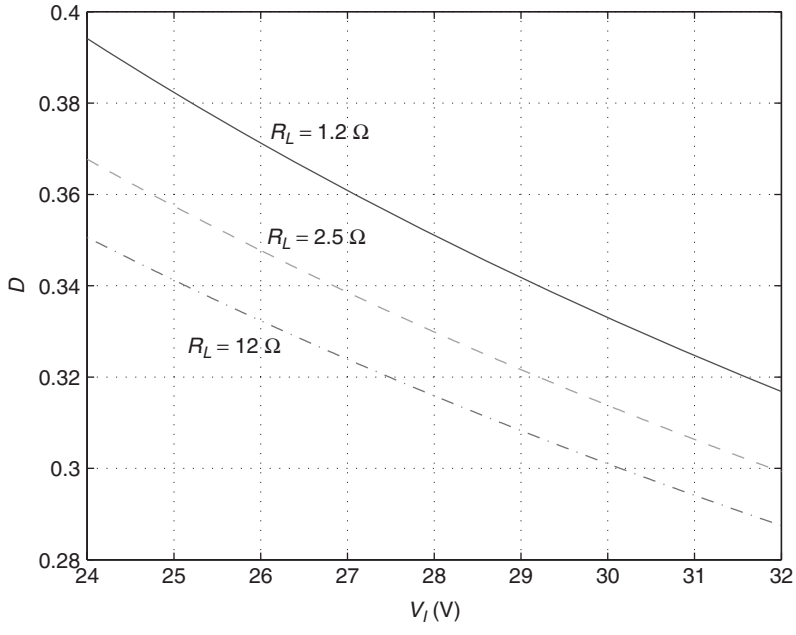


Figure 4.12 Duty cycle D as a function of the dc input voltage V_I at fixed load resistances R_L for the buck-boost converter in CCM.

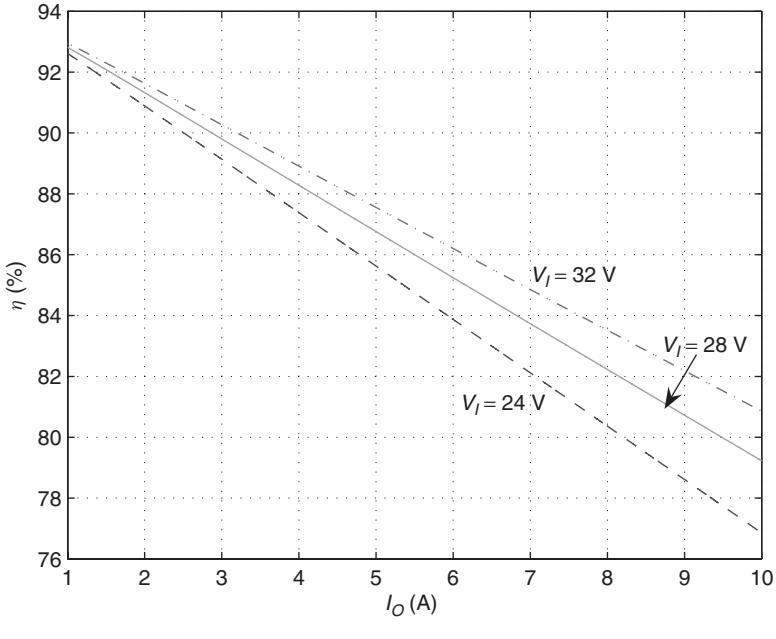


Figure 4.13 Efficiency η as a function of the dc load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in CCM.

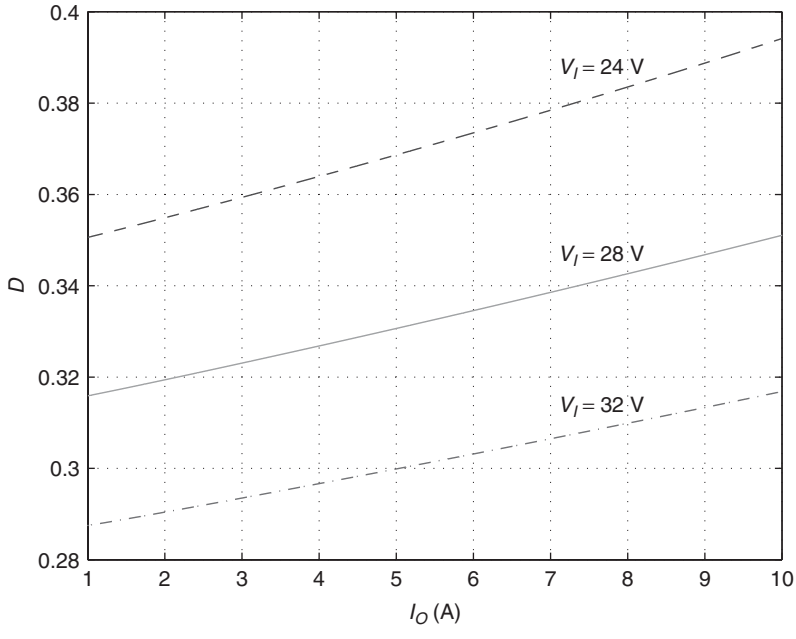


Figure 4.14 Duty cycle D as a function of the dc load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in CCM.

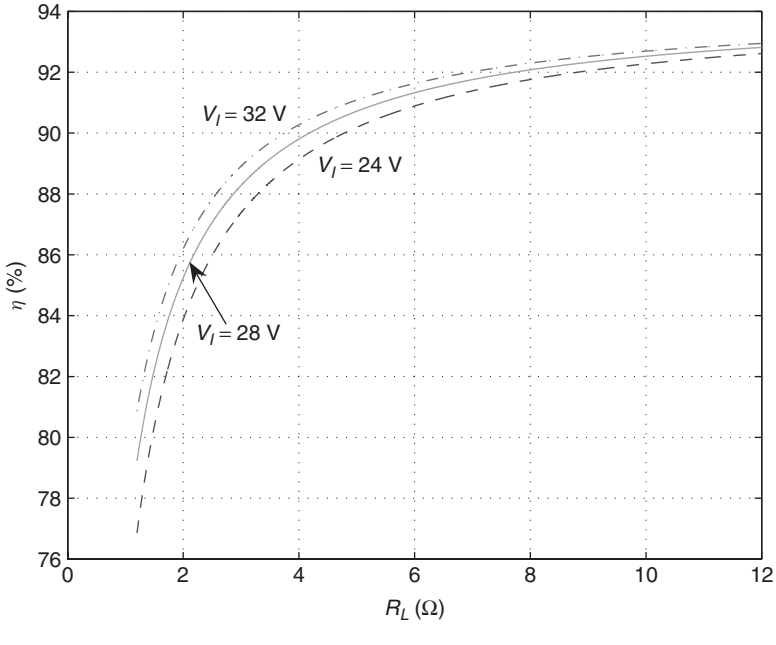


Figure 4.15 Efficiency η as a function of the load resistance R_L at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in CCM.

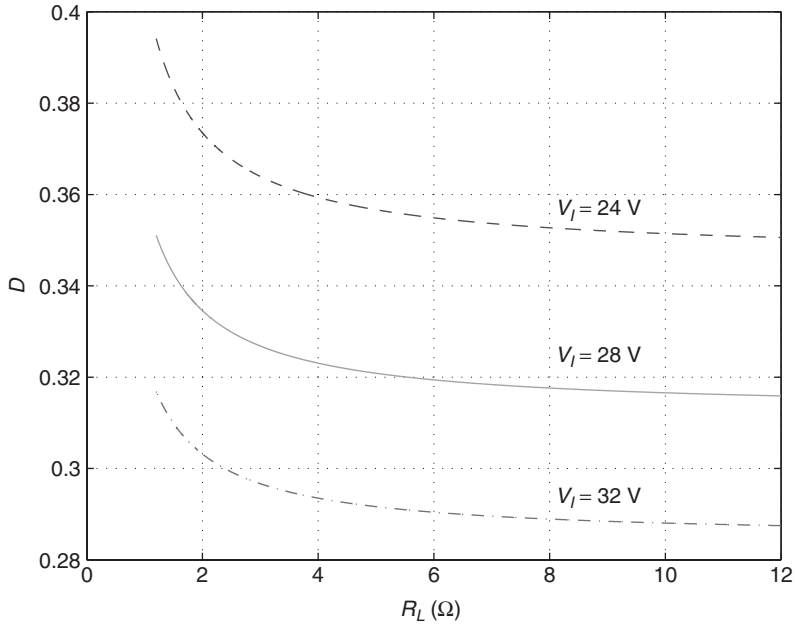


Figure 4.16 Duty cycle D as a function of the load resistance R_L at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converters in CCM.

Using (4.71)–(4.73), the efficiency η of the designed buck-boost converter can be computed for the specified range of V_I and I_O for CCM. Using the computed efficiency η, the duty cycle D can be calculated from (4.70). The plots of the efficiency η and the duty cycle D versus V_I at fixed load resistances R_L are depicted in Figure 4.11 and 4.12, respectively. Figure 4.13 and 4.14 show the plots of the efficiency η and the duty cycle D versus the load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$. Plots of the efficiency η and the duty cycle D versus R_L at fixed values of V_I are shown in Figure 4.15 and 4.16. The efficiency η decreases as I_O increases (or R_L decreases). The duty cycle D increases as V_I decreases and I_O increases (or R_L decreases).

4.3 DC Analysis of PWM Buck-boost Converter for DCM

Equivalent circuits for the PWM buck-boost converter operating in DCM are depicted in Figure 4.17. Idealized current and voltage waveforms are shown in Figure 4.18. Prior to time $t = 0$, the inductor current is zero. At time $t = 0$, the switch is turned on, causing the diode to turn off. The voltage across the inductor is V_I and the inductor current increases linearly from zero. At time $t = DT$, the switch is turned off and the diode turns on. The voltage across the inductor is $-V_O$. Therefore, the inductor current decreases linearly. This current flows through the diode. Once the diode current reaches zero, the diode begins to turn off. Since both the transistor and the diode are OFF, the inductor current is zero until the switch is turned on.

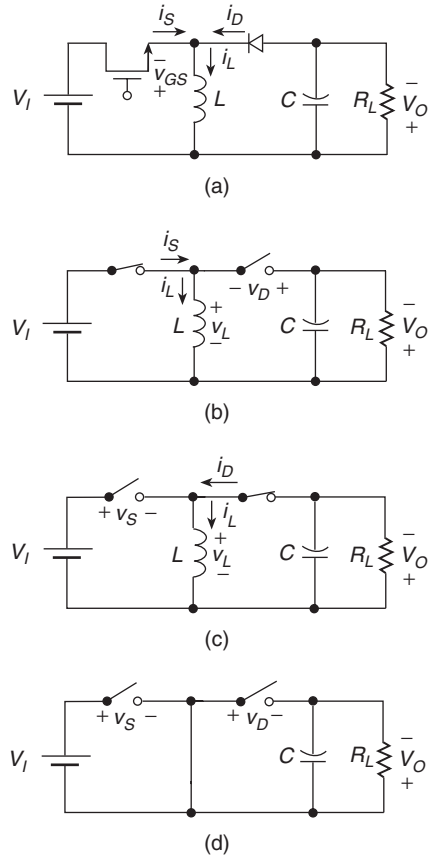


Figure 4.17 PWM buck-boost converter and its ideal equivalent circuits for DCM. (a) Circuit. (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON. (d) Equivalent circuit when both the switch and the diode are OFF.

4.3.1 Time Interval $0 < t \leq DT$

During this time interval, the switch is ON and the diode is OFF. The equivalent circuit is shown in Figure 4.17(b). The switch voltage v_S and the diode current i_D are zero. The voltage across the inductor L is

$$v_L = V_I = L\frac{di_L}{dt}, \qquad i_L(0) = 0, \tag{4.108}$$

and the inductor and switch current is

$$i_S = i_L = \frac{1}{L}\int_0^t v_L\,dt = \frac{1}{L}\int_0^t V_I\,dt = \frac{V_I}{L}t. \tag{4.109}$$

Hence, one obtains the peak switch and inductor current

$$I_{SM} = \Delta i_L = i_L(DT) = \frac{V_I DT}{L} = \frac{V_I D}{f_s L}. \tag{4.110}$$

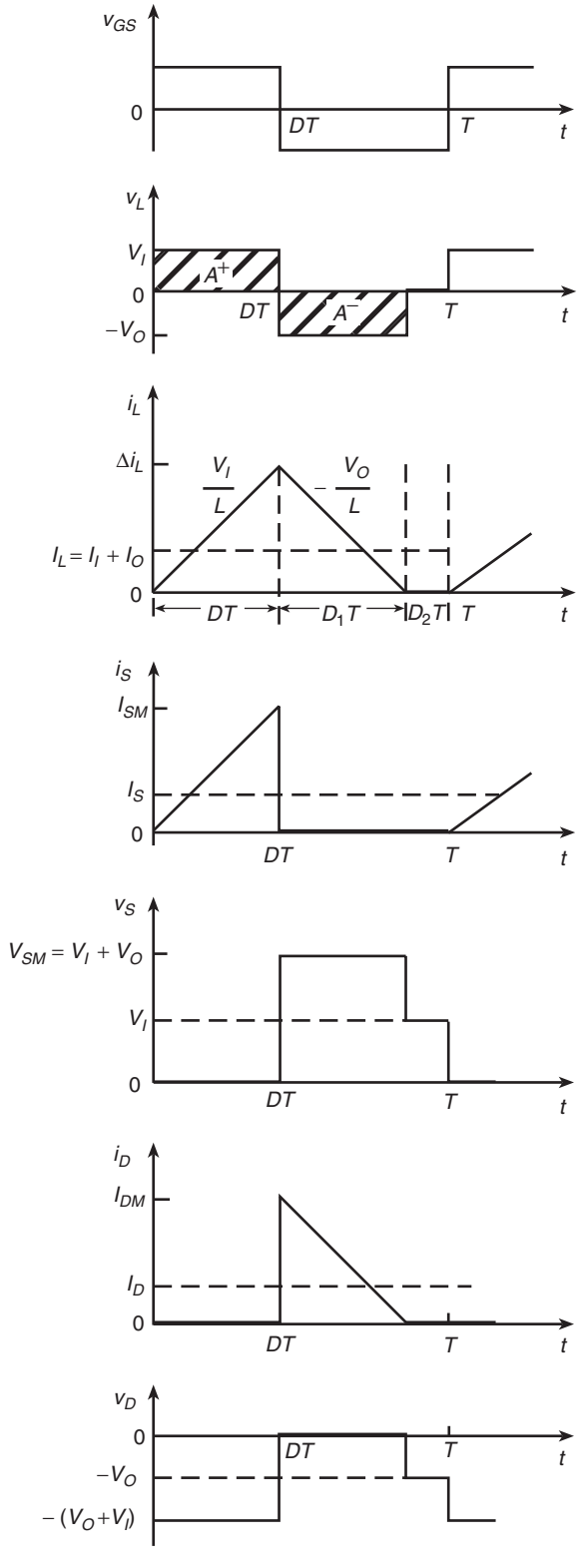


Figure 4.18 Waveforms for the PWM buck-boost converter operating in DCM.

The voltage across the diode is

$$v_D = -(V_I + V_O). \tag{4.111}$$

This time interval ends when the switch is turned off by the driver.

4.3.2 Time Interval $DT < t \leq (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 4.17(c). The switch is OFF and the diode is ON. Hence, $i_S = 0$ and $v_D = 0$. The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt} \tag{4.112}$$

and, using (4.110), the inductor and diode current is given by

$$\begin{aligned} i_D = i_L &= \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t}(-V_O)\,dt + i_L(DT) \\ &= -\frac{V_O}{L}(t - DT) + i_L(DT) = -\frac{V_O}{L}(t - DT) + \frac{V_I DT}{L}. \end{aligned} \tag{4.113}$$

The peak diode and inductor current is found to be

$$I_{DM} = \Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^{DT}(-V_O)\,dt = \frac{V_O D_1 T}{L} = \frac{V_O D_1}{f_s L}. \tag{4.114}$$

The peak voltage across the switch is

$$V_{SM} = V_I + V_O. \tag{4.115}$$

This time interval ends when the diode current reaches zero.

4.3.3 Time Interval $(D + D_1)T < t \leq T$

During this time interval, both the switch and the diode are OFF. The equivalent circuit is shown in Figure 4.17(d). The inductor current i_L, the inductor voltage v_L, the switch current i_S, and the diode current i_D are zero. The voltage across the switch is

$$v_S = V_I \tag{4.116}$$

and the voltage across the diode is

$$v_D = -V_O. \tag{4.117}$$

This time interval ends when the switch is turned on by the driver.

4.3.4 Device Stresses of the Buck-boost Converter in DCM

From (4.111) and (4.115), the voltage stress of the transistor and the diode is

$$V_{SMmax} = V_{DMmax} = V_{Imax} + V_O \tag{4.118}$$

and, from (4.110) and (4.114), the current stress of the transistor and the diode is

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{V_{Imax} D_{min}}{f_s L}. \tag{4.119}$$

4.3.5 DC Voltage Transfer Function of the Buck-boost Converter for DCM

Referring to Figure 4.18 and using the volt-second balance principle,

$$V_I DT = V_O D_1 T, \tag{4.120}$$

which leads to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{D_1}. \tag{4.121}$$

Using (4.110), the dc output current is found to be

$$I_O = \frac{1}{T}\int_0^T i_D\, dt = \frac{D_1 \Delta i_L}{2} = \frac{D_1 D V_I}{2 f_s L} = \frac{V_O}{R_L}. \tag{4.122}$$

Thus,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D D_1 R_L}{2 f_s L}. \tag{4.123}$$

Equating the right-hand sides of (4.121) and (4.123) gives

$$D_1 = \sqrt{\frac{2 f_s L}{R_L}}. \tag{4.124}$$

Substitution of this into (4.121) yields the dc voltage transfer function of the buck-boost converter for DCM,

$$M_{V\,DC} = D\sqrt{\frac{R_L}{2 f_s L}} = D\sqrt{\frac{V_O}{2 f_s L I_O}}, \quad \text{for } D \le 1 - \sqrt{\frac{2 f_s L}{R_L}} = 1 - \sqrt{\frac{2 f_s L I_O}{V_O}}. \tag{4.125}$$

It follows from this equation that $M_{V\,DC}$ depends on D, R_L, L, and f_s. From (4.125),

$$D = M_{V\,DC}\sqrt{\frac{2 f_s L}{R_L}} = M_{V\,DC}\sqrt{\frac{2 f_s L I_O}{V_O}}, \quad \text{for } D \le 1 - \sqrt{\frac{2 f_s L}{R_L}} = 1 - \sqrt{\frac{2 f_s L I_O}{V_O}}. \tag{4.126}$$

At the CCM/DCM boundary,

$$M_{V\,DCB} = \frac{D_B}{1 - D_B}. \tag{4.127}$$

Hence, from (4.126), one obtains the boundary duty cycle

$$D_B = 1 - \sqrt{\frac{2 f_s L}{R_L}} = 1 - \sqrt{\frac{2 f_s L I_O}{V_O}}. \tag{4.128}$$

Figure 4.19 and 4.20 show plots of the duty cycle D versus normalized load current $I_O/(V_O/2 f_s L)$ and normalized load resistance $R_L/(2 f_s L)$ at various values of $M_{V\,DC}$ for both CCM and DCM.

Substitution of (4.126) into (4.128) produces the dc voltage transfer function of the buck-boost converter at the boundary

$$M_{V\,DCB} = \sqrt{\frac{R_L}{2 f_s L}} - 1 = \sqrt{\frac{V_O}{2 f_s L I_O}} - 1. \tag{4.129}$$

Plots of $M_{V\,DC}$ as a function of normalized load current $I_O/(V_O/2 f_s L)$ and normalized load resistance $R_L/(2 f_s L)$ at fixed values of D are depicted in Figure 4.21 and 4.22, respectively.

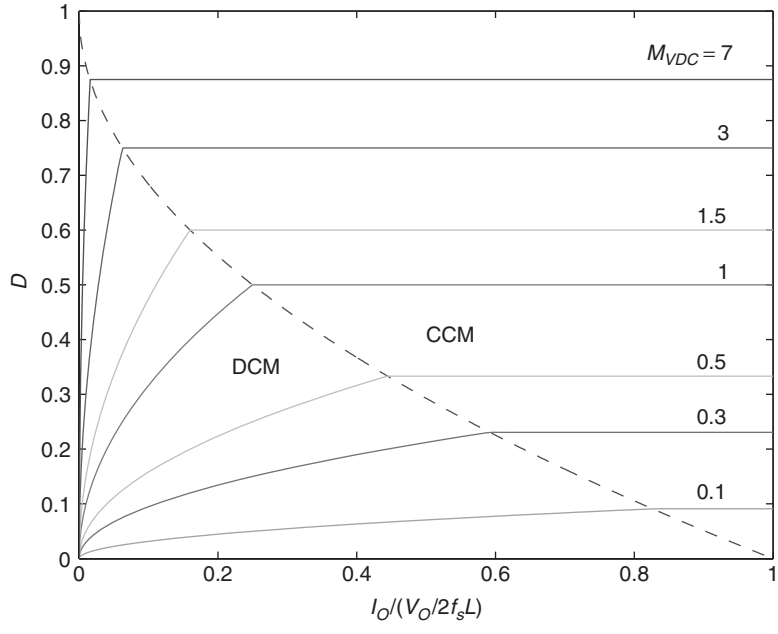


Figure 4.19 Duty cycle D as a function of the normalized load current $I_O/(V_O/2f_sL)$ at fixed values of $M_{V\,DC}$ for the lossless buck-boost converter.

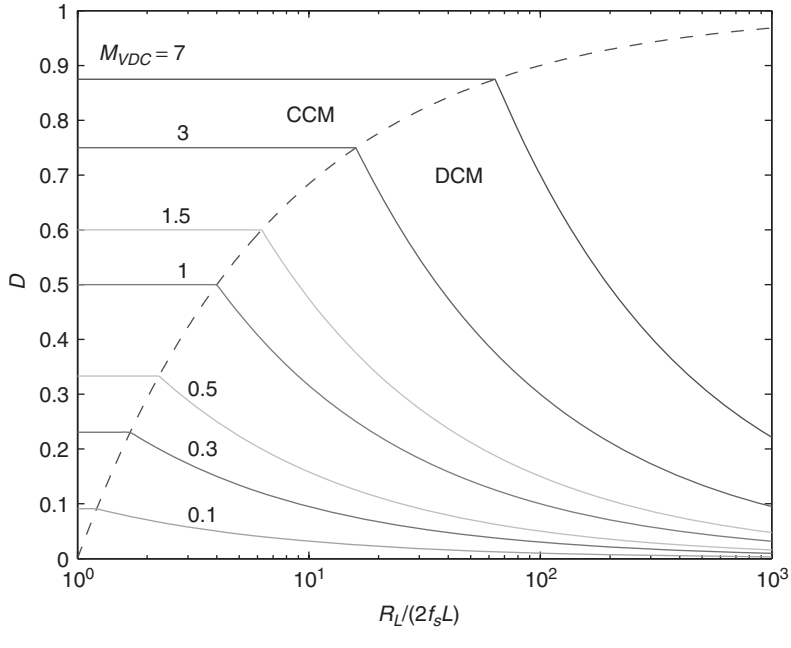


Figure 4.20 Duty cycle D as a function of the normalized load resistance $R_L/(2f_sL)$ at fixed values of $M_{V\,DC}$ for the lossless buck-boost converter.

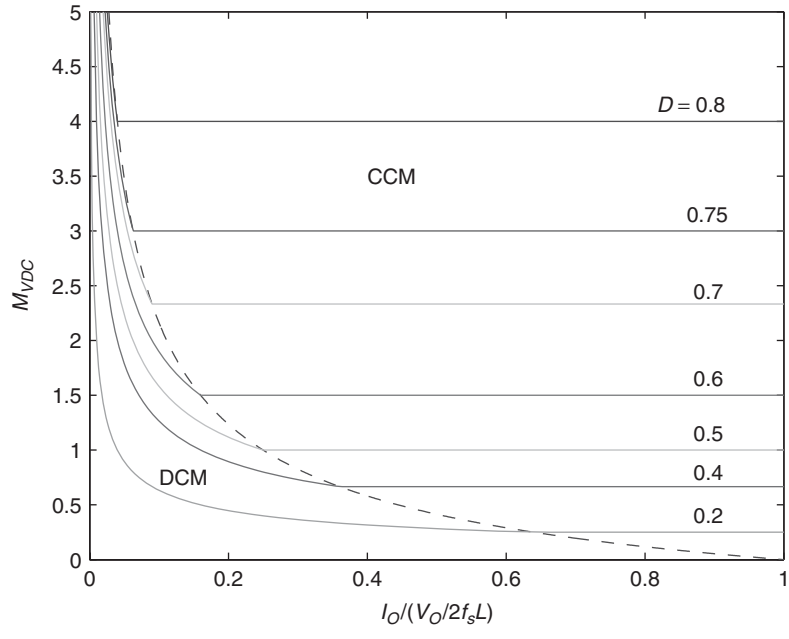


Figure 4.21 DC voltage transfer function $M_{V\,DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ at fixed values of duty cycle D for the lossless buck-boost converter.

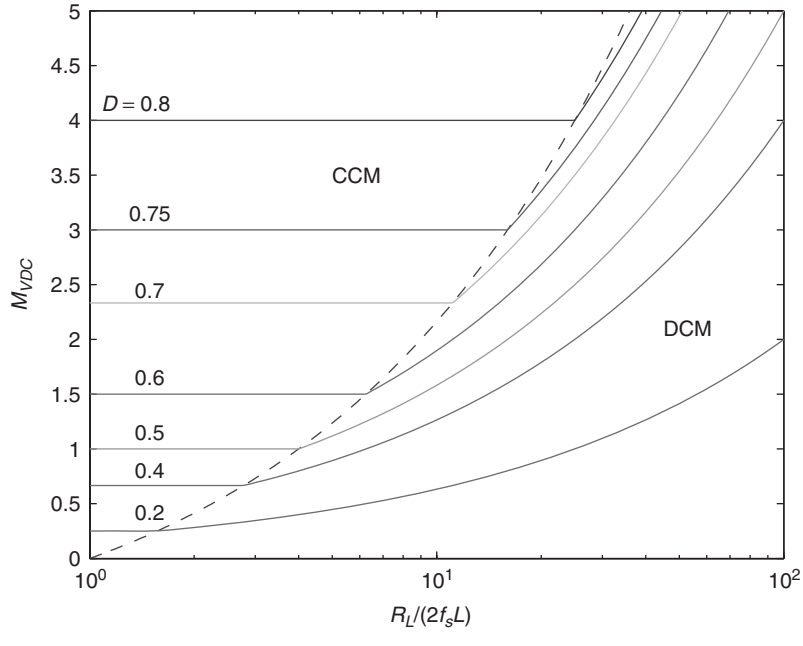


Figure 4.22 DC voltage transfer function $M_{V\,DC}$ versus normalized load resistance $R_L/(2f_sL)$ at fixed values of duty cycle D for the lossless buck-boost converter.

4.3.6 Maximum Inductance for DCM

Referring to Figure 4.2, the minimum value of the inductor peak current at the CCM/DCM boundary is

$$\Delta i_{Lmin} = \frac{V_{Imin} D_{Bmax} T}{L_{max}} = \frac{V_O(1 - D_{Bmax})}{f_s L_{max}}. \tag{4.130}$$

The dc inductor current at the CCM/DCM boundary is

$$I_{LB} = \frac{\Delta i_{Lmin}}{2} = \frac{V_O(1 - D_{Bmax})}{2 f_s L_{max}}. \tag{4.131}$$

Using (4.22),

$$I_L = \frac{I_O}{1 - D}, \tag{4.132}$$

from which the dc output current at the boundary is obtained:

$$I_{OB} = I_{LB}(1 - D_{Bmax}) = \frac{V_O(1 - D_{Bmax})^2}{2 f_s L_{max}} = \frac{V_O}{R_{Lmin}}. \tag{4.133}$$

The load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2 f_s L}{(1 - D_{min})^2}. \tag{4.134}$$

Therefore, the maximum inductance L required for operation in DCM is

$$L_{max} = \frac{V_O(1 - D_{Bmax})^2}{2 f_s I_{OB}} = \frac{R_{Lmin}(1 - D_{Bmax})^2}{2 f_s}. \tag{4.135}$$

4.3.7 Power Losses and Efficiency of the Buck-boost Converter in DCM

Using (4.125), the peak inductor, switch, and diode current is

$$\Delta i_L = I_{SM} = I_{DM} = \frac{DV_I}{f_s L} = \frac{DV_O}{f_s L M_{V\,DC}} = V_O \sqrt{\frac{2}{f_s L R_L}}. \tag{4.136}$$

The rms value of the switch current is

$$I_{Srms} = \sqrt{\frac{1}{T} \int_0^{DT} i_S^2 \, dt} = \Delta i_L \sqrt{\frac{D}{3}} = V_O \sqrt{\frac{2D}{3 f_s L R_L}}. \tag{4.137}$$

Therefore, the MOSFET conduction loss is

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} \Delta i_L^2}{3} = \frac{2 r_{DS} D V_O^2}{3 f_s L R_L} = \frac{2 D r_{DS}}{3 f_s L} P_O = \frac{2 r_{DS}}{3} \sqrt{\frac{2}{f_s L R_L}} M_{V\,DC} P_O. \tag{4.138}$$

From (4.115) and (4.125), the switching loss is

$$P_{sw} = f_s C_o V_{SM}^2 = f_s C_o (V_I + V_O)^2 = f_s C_o V_O^2 \left(\frac{1}{M_{V\,DC}} + 1 \right)^2$$

$$= f_s C_o R_L \left(\frac{1}{M_{V\,DC}} + 1 \right)^2 P_O = f_s C_o R_L \left(\sqrt{\frac{2 f_s L}{D^2 R_L}} + 1 \right)^2 P_O. \tag{4.139}$$

The rms value of the diode current is

$$I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} i_D^2\, dt} = \Delta i_L \sqrt{\frac{D_1}{3}} = V_O \left(\frac{8}{9 f_s L R_L^3}\right)^{0.25}. \tag{4.140}$$

Hence, the power loss in the diode associated with R_F is

$$P_{RF} = R_F I_{Drms}^2 = \frac{D_1 R_F \Delta i_L^2}{3} = \frac{2R_F V_O^2}{3R_L}\sqrt{\frac{2}{f_s L R_L}} = \frac{2R_F}{3}\sqrt{\frac{2}{f_s L R_L}} P_O. \tag{4.141}$$

The average diode current is $I_D = I_O$, resulting in the diode loss associated with V_F,

$$P_{VF} = V_F I_D = V_F I_O = \frac{V_F}{V_O} P_O. \tag{4.142}$$

Thus the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = \left(\frac{V_F}{V_O} + \frac{2R_F}{3}\sqrt{\frac{2}{f_s L R_L}}\right) P_O. \tag{4.143}$$

Using (4.124) and (4.126), the rms value of the current through the inductor L is

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^{(D+D_1)T} i_L^2\, dt} = \Delta i_L \sqrt{\frac{D+D_1}{3}} = V_O \sqrt{\frac{2D}{3 f_s L R_L}\left(1 + \sqrt{\frac{2 f_s L}{D^2 R_L}}\right)}. \tag{4.144}$$

The power loss in the inductor ESR is therefore given by

$$\begin{aligned} P_{rL} = r_L I_{Lrms}^2 &= \frac{r_L \Delta i_L^2 (D+D_1)}{3} = \frac{2 r_L D V_O^2}{3 f_s L R_L}\left(1 + \sqrt{\frac{2 f_s L}{D^2 R_L}}\right) \\ &= \frac{2 r_L D}{3 f_s L}\left(1 + \sqrt{\frac{2 f_s L}{D^2 R_L}}\right) P_O = \frac{2 r_L}{3} M_{V\,DC}\sqrt{\frac{2}{f_s L R_L}}\left(1 + \frac{1}{M_{V\,DC}}\right) P_O. \end{aligned} \tag{4.145}$$

The total power loss in the converter is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} \\ &= \left[\frac{2 D r_{DS}}{3 f_s L} + \frac{2R_F}{3}\sqrt{\frac{2}{f_s L R_L}} + \frac{V_F}{V_O} + f_s C_o R_L \left(\sqrt{\frac{2 f_s L}{D^2 R_L}} + 1\right)^2 \right. \\ &\quad \left. + \frac{2 D r_L}{3 f_s L}\left(1 + \sqrt{\frac{2 f_s L}{D^2 R_L}}\right)\right] P_O \\ &= \left[\frac{2 r_{DS}}{3} M_{V\,DC}\sqrt{\frac{2}{f_s L R_L}} + \frac{2R_F}{3}\sqrt{\frac{2}{f_s L R_L}} + \frac{V_F}{V_O} + f_s C_o R_L \left(\frac{1}{M_{V\,DC}} + 1\right)^2 \right. \\ &\quad \left. + \frac{2 r_L}{3} M_{V\,DC}\sqrt{\frac{2}{f_s L R_L}}\left(1 + \frac{1}{M_{V\,DC}}\right)\right] P_O. \end{aligned} \tag{4.146}$$

This leads to the efficiency of the buck-boost converter in DCM,

$$\eta \equiv \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}$$

$$= \frac{1}{1 + \frac{2Dr_{DS}}{3f_sL} + \frac{2R_F}{3}\sqrt{\frac{2}{f_sLR_L}} + \frac{2Dr_L}{3f_sL}\left(1 + \sqrt{\frac{2f_sL}{D^2R_L}}\right) + \frac{V_F}{V_O} + f_sC_oR_L\left(\sqrt{\frac{2f_sL}{D^2R_L}} + 1\right)^2}$$

$$= \left[1 + \frac{2r_{DS}}{3}M_{V\,DC}\sqrt{\frac{2}{f_sLR_L}} + \frac{2R_F}{3}\sqrt{\frac{2}{f_sLR_L}} + \frac{2r_L}{3}M_{V\,DC}\sqrt{\frac{2}{f_sLR_L}}\left(1 + \frac{1}{M_{V\,DC}}\right) + \frac{V_F}{V_O} + f_sC_oR_L\left(\frac{1}{M_{V\,DC}} + 1\right)^2\right]^{-1}. \quad (4.147)$$

The dc input current is

$$I_I = \frac{1}{T}\int_0^{DT} i_I\,dt = \frac{1}{T}\int_0^{DT}\frac{V_I t}{L}\,dt = \frac{V_I D^2}{2f_sL}, \quad (4.148)$$

yielding the dc input power

$$P_I = V_I I_I = \frac{V_I^2 D^2}{2f_sL}. \quad (4.149)$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \quad (4.150)$$

The dc input power, dc output power, and the efficiency are related by

$$P_O = \eta P_I, \quad (4.151)$$

leading to

$$\frac{V_O^2}{R_L} = \frac{\eta V_I^2 D^2}{2f_sL}. \quad (4.152)$$

Hence, the dc voltage transfer function of lossy converter is

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = D\sqrt{\frac{\eta R_L}{2f_sL}} = D\sqrt{\frac{\eta V_O}{2f_sLI_O}} = \frac{D\sqrt{\frac{R_L}{2f_sL}}}{\sqrt{1 + \frac{2Dr_{DS}}{3f_sL} + \frac{2R_F}{3}\sqrt{\frac{2}{f_sLR_L}} + \frac{2Dr_L}{3f_sL}\left(1 + \sqrt{\frac{2f_sL}{D^2R_L}}\right) + \frac{V_F}{V_O} + f_sC_oR_L\left(\sqrt{\frac{2f_sL}{D^2R_L}} + 1\right)^2}}. \quad (4.153)$$

Thus,

$$D = M_{V\,DC}\sqrt{\frac{2f_sL}{\eta R_L}} = M_{V\,DC}\sqrt{\frac{2f_sLI_O}{\eta V_O}}. \quad (4.154)$$

4.3.8 Design of Buck-boost Converter for DCM

Design a PWM buck-boost converter that meets the following specifications: $V_I = 28\,\text{V}$ $\pm 4\,\text{V}$, $V_O = 12\,\text{V}$, $I_O = 0$ to $10\,\text{A}$, and $V_r/V_O \le 1\,\%$.

Solution. The maximum and minimum values of the output power are

$$P_{Omax} = V_O I_{Omax} = 12 \times 10 = 120\,\text{W} \tag{4.155}$$

and

$$P_{Omin} = V_O I_{Omin} = 12 \times 0 = 0\,\text{W}. \tag{4.156}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{10} = 1.2\,\Omega \tag{4.157}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{12}{0} = \infty. \tag{4.158}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{12}{32} = 0.375, \tag{4.159}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{12}{28} = 0.429, \tag{4.160}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{12}{24} = 0.5. \tag{4.161}$$

Assume the converter efficiency $\eta = 85\,\%$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{M_{V\,DCmin}}{M_{V\,DCmin} + \eta} = \frac{0.375}{0.375 + 0.85} = 0.306, \tag{4.162}$$

$$D_{nom} = \frac{M_{V\,DCnom}}{M_{V\,DCnom} + \eta} = \frac{0.429}{0.429 + 0.85} = 0.335, \tag{4.163}$$

and

$$D_{max} = \frac{M_{V\,DCmax}}{M_{V\,DCmax} + \eta} = \frac{0.5}{0.5 + 0.85} = 0.370. \tag{4.164}$$

Assuming the switching frequency $f_s = 100\,\text{kHz}$, the maximum inductance required for DCM operation is

$$L_{max} = \frac{R_{Lmin}(1 - D_{max})^2}{2f_s} = \frac{1.2 \times (1 - 0.370)^2}{2 \times 10^5} = 2.3814\,\mu\text{H}. \tag{4.165}$$

Pick $L = 2.2\,\mu\text{H}$.

At full load $R_L = R_{Lmin}$,

$$D_{max} = M_{V\,DCmax}\sqrt{\frac{2f_sL}{\eta R_{Lmin}}} = 0.5\sqrt{\frac{2 \times 10^5 \times 2.2 \times 10^{-6}}{0.85 \times 1.2}} = 0.328, \tag{4.166}$$

$$D_{nom} = M_{V\,DCnom}\sqrt{\frac{2f_sL}{\eta R_{Lmin}}} = 0.429\sqrt{\frac{2 \times 10^5 \times 2.2 \times 10^{-6}}{0.85 \times 1.2}} = 0.282, \tag{4.167}$$

$$D_{min} = M_{V\,DCmin}\sqrt{\frac{2f_sL}{\eta R_{Lmin}}} = 0.375\sqrt{\frac{2 \times 10^5 \times 2.2 \times 10^{-6}}{0.85 \times 1.2}} = 0.246, \tag{4.168}$$

and

$$D_{1max} = \sqrt{\frac{2f_sL}{\eta R_{Lmin}}} = \sqrt{\frac{2 \times 10^5 \times 2.2 \times 10^{-6}}{0.85 \times 1.2}} = 0.6568. \tag{4.169}$$

Hence,

$$D_{max} + D_{1max} = 0.328 + 0.6568 = 0.9848 < 1. \tag{4.170}$$

The current and voltage stresses of the semiconductor devices are

$$I_{SMmax} = I_{DMmax} = \Delta i_{Lmax} = \frac{V_{Imax}D_{min}}{f_sL} = \frac{32 \times 0.246}{10^5 \times 2.2 \times 10^{-6}} = 35.78\,\text{A} \tag{4.171}$$

and

$$V_{SMmax} = V_{DMmax} = V_O + V_{Imax} = 12 + 32 = 44\,\text{V}. \tag{4.172}$$

Select an International Rectifier IRF142 power MOSFET whose $V_{DSS} = 100\,\text{V}$, $I_{SM} = 24\,\text{A}$, $r_{DS} = 0.11\,\Omega$, $Q_g = 38\,\text{nC}$, and $C_o = 100\,\text{pF}$. Also select an MUR2510 ultrafast recovery diode whose $I_{F(AV)} = 25\,\text{A}$, $V_{DM} = 100\,\text{V}$, $V_F = 0.7\,\text{V}$, and $R_F = 20\,\text{m}\Omega$.

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{12}{100} = 120\,\text{mV}. \tag{4.173}$$

Assume that $V_{rcpp} = 100\,\text{mV}$. Hence, one obtains the maximum value of the ESR of the filter capacitor,

$$r_{Cmax} = \frac{V_{rcpp}}{I_{DMmax}} = \frac{100 \times 10^{-3}}{35.78} = 2.795\,\text{m}\Omega. \tag{4.174}$$

The ripple voltage across the filter capacitance is

$$V_{Cpp} = V_r - V_{rcpp} = 120 - 100 = 20\,\text{mV}, \tag{4.175}$$

and the filter capacitance is

$$C_{min} = \frac{D_{max}}{f_sR_{Lmin}}\frac{V_O}{V_{Cpp}} = \frac{0.328}{10^5 \times 1.2}\,\frac{12}{0.02} = 1.64\,\text{mF}. \tag{4.176}$$

Pick $C = 1.8\,\text{mF}/25\,\text{V}/2.5\,\text{m}\Omega$.

Power losses and efficiency will be calculated at full power and $V_{Imin} = 24\,\text{V}$ at which $D = D_{max} = 0.328$. The maximum conduction power loss in the MOSFET occurs at full load $R_{Lmin} = 1.2\,\Omega$ and $D_{max} = 0.328$ and is given by

$$P_{rDS} = \frac{2r_{DS}D_{max}V_O^2}{3f_sLR_{Lmin}} = \frac{2 \times 0.11 \times 0.328 \times 12^2}{3 \times 10^5 \times 2.2 \times 10^{-6} \times 1.2} = 13.12\,\text{W}. \tag{4.177}$$

The transistor output capacitance is $C_o = 100\,\text{pF}$. The switching loss occurs at $V_{Imin} = 24\,\text{V}$ and is given by

$$P_{sw} = f_sC_oV_{SMmin}^2 = f_sC_o(V_{Imin} + V_O)^2 = 10^5 \times 100 \times 10^{-12} \times (24 + 12)^2 = 12.96\,\text{mW}. \tag{4.178}$$

The power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 13.12 + \frac{0.013}{2} = 13.126\,\text{W}. \tag{4.179}$$

The diode conduction power loss due to R_F is

$$P_{RF} = \frac{2R_FV_O^2}{3R_{Lmin}}\sqrt{\frac{2}{f_sLR_{Lmin}}} = \frac{2 \times 0.02 \times 12^2}{3 \times 1.2}\sqrt{\frac{2}{10^5 \times 2.2 \times 10^{-6} \times 1.2}} = 4.404\,\text{W}, \tag{4.180}$$

and the diode conduction power loss due to V_F is

$$P_{VF} = V_F I_{Omax} = 0.7 \times 10 = 7\,\text{W}. \tag{4.181}$$

Hence, the total diode conduction power loss is

$$P_{Dmax} = P_{RF} + P_{VF} = 4.404 + 7 = 11.404\,\text{W}. \tag{4.182}$$

Assuming the ESR of the inductor $r_L = 10\,\text{m}\Omega$, the power loss in the inductor winding is

$$\begin{aligned} P_{rL} &= \frac{2r_L D_{max} V_O^2}{3 f_s L R_{Lmin}} \left(1 + \sqrt{\frac{2 f_s L}{D_{max}^2 R_{Lmin}}}\right) \\ &= \frac{2 \times 0.01 \times 0.328 \times 12^2}{3 \times 10^5 \times 2.2 \times 10^{-6} \times 1.2} \left(1 + \sqrt{\frac{2 \times 10^5 \times 2.2 \times 10^{-6}}{0.328^2 \times 1.2}}\right) \\ &= 3.397\,\text{W}. \end{aligned} \tag{4.183}$$

Neglecting the power loss in the filter capacitor, the total power loss in the converter is

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rL} = 13.12 + 0.013 + 11.404 + 3.397 = 27.932\,\text{W}. \tag{4.184}$$

The converter efficiency is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{120}{120 + 27.932} = 81.11\,\%. \tag{4.185}$$

Assuming that the peak-to-peak gate-to-source voltage is $V_{GSpp} = 14\,\text{V}$, the gate-drive power is

$$P_G = f_s V_{GSpp} Q_g = 10^5 \times 14 \times 38 \times 10^{-9} = 53.2\,\text{mW}. \tag{4.186}$$

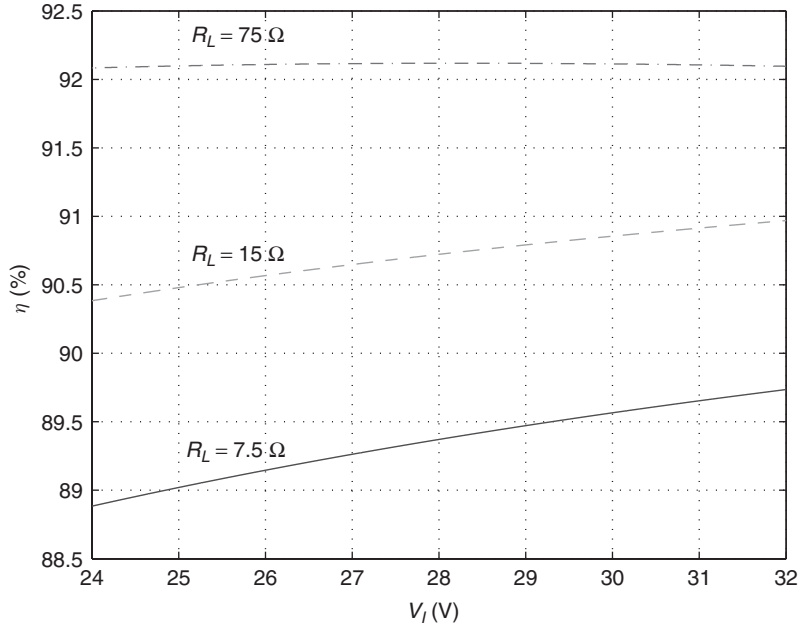


Figure 4.23 Efficiency η as a function of the dc input voltage V_I at fixed load resistances for the buck-boost converter in DCM.

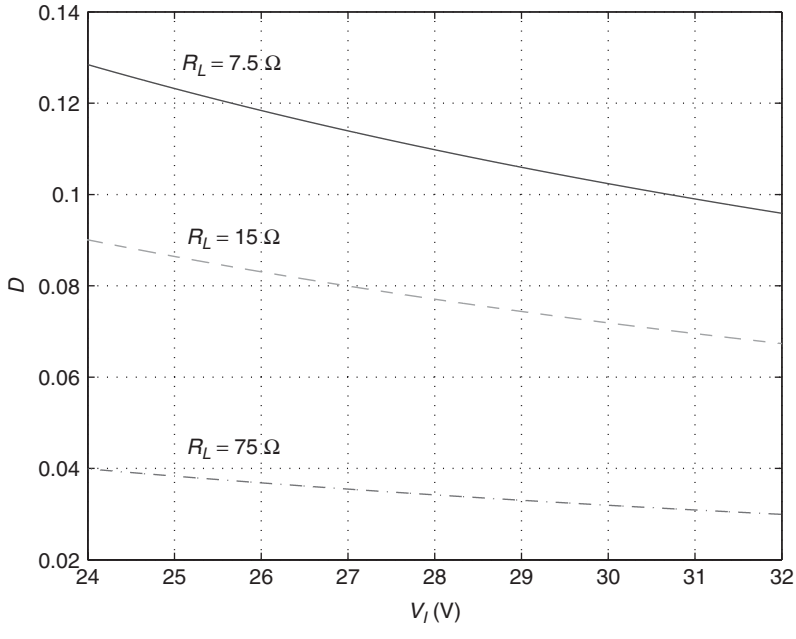


Figure 4.24 Duty cycle D as a function of the dc input voltage V_I at various load resistances for the buck-boost converter in DCM.

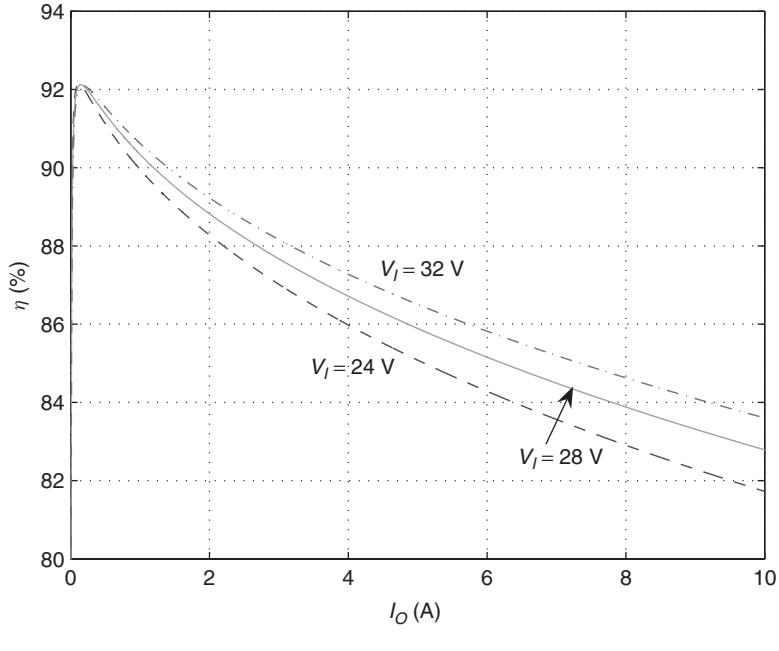


Figure 4.25 Efficiency η as a function of the dc load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in DCM.

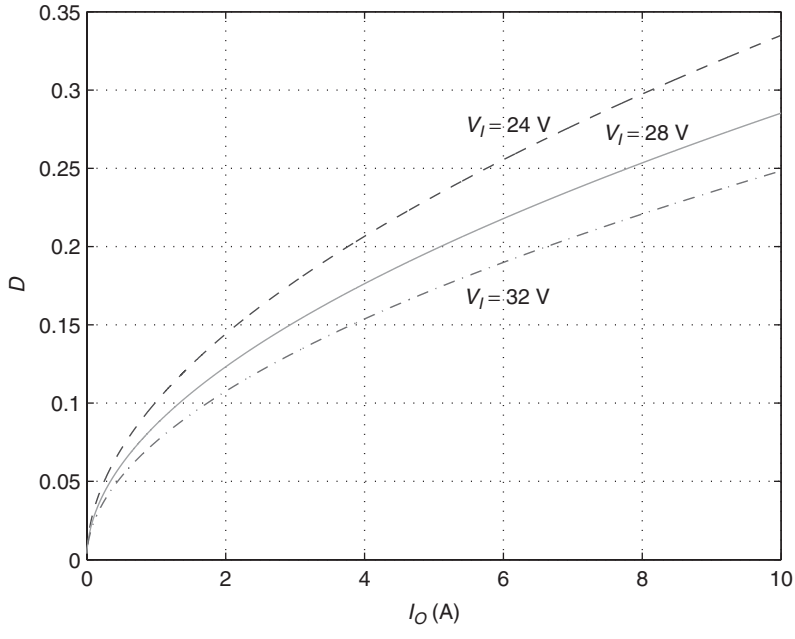


Figure 4.26 Duty cycle D as a function of the dc load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in DCM.

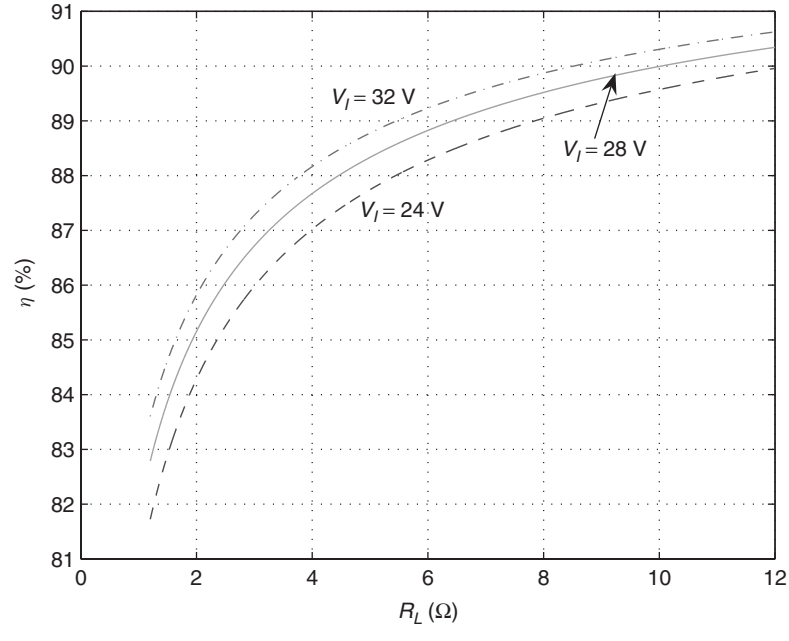


Figure 4.27 Efficiency η as a function of the load resistance R_L at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in DCM.

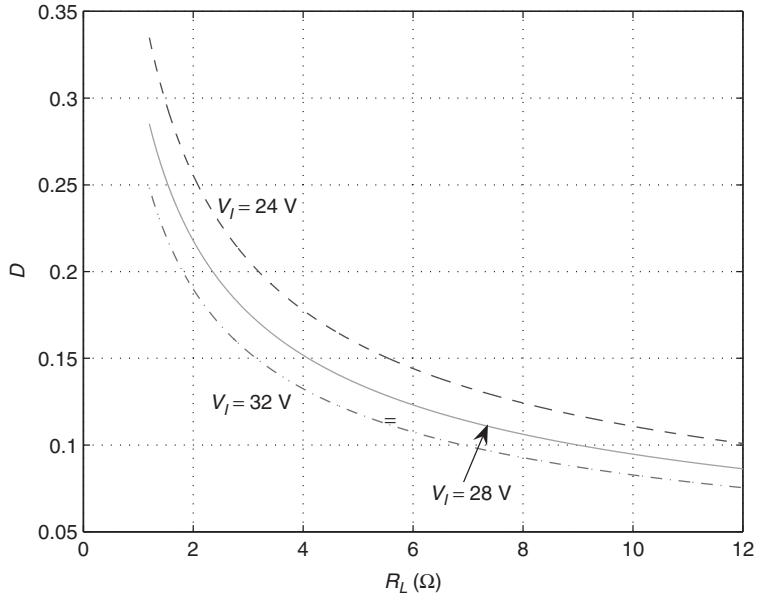


Figure 4.28 Duty cycle D as a function of the load resistance R_L at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$ for the buck-boost converter in DCM.

The converter efficiency η can be computed from (4.147) and the duty cycle D from (4.154). Plots of the efficiency η versus V_I at fixed load resistances are depicted in Figure 4.23. Figure 4.24 shows plot of D as V_I increases from 24 to 32 V for the buck-boost converter in CCM given in the design example. Figure 4.25 shows the plots of the efficiency η versus the load current I_O at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$. Figure 4.26 depicts plots of the duty cycle D as a function of the dc load current I_O for DCM at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$. Plots of the efficiency η versus R_L at fixed values of V_I are shown in Figure 4.27. Figure 4.28 exhibits the plots of the duty cycle D as a function of the load resistance R_L for DCM at $V_{Imin} = 24\,\text{V}$, $V_{Inom} = 28\,\text{V}$, and $V_{Imax} = 32\,\text{V}$.

4.4 Bidirectional Buck-boost Converter

A bidirectional buck-boost converter is shown in Figure 4.29. It is derived from the conventional unidirectional buck-boost converter of Figure 4.1(a) by replacing a diode with a

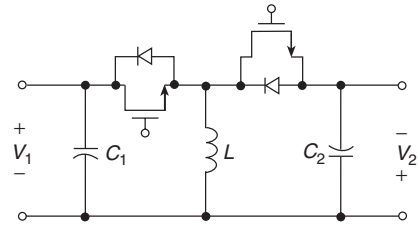


Figure 4.29 Bidirectional buck-boost converter.

MOSFET. If a dc voltage source is connected in parallel with the capacitor C_1 and a load is connected in parallel with the capacitor C_2, the energy flows from left to right. On the other hand, if a dc voltage source is connected in parallel with the capacitor C_2 and a load is connected in parallel with the capacitor C_1, the energy flows from right to left.

4.5 Synthesis of Buck-boost Converter

The buck-boost converter can be derived from the buck and boost converters [23]. The dc–dc voltage transfer function of the buck-boost converter for CCM can be represented as follows:

$$M_{V\,DC} = \frac{V_O}{V_I} = -\frac{D}{1-D} = (D)(-1)\left(\frac{1}{1-D}\right). \tag{4.187}$$

Hence, a block diagram of the buck-boost converter can be presented as in Figure 4.30, where $V_O < 0$. It consists of a converter with dc–dc voltage transfer function equal to D such as the buck converter, an inverting unity-gain block with a voltage transfer function equal to -1, and a converter with dc–dc voltage transfer function equal to $1/(1-D)$ such as the boost converter.

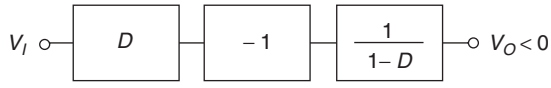


Figure 4.30 Block diagram of the buck-boost converter.

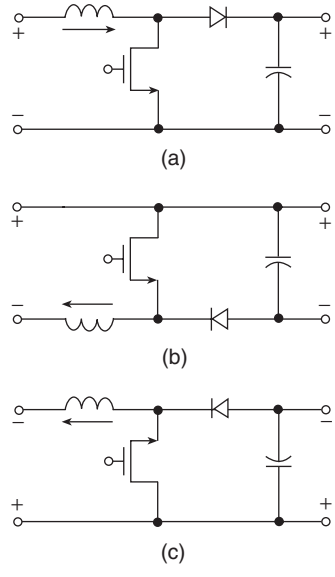


Figure 4.31 Transformation of the boost converter. (a) Boost converter with a positive input voltage. (b) Boost converter with inductor and diode moved to the bottom common rail. (c) Boost converter with a negative input voltage.

Due the presence of the inverting unity-gain block, the polarity of the boost converter input voltage should be opposite to that of the buck converter output voltage. Figure 4.31 shows the transformation of the boost converter from a circuit accepting a positive input voltage to a circuit accepting a negative input voltage. A conventional boost converter with a positive input voltage is depicted in Figure 4.31(a). In Figure 4.31(b), the inductor and the diode are moved to the common rail. In Figure 4.31(c), the converter is flipped over to obtain a circuit that accepts a negative input voltage.

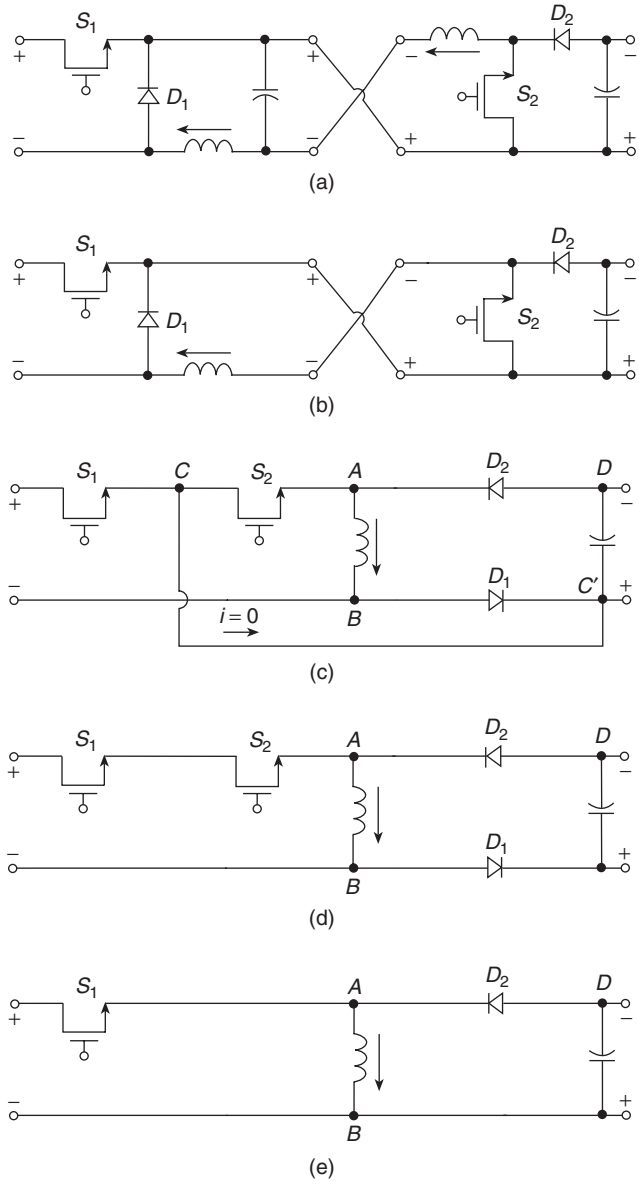


Figure 4.32 Derivation of the buck-boost converter. (a) Buck and modified boost converters connected by a unity-gain inverter. (b) Filter capacitor is removed from the circuit and two inductors are combined into one inductor. (c) Simplified circuit. (d) Conductor CC' is removed. (e) Redundant components S_2 and D_1 are removed.

Figure 4.32(a) shows the buck and modified boost converters connected by the unity-gain inverter, where the transistors in both the converters are synchronized to the same switching frequency f_s and have the same duty cycle D. The inductors in the buck and boost converters ideally act as current sources and the dc current through the filter capacitor of the buck converter is zero in steady-state operation. Therefore, the filter capacitor can be removed from the circuit and the two inductors can be combined into one inductor, as shown in Figure 4.32(b). A simplified circuit is shown in Figure 4.32(c). It can be seen that the current in the conductor CC' is zero and therefore this conductor can be removed from the circuit. When both transistors are OFF and both diodes are ON, the conductor is connected to an open circuit between the two transistors and conducts zero current. When both transistors are ON and both diodes are OFF, the conductor is connected to an open circuit between points B and C' and conducts no current. Therefore, this conductor can be removed from the circuit, as shown in Figure 4.32(d). Finally, the redundant components S_2 and D_1 can be removed to obtain the inverting buck-boost converter, as shown in Figure 4.32(e).

4.6 Synthesis of Boost-buck (Ćuk) Converter

A derivation of the boost-buck converter [24], known as the Ćuk converter, is shown in Figure 4.33. The dc–dc voltage transfer function of the boost-buck converter for CCM can be written as

$$M_{V\,DC} = \frac{V_O}{V_I} = \left(\frac{1}{1-D}\right)(-1)(D). \tag{4.188}$$

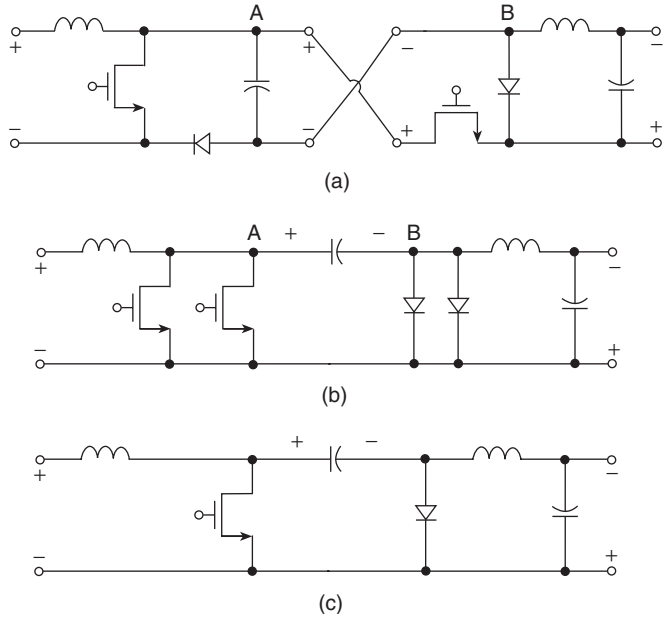


Figure 4.33 Derivation of the Ćuk (boost-buck) converter. (a) Cascaded boost converter, inverting unity-gain stage, and buck converter with negative input voltage. (b) Simplified circuit to reveal redundant components. (c) Ćuk (boost-buck) converter.

This equation represents the product of the dc voltage transfer functions of a boost converter, an inverting unity-gain stage, and a buck converter with negative input voltage, as shown in Figure 4.33(a). The circuit is redrawn in Figure 4.33(b) and reveals a redundant MOSFET and a redundant diode. Removing the redundant components, we obtain the boost-buck (Ćuk) converter shown in Figure 4.33(c). If we replace the horizontal capacitor by a series combination of two capacitors, a transformer can be inserted between the two capacitors and ground to obtain an isolated Ćuk converter.

4.7 Noninverting Buck-boost Converters

4.7.1 Cascaded Noninverting Buck-boost Converters

There is a great demand for a noninverting step-down/step-up dc–dc converter, especially for battery-powered portable electronics applications. For example, the voltage of the lithium-ion battery changes from 4.2 to 2.8 V and the supply voltage of an electronic circuit is 3.3 V. A noninverting step-down/step-up converter can be obtained by cascading the buck and boost converters. The output filter capacitor of the buck converter can be removed and the buck output filter inductor and the boost input filter inductor can be combined to obtain a noninverting buck-boost converter as shown in Figure 4.34(a). A noninverting boost-buck converter is shown in Figure 4.34(b). A noninverting synchronous boost-buck converter is shown in Figure 4.35.

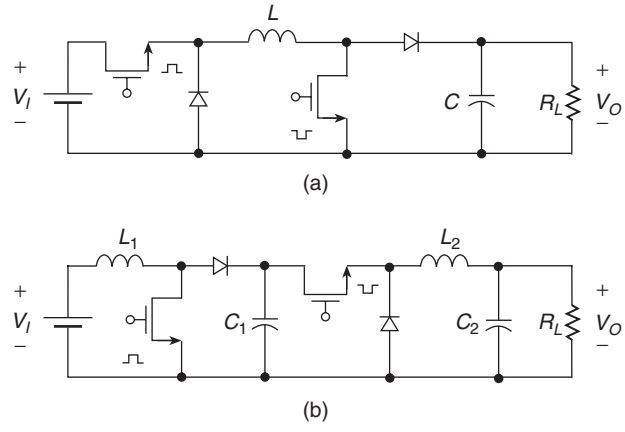


Figure 4.34 Noninverting cascaded buck-boost and boost-buck converters. (a) Noninverting buck-boost converter. (b) Noninverting boost-buck converter.

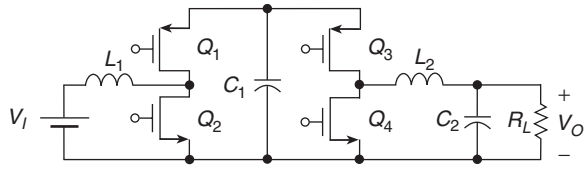


Figure 4.35 Noninverting cascaded synchronous CMOS boost-buck converter.

4.7.2 Four-transistor Noninverting Buck-boost Converters

A four-transistor CMOS noninverting buck-boost converter [26] is shown in Figure 4.36(a). It consists of four switches, an inductor L, and a filter capacitor C. Each pair of transistors is a CMOS inverter that consists of an NMOS and a PMOS. Synchronous rectification is employed to increase efficiency. This is a reconfigurable converter topology. If the transistor Q_3 is ON and the transistor Q_4 is OFF, a synchronous buck converter is obtained, as shown in Figure 4.36(b). The transistors Q_1 and Q_2 are used to control the duty cycle. If the transistor Q_1 is ON and the transistor Q_2 is OFF, a synchronous boost converter is obtained, as shown in Figure 4.36(c). The transistors Q_3 and Q_4 are used to control the duty cycle. The input voltage V_I is compared to a reference voltage to reconfigure the converter structure to the buck or boost converter. The smooth transition between the two converters may create a problem because it is difficult to achieve a duty cycle close to 0 in the boost converter and a duty cycle close to 1 in the buck converter for $V_I \approx V_O$. A four-transistor noninverting buck-boost converter with four NMOS transistors is shown in Figure 4.37.

The four-transistor noninverting buck-boost converter shown in Figure 4.38(a) can be operated in such a way that all transistors are switched in every cycle. When transistors Q_1 and Q_4 are ON and transistors Q_2 and Q_3 are OFF in every cycle, the inductor L is charged as shown Figure 4.38(b). When transistors Q_2 and Q_3 are ON and transistors Q_1 and Q_4 are OFF in every cycle, the inductor L is discharged into the capacitor C and the load resistor R_L, as shown in Figure 4.38(c). The efficiency of the converter in this mode of operation is reduced because all four switches turn on and off every cycle, increasing switching losses.

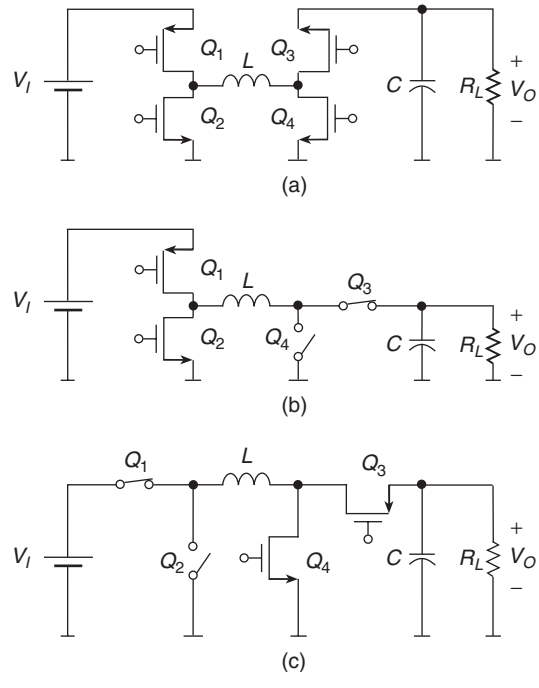


Figure 4.36 Four-transistor CMOS noninverting buck-boost converter. (a) Circuit. (b) Buck converter. (c) Boost converter.

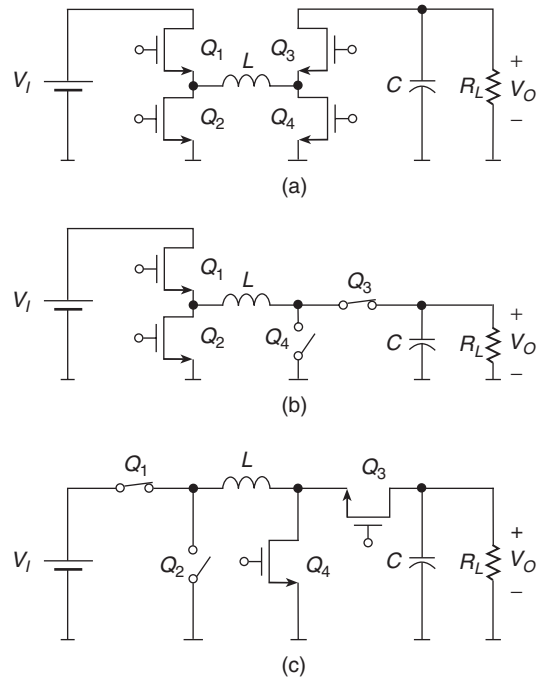


Figure 4.37 Four-transistor noninverting buck-boost converter with NMOS transistors. (a) Circuit. (b) Buck converter. (c) Boost converter.

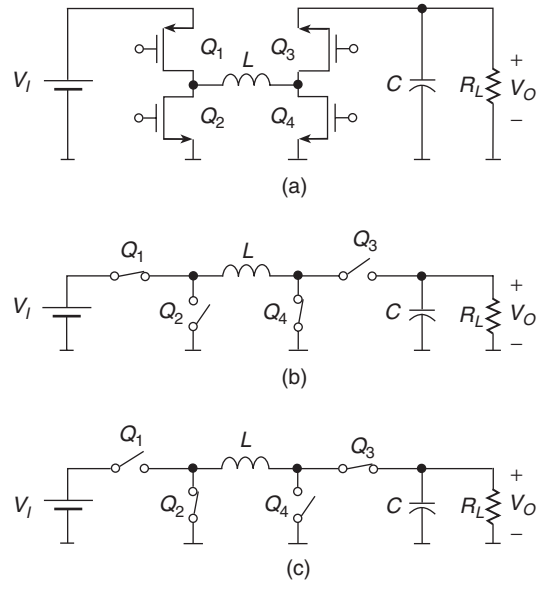


Figure 4.38 Four-transistor noninverting buck-boost converter. (a) Circuit. (b) When Q_1 and Q_4 are ON and Q_2 and Q_3 are OFF, the inductor is charged. (c) When Q_1 and Q_4 are OFF and Q_2 and Q_3 are ON, the inductor is discharged.

4.8 Tapped-inductor Buck-boost Converters

Tapped-inductor buck-boost converters are shown in Figure 4.39. The turns ratio of the tapped inductor is defined as

$$n = \frac{v}{v_s} = \frac{N_s + N_p}{N_s} = 1 + \frac{N_p}{N_s}. \tag{4.189}$$

4.8.1 Tapped-inductor Common-diode Buck-boost Converter

The tapped-inductor common-diode buck-boost converter is shown in Figure 4.39(a). When the MOSFET is ON,

$$v = V_I. \tag{4.190}$$

When the MOSFET is OFF,

$$v_s = V_O = \frac{v}{n}. \tag{4.191}$$

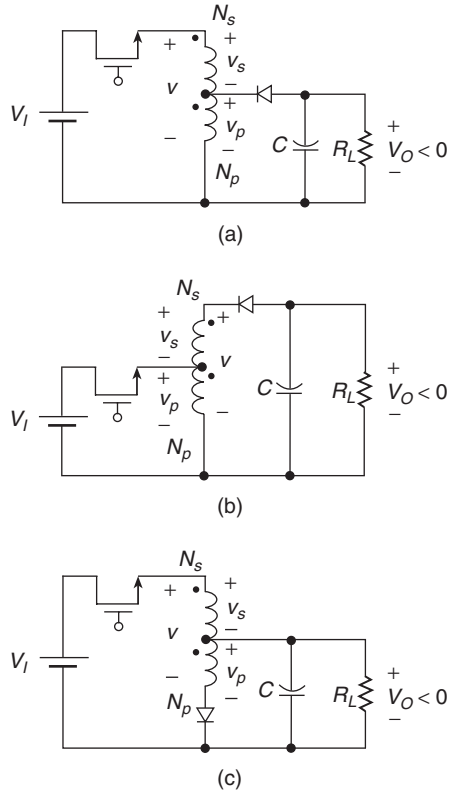


Figure 4.39 Tapped-inductor buck-boost converters. (a) Tapped-inductor common-diode buck-boost converter. (b) Tapped-inductor common-tansistor buck-boost converter. (c) Tapped-inductor common-load buck-boost converter.

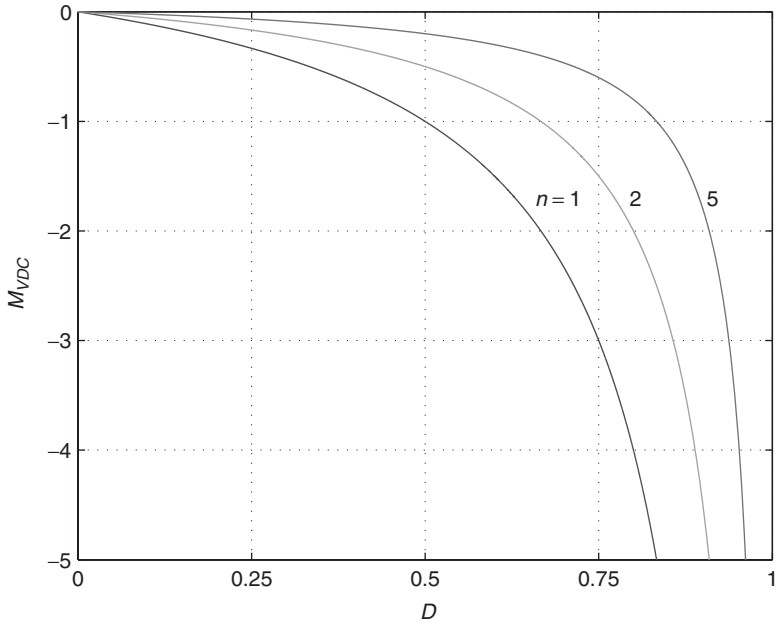


Figure 4.40 DC voltage transfer function of tapped-inductor common-diode buck-boost converter operating in CCM.

Hence,

$$V_I DT = -nV_O(1-D)T. \tag{4.192}$$

Thus, the dc voltage transfer function for CCM for the tapped-inductor common-diode buck-boost converter is

$$M_{V\,DC} = \frac{V_O}{V_I} = -\frac{D}{n(1-D)}. \tag{4.193}$$

Figure 4.40 shows $M_{V\,DC}$ as a function of D for the tapped-inductor common-diode converter operating in CCM.

4.8.2 Tapped-inductor Common-transistor Buck-boost Converter

The tapped-inductor common-transistor buck-boost converter is shown in Figure 4.39(b). When the MOSFET is ON,

$$v_s = V_I = \frac{v}{n}. \tag{4.194}$$

When the MOSFET is OFF,

$$v = V_O. \tag{4.195}$$

Hence,

$$nV_I DT = -V_O(1-D)T. \tag{4.196}$$

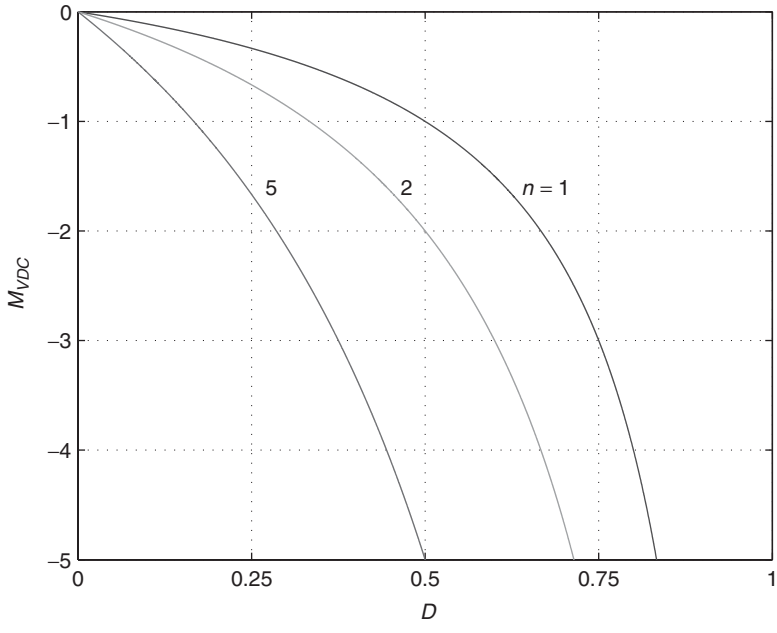


Figure 4.41 DC voltage transfer function of tapped-inductor common-transistor buck-boost converter operating in CCM.

The dc voltage transfer function for the tapped-inductor common-transistor buck-boost converter for CCM is

$$M_{V\,DC} = \frac{V_O}{V_I} = -\frac{nD}{1-D}. \tag{4.197}$$

This transfer function is identical to the dc voltage transfer function of the flyback converter. Figure 4.41 shows plots of $M_{V\,DC}$ as a function of D for the tapped-inductor common-transistor converter operating in CCM.

4.8.3 Tapped-inductor Common-load Buck-boost Converter

The tapped-inductor common-load buck-boost converter is shown in Figure 4.39(c). When the MOSFET is ON,

$$v_s = V_I - V_O = \frac{v}{n}. \tag{4.198}$$

When the MOSFET is OFF,

$$v_p = V_O = \frac{n-1}{n}v. \tag{4.199}$$

Hence,

$$n(V_I - V_O)DT = -V_O\frac{n}{n-1}(1-D)T. \tag{4.200}$$

The dc voltage transfer function of the tapped-inductor common-load buck-boost converter for CCM is

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D(n-1)}{n(1-D)}, \quad \text{for } D < \frac{1}{n}. \tag{4.201}$$

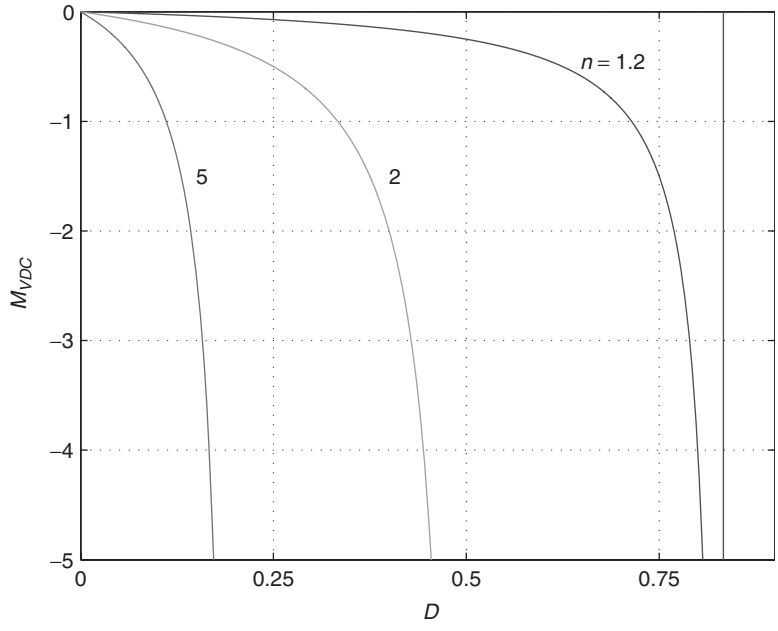


Figure 4.42 DC voltage transfer function of tapped-inductor common-load buck-boost converter operating in CCM.

Figure 4.42 shows plots of $M_{V\,DC}$ as a function of D for the tapped-inductor common-load buck-boost converter operating in CCM.

4.8.4 Tapped-inductor Common-source Buck-boost Converter

A tapped-inductor common-source buck-boost converter is shown in Figure 4.43 [28]. When the switch is ON,

$$v = nV_I. \tag{4.202}$$

When the switch is OFF,

$$v_s = V_O - V_I = \frac{n-1}{n}v, \tag{4.203}$$

which gives

$$v = \frac{n}{n-1}(V_O - V_I). \tag{4.204}$$

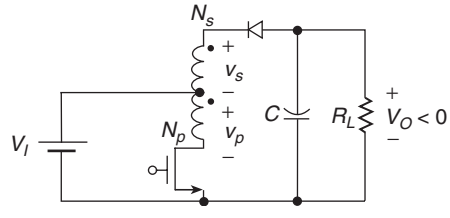


Figure 4.43 Tapped-inductor common-source buck-boost converter.

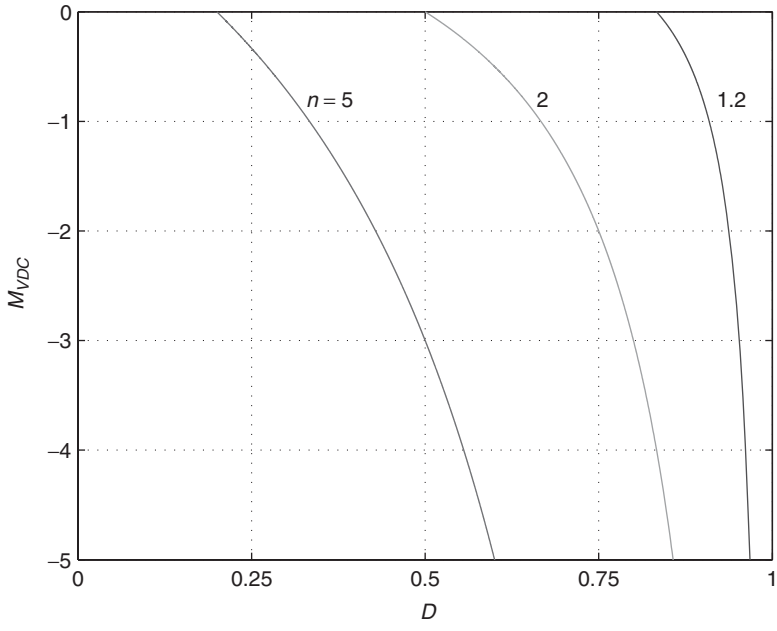


Figure 4.44 DC voltage transfer function of tapped-inductor common-source buck-boost converter operating in CCM.

Hence,

$$nV_I DT = -\frac{n}{n-1}(V_O - V_I)(1-D)T. \tag{4.205}$$

The dc voltage transfer function of the converter of the tapped-inductor common-source buck-boost converter operating in CCM is given by

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{1-nD}{1-D}, \quad \text{for } D > \frac{1}{n}. \tag{4.206}$$

Figure 4.44 shows plots of the dc voltage transfer function $M_{V\,DC}$ of the tapped-inductor common-source buck-boost converter for CCM. The noninverting flyback converter with two transformer terminals connected together belongs to the inductor-tapped buck-boost converter family.

4.9 Summary

- The buck-boost converter can be derived from the buck and boost converters.
- The buck-boost converter can be used either as a step-down or a step-up converter.
- It is an inverting converter.
- The inductor in the buck-boost converter can be replaced by a transformer, resulting in a flyback converter.
- For the lossless buck-boost converter, the dc voltage transfer function is $M_{V\,DC} = D/(1 - D)$ for CCM.

- For the lossy buck-boost converter, the dc voltage transfer has lower values than those for the lossless converter, especially when the duty cycle D is close to 1. For this reason, the maximum value of the dc voltage transfer function is limited.
- The converter should not be used at D close to 1 because its efficiency is poor for $D > 0.85$. Therefore, D is usually below 85 %.
- The peak-to-peak value of the current through the filter capacitor is very high, equal to the diode peak current I_{DM}.
- The input current is pulsating.
- It is relatively difficult to drive the transistor in the buck-boost converter because both the source and the gate of the transistor are connected to 'hot' points. Therefore, the driver is floating because neither end is connected to ground. Usually, a transformer or optical coupling is required.
- The inductance L for DCM is much lower than that for CCM.
- In DCM, D_1 is independent of D.
- The MOSFET and diode peak current for DCM is higher than that for CCM, by a factor of approximately 2.
- In DCM, the diode power loss is independent of the duty cycle, that is, V_I.

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4.11 Review Questions

4.1 What is the range of the dc voltage transfer function for the lossless and lossy buck-boost converter?

4.2 How does the efficiency of the buck-boost converter change with the duty cycle?

4.3 Is it difficult to drive the transistor in the buck-boost converter?

4.4 Is the input current of the buck-boost converter pulsating?

4.5 Is the current through the filter capacitor continuous in the buck-boost converter? What is the peak-to-peak value of the capacitor current?

4.6 Is only one-half of the $B-H$ curve of the inductor core utilized in the buck-boost converter?

4.7 Is the buck-boost converter an attractive type of converter? If so, explain why.

4.8 Is the corner frequency of the output filter dependent on the load resistance in the buck-boost converter?

4.9 When the polarity of the diode is reversed in the buck-boost converter, explain why the circuit obtained cannot function as a dc-dc converter.

4.12 Problems

4.1 A buck-boost PWM converter has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 1$ to 2 A, $\eta = 100\,\%$, and $f_s = 50$ kHz. Find the minimum inductance required for CCM operation.

4.2 A buck-boost PWM converter has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 1$ to 2 A, $\eta = 85\,\%$, and $f_s = 50$ kHz. Find the minimum inductance required for CCM operation.

4.3 A buck-boost PWM converter (given in Problem 4.1) has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 1$ to 2 A, $L = 420\,\mu$H, and $f_s = 50$ kHz. Find the voltage and current stresses of the transistor and the diode.

4.4 A buck-boost PWM converter (given in Problem 4.2) has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 1$ to 2 A, $L = 420\,\mu$H, and $f_s = 50$ kHz. Find the filter capacitance and the ESR so that $V_r/V_O \leq 1\,\%$.

4.5 A buck-boost PWM converter employs a filter capacitor with an ESR $r_C = 10\,\text{m}\Omega$. The load current is $I_O = 10$ A and the converter operates in CCM. Calculate the power loss in the filter capacitor at $D = 0.1$, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, and 0.9.

4.6 A buck-boost PWM converter has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 0$ to 2 A, $\eta = 100\,\%$, and $f_s = 50$ kHz. Find the maximum inductance required for DCM operation.

4.7 A buck-boost PWM converter has $V_I = 127$ to 187 V, $V_O = 48$ V, $I_O = 0$ to 2 A, $\eta = 85\,\%$, and $f_s = 50$ kHz. Find the maximum inductance required for DCM operation.

4.8 Derive an expression for the dc voltage transfer function of the lossless and lossy buck-boost PWM converter operating in DCM using the principle of energy conservation.

4.9 A buck-boost PWM converter has $V_I = 42$ to 60 V, $V_O = 28$ V, $I_O = 0.2$ to 2 A, $V_r/V_O \leq 1\,\%$, $r_{DS} = 0.1\,\Omega$, $R_F = 35\,\text{m}\Omega$, $V_F = 0.7$ V, $r_L = 12\,\text{m}\Omega$, $C_o = 200$ pF, and $f_s = 100$ kHz. Find the converter efficiency.

4.10 A buck-boost converter has $V_I = 42$ to 60 V, $V_O = 28$ V, $I_O = 0.2$ to 2 A, $r_{DS} = 0.2\,\Omega$, $R_F = 20\,\text{m}\Omega$, $V_F = 0.7$ V, $r_L = 0.15\,\Omega$, $r_C = 25\,\text{m}\Omega$, $C_o = 200$ pF, $V_r/V_O \leq 1\,\%$, and $f_s = 100$ kHz. Find L, C, I_{SM}, V_{SM}, and η.

4.11 Design a buck-boost PWM converter to meet the following specifications: $V_{Imin} = 42$ V, $V_{Inom} = 48$ V, $V_{Imax} = 60$ V, $V_O = 28$ V, $I_O = 0.2$ to 2 A, $V_r/V_O \leq 1.5\,\%$, $f_s = 100$ kHz, $r_L = 0.32\,\Omega$, $r_C = 33\,\text{m}\Omega$, $r_{DS} = 0.4\,\Omega$, $R_F = 20\,\text{m}\Omega$, $V_F = 0.7$ V, and $C_o = 100$ pF.

4.12 In a buck-boost converter, $V_I = 48 \pm 6$ V, $V_O = 12$ V, $I_O = 0.4$ to 4 A, $V_r/V_O \leq 1\,\%$, and $f_s = 200$ kHz. Find L, C, and r_{Cmax}.

5

Flyback PWM DC–DC Converter

5.1 Introduction

A PWM flyback dc–dc converter [1]–[22] is a transformer (or isolated) version of the buck-boost converter. A transformer is used to eliminate any direct electrical connection between the input and the output of the converter power stage. This safety feature is required in many applications. For example, 1.5 kV dc isolation is typical for worldwide compliance. The safety standard in the US is regulated by Underwriters Laboratories (UL). For most worldwide system applications, power supplies should satisfy the following safety agency standards: UL1950, VDE0805 (EN60950, IEC950), and CSA C22.2, No. 950-95. In addition, the transformer allows the converters to achieve much higher or lower values of the dc voltage transfer function than their transformerless counterparts. Since the operating frequency of PWM converters is much higher than 50–60 Hz line frequency, the transformer, inductors, and capacitors are much smaller than those operated at line frequencies. The transformer performs several functions in the flyback converter:

- It provides dc isolation.
- It stores the magnetic energy.
- It changes the voltage levels.
- The output voltages can be either positive or negative.
- Additional secondary transformer windings and rectifiers may be added to provide more than one output voltage of any polarity.

A multiple-output transformer allows one switching-mode power supply to provide all the voltages required by most product designs, for example, 5 V, −5 V, 12 V, and −12 V. The flyback converter is used in low-power applications, typically from 20 to 200 W. It has

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a low parts count. The magnetizing inductance of the transformer is used to store magnetic energy, and therefore, an inductor is not required. However, a large transformer core is needed for higher power levels. An air gap is normally used to avoid core saturation. The voltage stress of the switch is high. The flyback converter is widely used in computers, TV sets, and other electronic equipment.

5.2 Transformers

Let us consider an ideal noninverting transformer as shown in Figure 5.1(a). In an ideal transformer, both coils share precisely the same magnetic flux $\phi = \phi_{21} = \phi_{12}$ and have the coupling coefficient $k = 1$. The voltages of the transformer are given by

$$v_1 = N_1 \frac{d\phi}{dt} \tag{5.1}$$

and

$$v_2 = N_2 \frac{d\phi}{dt}, \tag{5.2}$$

where N_1 is the number of turns of the primary winding and N_2 is the number of turns of the secondary winding. The ratio of the two voltages is

$$\frac{v_1}{v_2} = \frac{N_1 \dfrac{d\phi}{dt}}{N_2 \dfrac{d\phi}{dt}} = \frac{N_1}{N_2} = n, \tag{5.3}$$

where n is the transformer turns ratio.

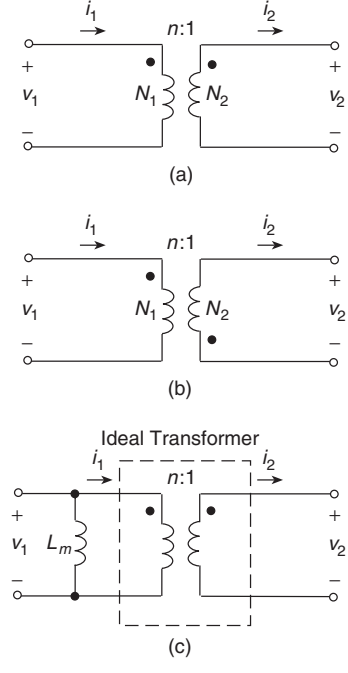


Figure 5.1 Transformer. (a) Ideal noninverting transformer. (b) Ideal inverting transformer. (c) Model of a transformer consisting of an ideal noninverting transformer and a magnetizing inductance L_m.

The instantaneous input power of the transformer is $P_i = i_1 v_1$ and the instantaneous output power of the transformer is $P_o = i_2 v_2$. Assuming that the efficiency of the transformer $\eta = P_o/P_i = 1$, one obtains

$$i_1 v_1 = i_2 v_2, \tag{5.4}$$

from which the ratio of the voltages and currents is given by

$$\frac{v_1}{v_2} = \frac{i_2}{i_1}. \tag{5.5}$$

From (5.3) and (5.5), one obtains the relationship among voltages, currents, and turns ratio for the ideal noninverting transformer,

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{N_1}{N_2} = n. \tag{5.6}$$

Figure 5.1(b) shows an ideal inverting transformer. The input voltage is given by (5.1) and the output voltage is

$$v_2 = -N_2 \frac{d\phi}{dt}. \tag{5.7}$$

Equations (5.4) and (5.5) hold here, too. Therefore, the relationship for the ideal inverting transformer is given by

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = -\frac{N_1}{N_2} = -n. \tag{5.8}$$

Thus, v_2 is out of phase by 180° with respect to v_1 and i_2 is out of phase by 180° with respect to i_1.

A complete model of an actual transformer contains a number of components such as magnetizing inductance, core resistance, resistances of the windings, leakage inductances, and stray capacitances. A simple transformer model, shown in Figure 5.1(c), is usually used for analysis of PWM converters. It consists of an ideal transformer and a magnetizing inductance L_m. This model reflects the ability of the transformer to store magnetic energy in L_m and to transform the ac current and voltage levels.

5.3 DC Analysis of PWM Flyback Converter for CCM

5.3.1 Derivation of PWM Flyback Converter

Figure 5.2 shows the derivation of the PWM flyback converter. The PWM buck-boost converter is shown in Figure 5.2(a). It is an inverting dc–dc converter. Its disadvantage is that the gate is driven with respect to a 'hot' point. The inductor may be replaced by a noninverting transformer in the buck-boost converter, resulting in an inverting flyback PWM converter. The transformer magnetizing inductance L_m can be used to store the magnetic energy. Gapped cores are usually used to obtain a low magnetizing inductance L_m. The converter of Figure 5.2(b) has a gate driven with respect to a 'hot' point as the buck-boost converter. This circuit can be redrawn so that the gate is driven with respect to ground, as depicted in Figure 5.2(c), because the switch and the primary of the transformer are connected in series. If the direction of the diode and the filter capacitor (if it is an electrolytic capacitor) is reversed, and the polarity of the transformer is reversed, a noninverting flyback PWM converter is obtained as shown in Figure 5.2(d).

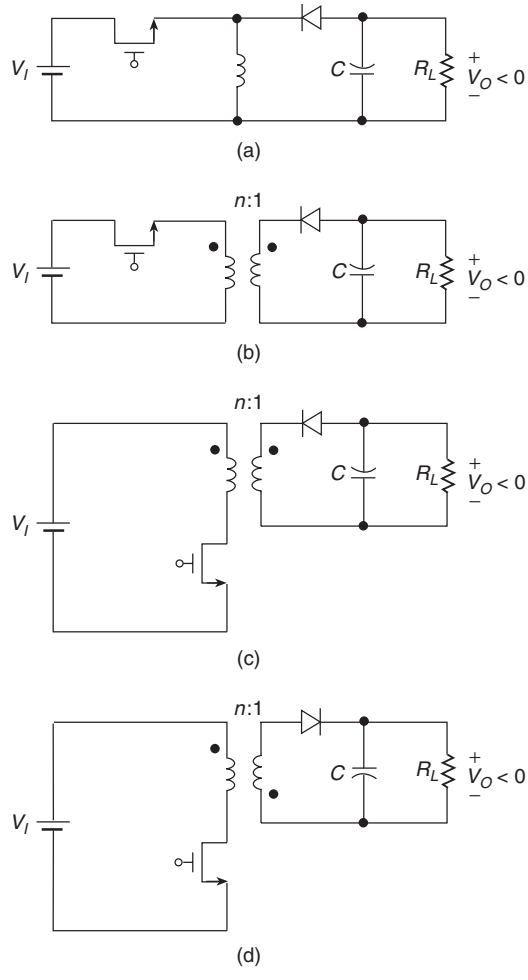


Figure 5.2 Derivation of the PWM flyback converter from the PWM buck-boost converter. (a) Buck-boost converter. (b) Flyback inverting converter. (c) Flyback inverting converter with the gate driven with respect to ground. (d) Flyback noninverting converter with the gate driven with respect to ground.

To accomplish dc isolation between the input and the output, a control circuit must also have dc isolation. Optocouplers or transformers are used to provide dc isolation in a control circuit. The transformer can have many secondary windings, and therefore a flyback converter can have multiple outputs. Some of them can have positive voltages and others negative voltages, depending upon the polarity of secondary outputs.

5.3.2 Circuit Description

An equivalent circuit of the non-inverting PWM flyback dc–dc converter is depicted in Figure 5.3. It consists of a power MOSFET operated as a switch, a transformer, a diode, and a filter capacitor C. The transformer performs two functions: it provides dc isolation and stores the magnetic energy. It is the simplest transformer-isolated converter. The power

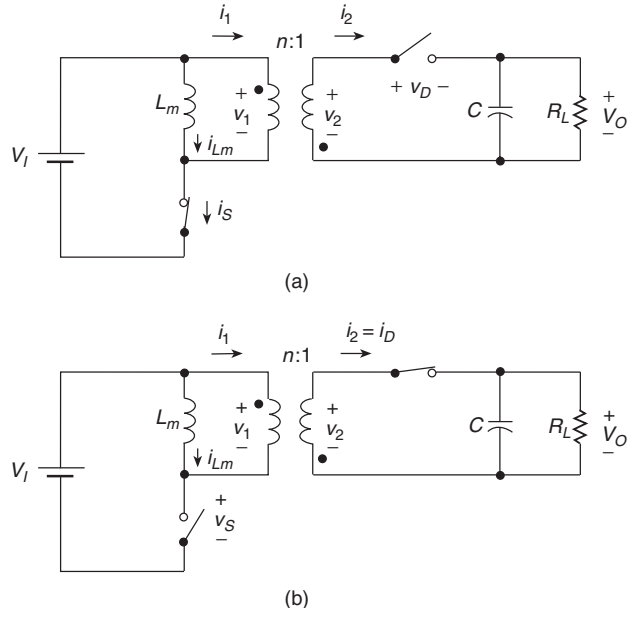


Figure 5.3 Equivalent circuits of the noninverting PWM flyback converter for CCM. (a) Equivalent circuit when the switch is ON and the diode is OFF. (b) Equivalent circuit when the switch is OFF and the diode is ON.

level for the flyback converter is usually between 20 and 200 W. There are two modes of operation: CCM and DCM. Figure 5.3(a)–(b) shows equivalent circuits of the non-inverting flyback converter of Figure 5.2(d) for CCM when the switch is ON and the diode is OFF, and when the switch is OFF and the diode is ON, respectively. The transformer is modeled by an ideal transformer and its magnetizing inductance L_m. The principle of operation of the flyback converter is explained by the idealized waveforms of the currents and voltages shown in Figure 5.4. During the time interval $0 < t \leq DT$, the switch is ON and the diode is OFF, as indicated in Figure 5.3(a). The voltage across the diode is $-(V_I/n + V_O)$, which maintains the diode in the off-state. The voltage across the magnetizing inductance L_m is V_I and gives rise to a linear increase in the magnetizing inductance current with a slope of V_I/L_m. During the time interval $DT < t \leq T$, the switch is OFF and the diode is ON, as shown in Figure 5.3(b). The voltage across the magnetizing inductance L_m is $-nV_O$, which causes the magnetizing inductance current to decrease linearly with a slope of $-nV_O/L_m$. The voltage across the switch is $V_I + nV_O$. At time $t = T$, the switch is turned on again and the next cycle begins.

5.3.3 Assumptions

The analysis of the flyback PWM converter of Figure 5.3(a) is based on the following assumptions:

1. The power MOSFET and the diode are ideal switches.
2. The transistor output capacitance, the diode capacitance, and lead inductances (and thus switching losses) are zero.

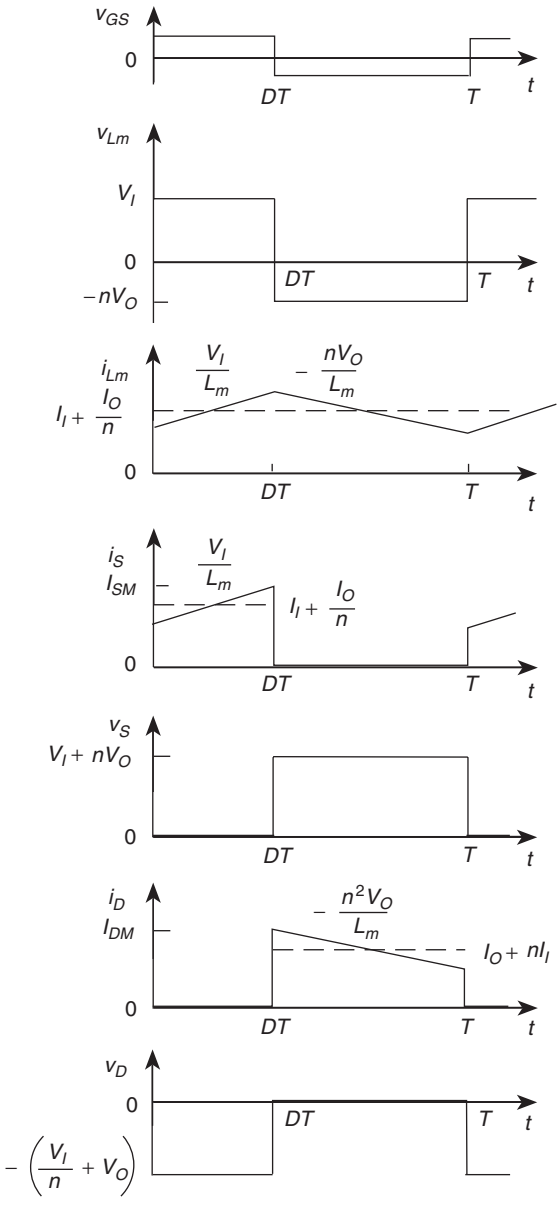


Figure 5.4 Idealized current and voltage waveforms in the PWM inverting flyback converter for CCM.

3. The transformer leakage inductances and the stray capacitances are neglected.
4. Passive components are linear, time-invariant, and frequency-independent.
5. The output impedance of the input voltage source V_I is zero for both dc and ac components.

5.3.4 Time Interval 0 < t ≤ DT

During the time interval $0 < t \leq DT$, the switch is ON and the diode OFF. An ideal equivalent circuit for this time interval is shown in Figure 5.3(a). When the switch is ON, the voltage across the diode v_D is approximately equal to $-(V_I/n + V_O)$, causing the diode to be reverse biased. The voltage across the switch v_S and the diode current are zero. From

$$i_D = i_2 = 0, \tag{5.9}$$

it follow that

$$i_1 = \frac{i_2}{-n} = 0. \tag{5.10}$$

The voltage across the magnetizing inductance L_m is given by

$$v_{Lm} = V_I = L_m \frac{di_{Lm}}{dt}. \tag{5.11}$$

Hence, one obtains the current through the magnetizing inductance L_m and the switch,

$$i_S = i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}dt + i_{Lm}(0) = \frac{1}{L_m}\int_0^t V_I dt + i_{Lm}(0) = \frac{V_I}{L_m}t + i_{Lm}(0), \tag{5.12}$$

where $i_{Lm}(0)$ is the initial current in the magnetizing inductance L_m at time $t = 0$. The peak current of the magnetizing inductance is

$$i_{Lm}(DT) = \frac{V_I DT}{L_m} + i_{Lm}(0) = \frac{V_I D}{f_s L_m} + i_{Lm}(0), \tag{5.13}$$

and the peak-to-peak value of the ripple current through the magnetizing inductance L_m is

$$\Delta i_{L_m} = i_{Lm}(DT) - i_{Lm}(0) = \frac{V_I DT}{L_m} = \frac{V_I D}{f_s L_m}. \tag{5.14}$$

It will shortly be shown that the dc voltage transfer function of the flyback converter is $M_{V\,DC} = V_O/V_I = I_I/I_O = D/[n(1-D)]$. Hence, we can find the peak value of the diode reverse voltage,

$$V_{DM} = -\left(\frac{V_I}{n} + V_O\right) = -\frac{V_O}{D}, \tag{5.15}$$

from which

$$V_{DMmax} = -\left(\frac{V_{Imax}}{n} + V_O\right) = -\frac{V_O}{D_{min}}. \tag{5.16}$$

The peak value of the switch current I_{SM} is

$$I_{SM} = I_I + \frac{I_O}{n} + \frac{\Delta i_{Lm}}{2} = \frac{I_O}{n(1-D)} + \frac{\Delta i_{Lm}}{2}, \tag{5.17}$$

which gives

$$I_{SMmax} = I_{Imax} + \frac{I_{Omax}}{n} + \frac{\Delta i_{Lm}}{2} = \frac{I_{Omax}}{n(1-D_{max})} + \frac{\Delta i_{Lm(max)}}{2}. \tag{5.18}$$

The increase in the magnetic energy in the magnetizing inductance L_m is

$$\Delta W_{Lm(in)} = \frac{1}{2}L_m[i_{Lm}^2(DT) - i_{Lm}^2(0)]. \tag{5.19}$$

This time interval is terminated at $t = DT$ when the switch is turned off by an external driver. The current through the magnetizing inductance i_{Lm} is a continuous function of time and because $i_{Lm}(DT)$ is nonzero, it acts as a current source, thus turning on the diode.

5.3.5 Time Interval DT < t ≤ T

During the time interval $DT < t \leq T$, the switch is OFF and the diode is ON. Figure 5.3(b) shows an ideal equivalent circuit for this time interval. The switch current i_S and the diode voltage v_D are zero. The voltage across the secondary of the transformer is

$$v_2 = V_O, \tag{5.20}$$

resulting in the voltage across the primary of the transformer,

$$v_1 = -nv_2 = -nV_O. \tag{5.21}$$

Therefore, the voltage across the magnetizing inductance L_m is

$$v_{Lm} = -nV_O = L_m \frac{di_{Lm}}{dt}. \tag{5.22}$$

The current through the magnetizing inductance L_m can be found to be

$$\begin{aligned} i_{Lm} &= \frac{1}{L_m}\int_{DT}^{t} v_{Lm}\,dt + i_{Lm}(DT) = \frac{1}{L_m}\int_{DT}^{t}(-nV_O)dt + i_{Lm}(DT) \\ &= -\frac{nV_O}{L_m}(t - DT) + i_{Lm}(DT) = -\frac{nV_O}{L_m}(t - DT) + \frac{V_I D}{f_s L_m} + i_{Lm}(0), \end{aligned} \tag{5.23}$$

where $i_{Lm}(DT)$ is the initial current of the magnetizing inductance L_m at $t = DT$. The peak-to-peak value of the ripple current through the magnetizing inductance L_m is

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(T) = \frac{nV_O T(1 - D)}{L_m} = \frac{nV_O(1 - D)}{f_s L_m}. \tag{5.24}$$

The current of the primary of the ideal transformer is

$$i_1 = -i_{Lm} = \frac{nV_O}{L_m}(t - DT) - i_{Lm}(DT), \tag{5.25}$$

which leads to the secondary and the diode current,

$$i_D = i_2 = -ni_1 = ni_{Lm} = -\frac{n^2 V_O}{L_m}(t - DT) + ni_{Lm}(DT). \tag{5.26}$$

Because $V_O/V_I = D/n(1 - D)$, the peak voltage across the switch S is given by

$$V_{SM} = V_I + nV_O = \frac{nV_O}{D}, \tag{5.27}$$

resulting in a maximum value of the peak voltage across the switch,

$$V_{SMmax} = V_{Imax} + nV_O = \frac{nV_O}{D_{min}}. \tag{5.28}$$

The peak diode current is

$$I_{DM} = nI_I + I_O + \frac{n\,\Delta i_{Lm}}{2} = \frac{I_O}{1 - D} + \frac{n\,\Delta i_{Lm}}{2}, \tag{5.29}$$

which in the worst case becomes

$$I_{DMmax} = nI_{Imax} + I_{Omax} + \frac{n\,\Delta i_{Lm(max)}}{2} = \frac{I_{Omax}}{1 - D_{max}} + \frac{n\,\Delta i_{Lm(max)}}{2}. \tag{5.30}$$

This time interval ends at $t = T$ when the switch is turned on by a external driver.

The decrease in the magnetic energy stored in the magnetizing inductance L_m during interval $DT < t \leq T$ is

$$\Delta W_{Lm(out)} = \frac{1}{2} L_m [i_{Lm}^2(DT) - i_{Lm}^2(T)]. \tag{5.31}$$

In steady-state operation, the increase in the stored magnetic energy in the magnetizing inductance $\Delta W_{Lm(in)}$ is equal to the decrease in the stored magnetic energy in the inductance $\Delta W_{Lm(out)}$.

5.3.6 DC Voltage Transfer Function for CCM

Referring to Figure 5.4 and using a volt-second balance, $A^+ = A^-$, we can write

$$DTV_I = (1 - D)TnV_O, \tag{5.32}$$

which can be rearranged as

$$V_O = \frac{DV_I}{n(1 - D)}, \tag{5.33}$$

resulting in the dc voltage transfer function of the lossless converter,

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{n(1 - D)}. \tag{5.34}$$

The range of $M_{V\,DC}$ for the lossless flyback converter for $0 \leq D \leq 1$ is

$$0 \leq M_{V\,DC} < \infty. \tag{5.35}$$

Notice that the plot of $nM_{V\,DC} = D/(1 - D)$ is the same as that of the dc voltage transfer function $M_{V\,DC} = D/(1 - D)$ for the buck-boost converter given in Chapter 4. It follows from (5.33) that the output voltage V_O is independent of the load resistance R_L and depends only on the dc input voltage V_I. It will shortly be shown that $M_{V\,DC}$ is significantly altered by losses, especially at the values of D close to 1. From (5.34),

$$D = \frac{nM_{V\,DC}}{nM_{V\,DC} + 1}. \tag{5.36}$$

The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = \frac{V_I}{n(1 - D)^2}. \tag{5.37}$$

In practice, V_O should be held constant. If V_I increases, D should be decreased by a control circuit so that V_O remains constant, and vice versa. The dc current transfer function is

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n(1 - D)}{D}, \tag{5.38}$$

and its value decreases from ∞ to 0 as D is increased from 0 to 1.

Using (5.34),

$$\frac{V_O}{V_{SM}} = \frac{V_O}{V_I + nV_O} = \frac{1}{n + \dfrac{V_I}{V_O}} = \frac{D}{n}, \tag{5.39}$$

and using (5.38),

$$\frac{I_O}{I_{SM}} \approx \frac{I_O}{I_I + \dfrac{I_O}{n}} = \frac{n}{1 + \dfrac{nI_I}{I_O}} = n(1 - D). \tag{5.40}$$

Thus, the switch and the diode utilization in the flyback converter is characterized by the output-power capability

$$c_p \equiv \frac{P_O}{V_{SM}I_{SM}} = \frac{V_O I_O}{V_{SM}I_{SM}} = D(1-D). \tag{5.41}$$

As D is increased from 0 to 1, c_p increases from 0, reaches a maximum equal to 0.25 at $D = 0.5$, and then decreases back to zero.

5.3.7 Boundary between CCM and DCM

Figure 5.5 depicts the current waveform of the magnetizing inductance at the CCM/DCM boundary for the flyback converter. This waveform can be described by

$$i_{Lm} = \frac{V_I}{L_m}t, \qquad \text{for } 0 < t \le DT. \tag{5.42}$$

Using (5.34), $V_I = nV_O(1-D)/D$. Hence,

$$\Delta i_{Lm} = i_{Lm}(DT) = \frac{nV_O(1-D)}{f_s L_m}, \tag{5.43}$$

resulting in

$$\Delta i_{Lm(max)} = \frac{nV_O(1-D_{min})}{f_s L_{m(min)}}. \tag{5.44}$$

The dc current through the magnetizing inductance at the CCM/DCM boundary is

$$I_{LmB} = \frac{\Delta i_{Lm(max)}}{2}. \tag{5.45}$$

The energy transferred from the input dc voltage source V_I to the magnetizing inductance during one cycle for the boundary case is

$$W_{OB} = \frac{L_{m(min)}\Delta i^2_{Lm(max)}}{2}, \tag{5.46}$$

which results in dc output power at the boundary given by

$$\begin{aligned} P_{OB} &= \frac{W_{OB}}{T} = f_s W_{OB} = \frac{f_s L_{m(min)}\Delta i^2_{Lm(max)}}{2} \\ &= \frac{f_s L_{m(min)} n^2 V_O^2 (1-D_{min})^2}{2f_s^2 L^2_{m(min)}} = \frac{n^2 V_O^2 (1-D_{min})^2}{2f_s L_{m(min)}}. \end{aligned} \tag{5.47}$$

On the other hand, the dc power transferred from the converter to the load at the CCM/DCM boundary can be expressed as

$$P_{OB} = \frac{V_O^2}{R_{Lmax}} = \frac{V_O^2}{R_{OB}}, \tag{5.48}$$

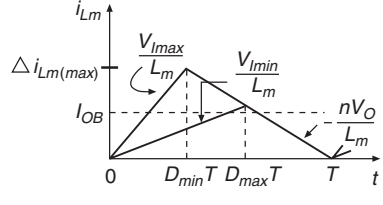


Figure 5.5 Waveform of the current through the magnetizing inductance L_m at the CCM/DCM boundary for the flyback converter.

where $R_{OB} = R_{Lmax} = V_O/I_{Omin}$. Hence, the minimum value of the magnetizing inductance L_m is

$$L_{m(min)} = \frac{n^2 R_{Lmax}(1 - D_{min})^2}{2f_s} = \frac{n^2 V_O(1 - D_{min})^2}{2f_s I_{Omin}}. \tag{5.49}$$

The load resistance R_{LB} at the CCM/DCM boundary is

$$R_{LB} = \frac{2f_s L_m}{n(1 - D)^2}, \tag{5.50}$$

and the load current at the boundary is

$$I_{OB} = \frac{nV_O(1 - D)^2}{2f_s L_m}. \tag{5.51}$$

Figures 5.6 and 5.7 show the normalized load current $I_{OB}/(nV_O/2f_sL_m) = (1 - D)^2$ and load resistance $R_{LB}/(2f_sL_m/n) = 1/(1 - D)^2$ at the CCM/DCM boundary as functions of D.

5.3.8 Ripple Voltage in Flyback Converter for CCM

The output part of the flyback converter is shown in Figure 5.8, where the filter capacitor is modeled by its capacitance C and its ESR denoted by r_C. Figure 5.9 displays current and voltage waveforms in the converter output circuit. The dc component of the diode current equals the dc load current I_O. The ac component of the diode current flows approximately through the filter capacitor C_f. The peak-to-peak value of the capacitor current may be written as

$$I_{Cpp} = I_{DM} \approx nI_I + I_O = \frac{I_O}{1 - D}, \tag{5.52}$$

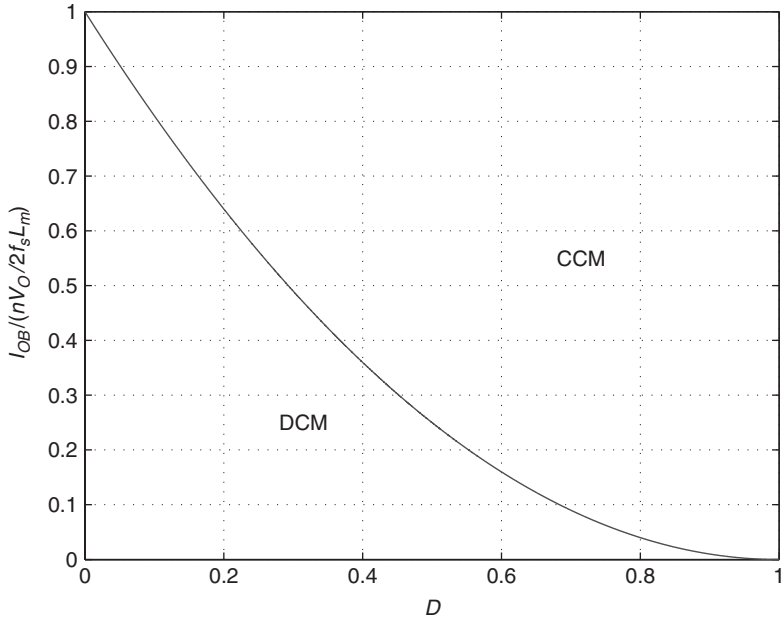


Figure 5.6 Normalized load current $I_{OB}/(nV_O/2f_sL_m)$ at the CCM/DCM boundary as a function of D for the flyback converter.

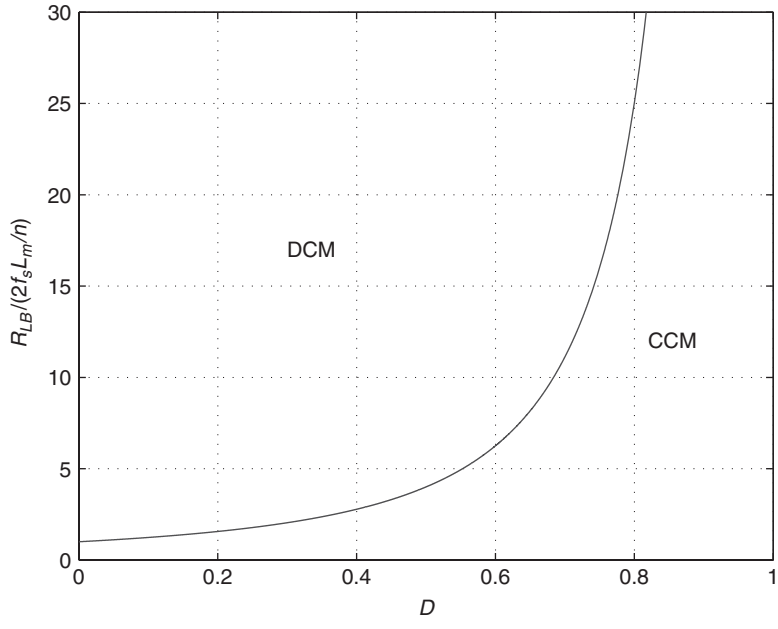


Figure 5.7 Normalized load resistance $R_{LB}/(2f_sL_m/n)$ at the CCM/DCM boundary as a function of D for the flyback converter.

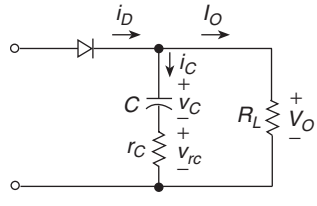


Figure 5.8 Output circuit of the flyback converter.

resulting in the peak-to-peak value of the voltage across r_C,

$$V_{rcpp} = r_C I_{Cpp} \approx \frac{r_C I_{Omax}}{1 - D_{max}}. \tag{5.53}$$

The peak-to-peak value of the output ripple voltage V_r is usually specified. Hence, the maximum peak-to-peak value of the ac component of the voltage across the capacitance C is found to be

$$V_{cpp} \approx V_r - V_{rcpp}. \tag{5.54}$$

On the other hand, this voltage is approximately given by

$$V_{cpp} = \frac{\Delta Q_{max}}{C_{min}} = \frac{I_{Omax} D_{max} T}{C_{min}} = \frac{V_O D_{max}}{f_s R_{Lmin} C_{min}}, \tag{5.55}$$

where ΔQ_{max} is the charge decrease during the time interval from zero to DT. Rearrangement of (5.55) gives

$$C_{min} = \frac{I_{Omax} D_{max}}{f_s V_{cpp}} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{cpp}}. \tag{5.56}$$

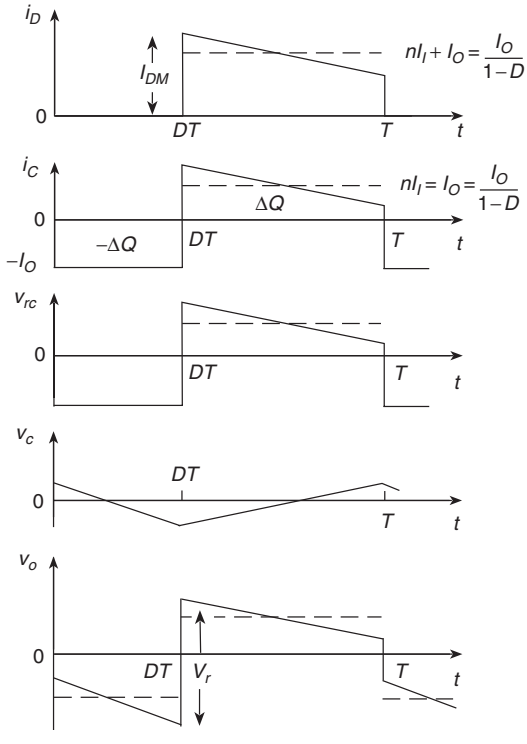


Figure 5.9 Waveforms illustrating the ripple voltage in the PWM flyback converter.

5.3.9 Power Losses and Efficiency of Flyback Converter for CCM

An equivalent circuit of the flyback converter with parasitic resistances is shown in Figure 5.10. In this figure, r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the magnetizing inductance L_m representing core losses, and r_C is the ESR of the filter capacitor C. The conduction losses will be found assuming that the magnetizing inductance current i_{Lm} is ripple-free. Hence, the switch current can be approximated by

$$i_S = \begin{cases} I_I + \dfrac{I_O}{n} = \dfrac{I_O}{n(1-D)}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{5.57}$$

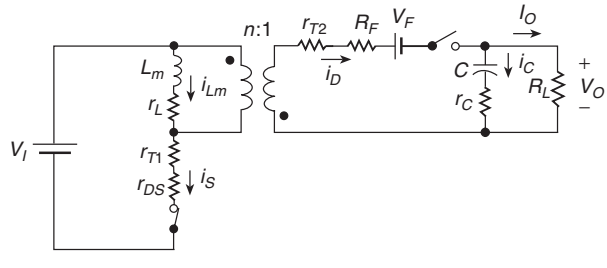


Figure 5.10 Equivalent circuit of the flyback converter with parasitic resistances and the diode offset voltage.

resulting in its rms value,

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \frac{I_O}{n(1-D)}\sqrt{\frac{1}{T}\int_0^{DT} dt} = \frac{I_O\sqrt{D}}{n(1-D)}, \tag{5.58}$$

resulting in turn in the conduction loss in the MOSFET and in the primary winding of the transformer,

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{r_{DS} D I_O^2}{n^2(1-D)^2} = \frac{D r_{DS} P_O}{(1-D)^2 n^2 R_L}, \tag{5.59}$$

and the primary winding of the transformer,

$$P_{rT1} = r_{T1} I_{Srms}^2 = \frac{r_{T1} D I_O^2}{n^2(1-D)^2} = \frac{D r_{T1} P_O}{(1-D)^2 n^2 R_L}. \tag{5.60}$$

Assuming that the transistor output capacitance C_o is linear, the switching loss is expressed as

$$P_{sw} = f_s C_o V_{SM}^2 = f_s C_o (V_I + nV_O)^2 = \frac{f_s C_o n^2 V_O^2}{D^2} = \frac{f_s C_o V_O^2 (1 + nM_{V\,DC})^2}{M_{V\,DC}^2}$$

$$= \frac{f_s C_o n^2 R_L P_O}{D^2} = \frac{f_s C_o R_L (1 + nM_{V\,DC})^2 P_O}{M_{V\,DC}^2}. \tag{5.61}$$

Hence, one obtains the total power dissipation in the MOSFET (excluding the drive power)

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \frac{D r_{DS} I_O^2}{n^2(1-D)^2} + \frac{1}{2} f_s C_o (V_I + nV_O)^2$$

$$= \left[\frac{D r_{DS}}{(1-D)^2 n^2 R_L} + \frac{f_s C_o n^2 R_L}{2D^2}\right] P_O$$

$$= \left[\frac{D r_{DS}}{(1-D)^2 n^2 R_L} + \frac{f_s C_o R_L (1 + nM_{V\ DC})^2}{2M_{V\ DC}^2}\right] P_O. \tag{5.62}$$

Similarly, the diode current may be approximated by

$$i_D = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ nI_I + I_O = \dfrac{I_O}{1-D}, & \text{for } DT < t \le T, \end{cases} \tag{5.63}$$

which yields its rms value,

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_{DT}^T dt} = \frac{I_O}{\sqrt{1-D}}, \tag{5.64}$$

leading to the power loss in the diode forward resistance R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F I_O^2}{1-D} = \frac{R_F P_O}{(1-D)R_L}, \tag{5.65}$$

and the resistance in the secondary winding of the transformer,

$$P_{rT2} = r_{T2} I_{Drms}^2 = \frac{r_{T2} I_O^2}{1-D} = \frac{r_{T2} P_O}{(1-D)R_L}. \tag{5.66}$$

The average value of the diode current is

$$I_D = \frac{1}{T}\int_0^T i_D\, dt = \frac{I_O}{(1-D)T}\int_{DT}^T dt = I_O, \tag{5.67}$$

which gives the power loss associated with the voltage V_F,

$$P_{VF} = V_F I_D = V_F I_O = \frac{V_F P_O}{V_O}. \tag{5.68}$$

Thus, the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = V_F I_O + \frac{R_F I_O^2}{1-D} = P_O \left[\frac{V_F}{V_O} + \frac{R_F}{(1-D)R_L} \right]. \tag{5.69}$$

The current through the magnetizing inductance is

$$i_{Lm} \approx I_I + \frac{I_O}{n} = \frac{I_O}{n(1-D)}, \tag{5.70}$$

leading to its rms value,

$$I_{Lm(rms)} \approx I_I + \frac{I_O}{n} = \frac{I_O}{n(1-D)}, \tag{5.71}$$

and the conduction loss in r_L,

$$P_{rL} = r_L I_{Lm(rms)}^2 = \frac{r_L I_O^2}{n^2(1-D)^2} = \frac{r_L P_O}{(1-D)^2 n^2 R_L}. \tag{5.72}$$

The current through the filter capacitor is

$$i_C = \begin{cases} -I_O, & \text{for } 0 < t \le DT, \\ nI_I = \dfrac{DI_O}{1-D}, & \text{for } DT < t \le T, \end{cases} \tag{5.73}$$

and the rms current through the filter capacitor is found to be

$$I_{Crms} = \sqrt{\frac{1}{T}\int_0^T i_C^2 dt} = I_O \sqrt{\frac{D}{1-D}} = I_L \sqrt{D(1-D)} = I_S \sqrt{\frac{1-D}{D}}, \tag{5.74}$$

and the power loss in the filter capacitor

$$P_{rC} = r_C I_{Crms}^2 = \frac{D r_C I_O^2}{1-D} = \frac{D r_C P_O}{(1-D)R_L}. \tag{5.75}$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{rT1} + P_{sw} + P_D + P_{rT2} + P_{rL} + P_{rC} \\ &= \frac{(r_{DS} + r_{T1})DI_O^2}{n^2(1-D)^2} + f_s C_o (V_I + nV_O)^2 + V_F I_O + \frac{(R_F + r_{T2})I_O^2}{1-D} \\ &\quad + \frac{r_L I_O^2}{n^2(1-D)^2} + \frac{D r_C I_O^2}{1-D} \\ &= \left[\frac{D(r_{DS} + r_{T1}) + r_L}{(1-D)^2 n^2 R_L} + \frac{R_F + r_{T2} + D r_C}{(1-D)R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L (1 + nM_{V\,DC})^2}{M_{V\,DC}^2} \right] P_O. \end{aligned} \tag{5.76}$$

Thus, the converter efficiency is

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} \\ &= \frac{1}{1 + \dfrac{D(r_{DS} + r_{T1}) + r_L}{(1-D)^2 n^2 R_L} + \dfrac{R_F + r_{T2} + D r_C}{(1-D)R_L} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o R_L (1 + nM_{V\,DC})^2}{M_{V\,DC}^2}}. \end{aligned} \tag{5.77}$$

5.3.10 DC Voltage Transfer Function of Lossy Converter for CCM

The dc component of the input current is

$$I_I = \frac{1}{T}\int_0^T i_S\,dt = \frac{1}{T}\int_0^{DT} \frac{I_O}{n(1-D)}dt = \frac{I_O D}{n(1-D)}. \tag{5.78}$$

Hence, one obtains the dc current transfer function of the flyback converter,

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n(1-D)}{D}. \tag{5.79}$$

This equation holds true for both lossless and lossy converter. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = \frac{n(1-D)M_{V\,DC}}{D}, \tag{5.80}$$

from which the voltage transfer function of the lossy flyback converter is

$$\begin{aligned} M_{V\,DC} &= \frac{\eta}{M_{I\,DC}} = \frac{\eta D}{n(1-D)} \\ &= \frac{D}{n(1-D)[1 + \dfrac{D(r_{DS}+r_{T1})+r_L}{n^2 R_L(1-D)^2} + \dfrac{R_F + r_{T2} + Dr_C}{R_L(1-D)} + \dfrac{V_F}{V_O} + \dfrac{f_s C_o n^2 R_L}{D^2}]}. \end{aligned} \tag{5.81}$$

Hence, the duty cycle for the lossy converter is given by

$$D = \frac{nM_{V\,DC}}{nM_{V\,DC} + \eta} = \frac{1}{1 + \dfrac{\eta}{nM_{V\,DC}}}. \tag{5.82}$$

Notice that the duty cycle D at a given dc voltage transfer function is greater for the lossy converter than for the lossless converter.

Substitution of (5.82) into (5.77) yields the efficiency of the flyback converter for CCM,

$$\eta = \frac{N_\eta}{D_\eta}, \tag{5.83}$$

where

$$\begin{aligned} N_\eta = 1 &- \frac{M_{V\,DC}(2r_L + r_{DS} + r_{T1})}{nR_L} - \frac{nM_{V\,DC}(R_F + r_{T2} + r_C)}{R_L} \\ &+ \left\{ \left[1 - \frac{M_{V\,DC}(2r_L + r_{DS} + r_{T1})}{nR_L} - \frac{nM_{V\,DC}(R_F + r_{T2} + r_C)}{R_L} \right]^2 \right. \\ &- \frac{4M_{V\,DC}^2(r_{DS} + r_{T1} + r_L)}{R_L}\left[1 + \frac{r_L}{n^2 R_L} + \frac{R_F + r_{T2}}{R_L} + \frac{V_F}{V_O} \right. \\ &\left. \left. + \frac{f_s C_o R_L (1 + nM_{V\,DC})^2}{M_{V\,DC}^2} \right] \right\}^{\frac{1}{2}} \end{aligned} \tag{5.84}$$

and

$$D_\eta = 2\left[1 + \frac{r_L}{n^2 R_L} + \frac{R_F + r_{T2}}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L (1 + nM_{V\,DC})^2}{M_{V\,DC}^2} \right]. \tag{5.85}$$

5.3.11 Design of Flyback Converter for CCM

Design a universal power supply that accepts a single-phase line voltage from 85 to 264 Vrms at frequencies 50, 60, and 400 Hz, $V_O = 5\,\text{V}$, $I_O = 1$ to 10 A, and $V_r/V_O \leq 1\,\%$.

Solution. The maximum and minimum output powers are

$$P_{Omax} = V_O I_{Omax} = 5 \times 10 = 50\,\text{W} \tag{5.86}$$

and

$$P_{Omin} = V_O I_{Omin} = 5 \times 1 = 5\,\text{W}. \tag{5.87}$$

The minimum and maximum load resistances are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{5}{10} = 0.5\,\Omega \tag{5.88}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{5}{1} = 5\,\Omega. \tag{5.89}$$

The minimum and maximum dc input voltages are

$$V_{Imin} = 85 \times \sqrt{2} = 120.21\,\text{V} \tag{5.90}$$

and

$$V_{Imax} = 264 \times \sqrt{2} = 373.35\,\text{V}. \tag{5.91}$$

Hence, the minimum and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{5}{373.35} = 0.01339 \tag{5.92}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{5}{120.21} = 0.04159. \tag{5.93}$$

Assume the converter efficiency $\eta = 80\,\%$ and $D_{max} = 0.36$. Hence, the transformer turns ratio is

$$n = \frac{\eta D_{max}}{(1 - D_{max})M_{V\,DCmax}} = \frac{0.8 \times 0.36}{(1 - 0.36) \times 0.04159} = 10.82. \tag{5.94}$$

Let $n = 11$.

The minimum and maximum duty cycle are

$$D_{min} = \frac{nM_{V\,DCmin}}{nM_{V\,DCmin} + \eta} = \frac{11 \times 0.01339}{11 \times 0.01339 + 0.8} = 0.1555 \tag{5.95}$$

and

$$D_{max} = \frac{nM_{V\,DCmax}}{nM_{V\,DCmax} + \eta} = \frac{11 \times 0.04159}{11 \times 0.04159 + 0.8} = 0.3638. \tag{5.96}$$

Assuming the switching frequency $f_s = 100\,\text{kHz}$, the minimum magnetizing inductance is

$$L_{m(min)} = \frac{n^2 R_{Lmax}(1 - D_{min})^2}{2f_s} = \frac{11^2 \times 5 \times (1 - 0.1555)^2}{2 \times 10^5} = 2.157\,\text{mH}. \tag{5.97}$$

Pick $L_m = 2.5\,\text{mH}$.

The peak-to-peak value of the ac component of the current through the magnetizing inductance is

$$\Delta i_{Lm(max)} = \frac{nV_O(1 - D_{min})}{f_s L_m} = \frac{11 \times 5 \times (1 - 0.1555)}{10^5 \times 2.5 \times 10^{-3}} = 0.1858\,\text{A}. \tag{5.98}$$

The maximum dc input current occurs at $V_{Imin} = 120.21\,\text{V}$, which corresponds to the maximum dc voltage transfer function $M_{V\,DCmax} = 0.04159$. This current is given by

$$I_{Imax} = M_{V\,DCmax} I_{Omax} = 0.04159 \times 10 = 0.4159\,\text{A}. \tag{5.99}$$

The current and voltage stresses of the semiconductor devices are

$$I_{SMmax} = I_{Imax} + \frac{I_{Omax}}{n} + \frac{\Delta i_{Lm(max)}}{2} = 0.4159 + \frac{10}{11} + \frac{0.1858}{2} = 1.418\,\text{A}, \tag{5.100}$$

$$I_{DMmax} = nI_{Imax} + I_{Omax} + \frac{n\,\Delta i_{Lm(max)}}{2} = 11 \times 0.4159 + 10 + \frac{11 \times 0.1858}{2} = 15.597\,\text{A}, \tag{5.101}$$

$$V_{SMmax} = V_{Imax} + nV_O = 373.35 + 11 \times 5 = 428.35\,\text{V}, \tag{5.102}$$

and

$$V_{DMmax} = \frac{V_{Imax}}{n} + V_O = \frac{373.35}{11} + 5 = 38.94\,\text{V}. \tag{5.103}$$

Let us select an International Rectifier IRF840 power MOSFET whose $V_{DSS} = 500\,\text{V}$, $I_{SM} = 8\,\text{A}$, $r_{DS} = 0.85\,\Omega$, $Q_g = 42\,\text{nC}$, and $C_o = 100\,\text{pF}$, and an MBR2540 Schottky barrier diode whose $I_{DM} = 25\,\text{A}$, $V_{DM} = 40\,\text{V}$, $V_F = 0.3\,\text{V}$, and $R_F = 10\,\text{m}\Omega$.

The ripple voltage is

$$V_r = 0.01V_O = 0.01 \times 5 = 50\,\text{mV}. \tag{5.104}$$

Let us assume $V_{rcpp} = 40\,\text{mV}$ and $V_{Cpp} = 10\,\text{mV}$. Hence, one obtains the maximum value of the ESR of the filter capacitor,

$$r_{Cmax} = \frac{V_{rcpp}}{I_{DMmax}} = \frac{40 \times 10^{-3}}{15.597} = 2.56\,\text{m}\Omega, \tag{5.105}$$

and the filter capacitance,

$$C_{min} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{Cpp}} = \frac{0.3638 \times 5}{10^5 \times 0.5 \times 0.01} = 3.638\,\text{mF}. \tag{5.106}$$

Pick $C = 4\,\text{mF}/25\,\text{V}/r_C = 2.5\,\text{m}\Omega$.

The power losses and the converter efficiency will be calculated at the maximum load current $I_{Omax} = 10\,\text{A}$ and the maximum input voltage $V_{Imax} = 373.35\,\text{V}$. The rms value of the current through the magnetizing inductance is

$$I_{Lm(rms)} \approx I_{Lm} = I_{Imax} + \frac{I_{Omax}}{n} = 0.4159 + \frac{10}{11} = 1.325\,\text{A}. \tag{5.107}$$

Assuming the dc value of $r_L = 350\,\text{m}\Omega$, one obtains

$$P_{rL} = r_L I_{Lm(rms)}^2 = 0.35 \times 1.325^2 = 0.6145\,\text{W}. \tag{5.108}$$

The switch rms current is

$$I_{Srms} = \frac{I_{Omax}\sqrt{D_{max}}}{n(1 - D_{max})} = \frac{10\sqrt{0.3638}}{11 \times (1 - 0.3638)} = 0.8619\,\text{A} \tag{5.109}$$

which gives the MOSFET conduction loss

$$P_{rDS} = r_{DS} I_{Srms}^2 = 0.85 \times 0.8619^2 = 0.6313\,\text{W}. \tag{5.110}$$

Assuming the resistance of the primary winding of the transformer $r_{T1} = 0.9\,\Omega$, the conduction loss in r_{T1} is

$$P_{rT1} = r_{T1} I_{Srms}^2 = 0.9 \times 0.8619^2 = 0.6684\,\text{W}. \tag{5.111}$$

The switching loss is

$$P_{sw} = \frac{f_s C_o n^2 V_O^2}{D_{min}^2} = \frac{10^5 \times 100 \times 10^{-12} \times 11^2 \times 5^2}{0.1555^2} = 1.251\,\text{W}. \tag{5.112}$$

Hence,

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 0.6313 + \frac{1.251}{2} = 0.6313 + 0.625 = 1.256\,\text{W}. \tag{5.113}$$

The rms diode current is

$$I_{Drms} = \frac{I_{Omax}}{\sqrt{1 - D_{max}}} = \frac{10}{\sqrt{1 - 0.3638}} = 12.537\,\text{A}. \tag{5.114}$$

Thus, the power loss due to R_F is

$$P_{RF} = R_F I_{Drms}^2 = 0.01 \times 12.537^2 = 1.572\,\text{W}, \tag{5.115}$$

and the power loss due to V_F is

$$P_{VF} = V_F I_{Omax} = 0.3 \times 10 = 3\,\text{W}, \tag{5.116}$$

resulting in the diode conduction loss

$$P_D = P_{VF} + P_{RF} = 3 + 1.572 = 4.572\,\text{W}. \tag{5.117}$$

Assuming the resistance of the secondary winding of the transformer $r_{T2} = 20\,\text{m}\Omega$, the power loss in r_{T2} is

$$P_{rT2} = r_{T2} I_{Drms}^2 = 0.02 \times 12.537^2 = 3.144\,\text{W}. \tag{5.118}$$

The rms current of the filter capacitor is

$$I_{Crms} = I_{Omax} \sqrt{\frac{D_{max}}{1 - D_{max}}} = 10 \sqrt{\frac{0.3638}{1 - 0.3638}} = 7.562\,\text{A}. \tag{5.119}$$

Hence, the power loss in the ESR of the filter capacitor is

$$P_{rC} = r_C I_{Crms}^2 = 0.0025 \times 7.562^2 = 0.143\,\text{W}. \tag{5.120}$$

The total power loss is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL} + P_{rT1} + P_{rT2} + P_{rC} \\ &= 0.6313 + 1.25 + 4.572 + 0.6145 + 0.6684 + 3.144 + 0.143 = 11.0231\,\text{W}. \end{aligned} \tag{5.121}$$

Hence, the converter efficiency at full power is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{50}{50 + 11.0231} = 81.9\,\%. \tag{5.122}$$

A rectangular positive gate-to-source voltage of magnitude $V_{GSm} = 8\,\text{V}$ is used to drive the MOSFET. Therefore, the gate-drive power is

$$P_G = f_s Q_g V_{GSm} = 10^5 \times 42 \times 10^{-9} \times 8 = 33.6\,\text{mW}. \tag{5.123}$$

Using (5.83)–(5.85), one can calculate the efficiency η as a function of the dc input voltage V_I at fixed load resistances R_L for the designed flyback converter in CCM; the plots are depicted in Figure 5.11. Knowing the efficiency η, the duty cycle D can be computed from (5.82); Figure 5.12 shows the duty cycle D as a function of dc input voltage V_I for the

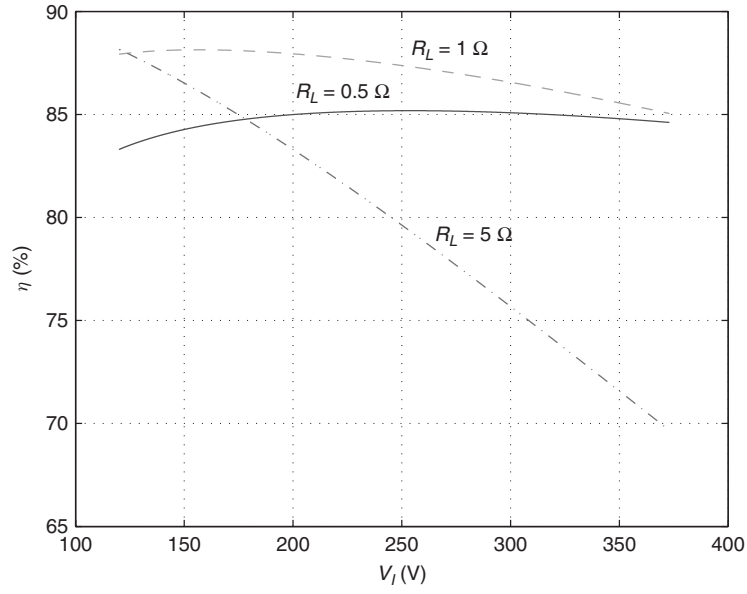


Figure 5.11 Efficiency η versus dc input voltage V_I at various load resistances R_L for the flyback converter in CCM.

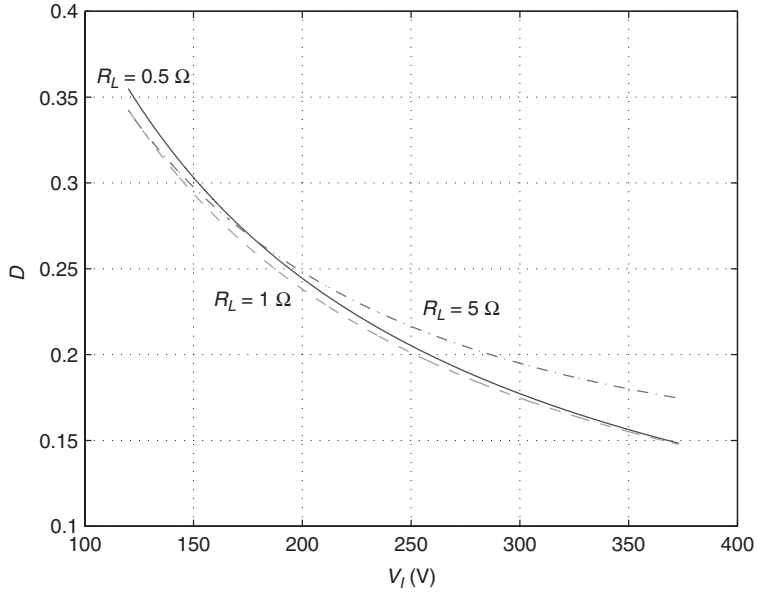


Figure 5.12 Duty cycle D versus dc input voltage V_I at fixed load resistances R_L for the flyback converter in CCM.

flyback converter designed for CCM. Figures 5.13 and 5.14 show the efficiency η and duty cycle D as functions of the dc output current I_O at fixed dc input voltages V_I, respectively. Plots of the efficiency η and the duty cycle D versus the load resistance R_L at fixed dc input voltages V_I are depicted in Figures 5.15 and 5.16. The duty cycle D decreases as V_I increases.

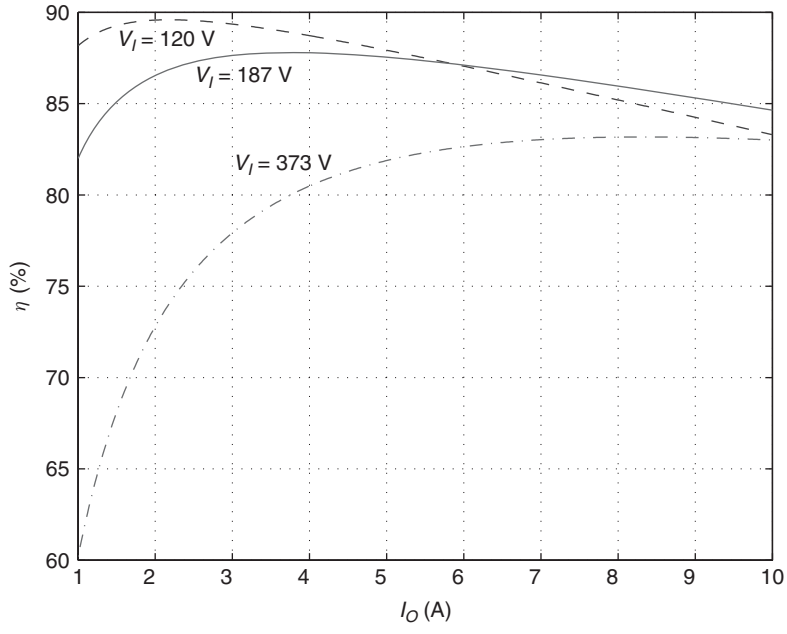


Figure 5.13 Efficiency η versus dc load current I_O at fixed values of dc input voltage V_I for the flyback converter in CCM.

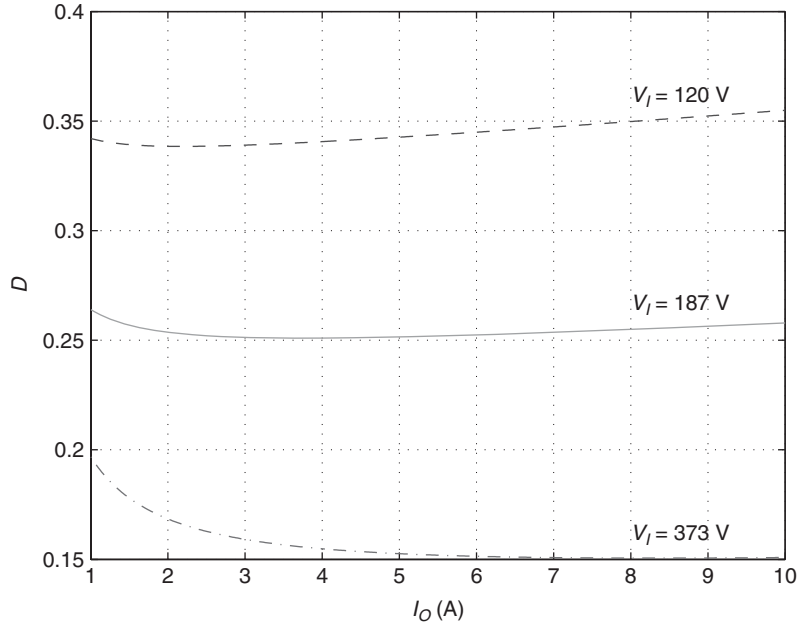


Figure 5.14 Duty cycle D versus dc load current I_O at fixed values of dc input voltage V_I for the flyback converter in CCM.

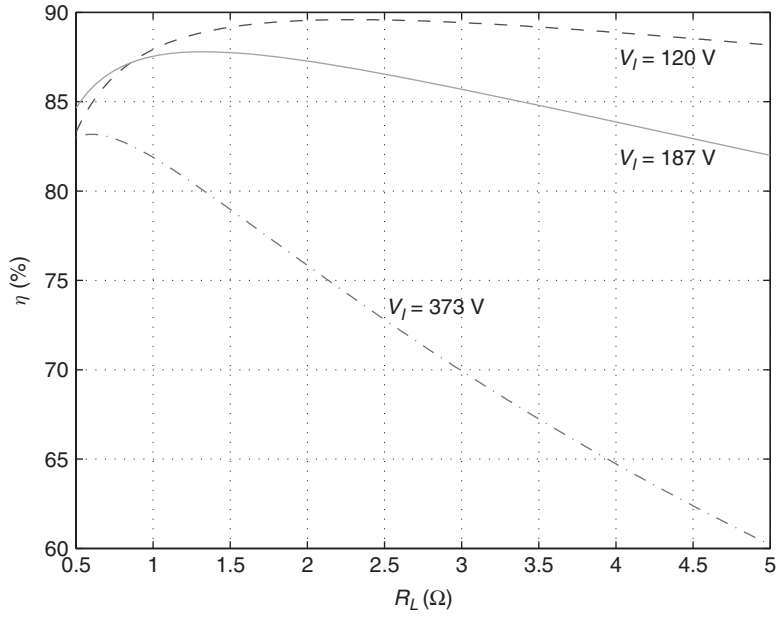


Figure 5.15 Efficiency η versus load resistance R_L at dc fixed values of input voltage V_I for the flyback converter in CCM.

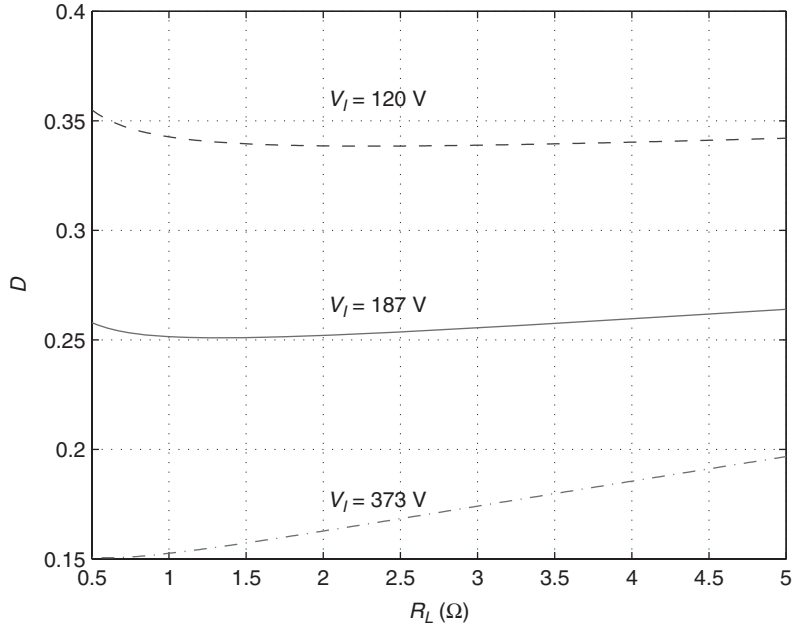


Figure 5.16 Duty cycle D versus load resistance R_L at dc fixed values of input voltage V_I for the flyback converter in CCM.

5.4 DC Analysis of PWM Flyback Converter for DCM

Equivalent circuits for the PWM flyback converter operating in the DCM are depicted in Figure 5.17. Idealized current and voltage waveforms are shown in Figure 5.18. Prior to time $t = 0$, the current through the magnetizing inductance L_m is zero. At time $t = 0$, the switch is turned on, causing the diode to turn off. The voltage across the magnetizing inductance is V_I, and the current through this inductance increases linearly from zero. At time $t = DT$, the switch is turned off and the diode turns on. The voltage across the magnetizing inductance is $-V_O$. Therefore, the current through the magnetizing inductance decreases linearly. This current is reflected to the secondary of the transformer and flows through the diode. Once the diode current reaches zero, the diode begins to turn off. The current through the magnetizing inductance is zero until the switch is turned on.

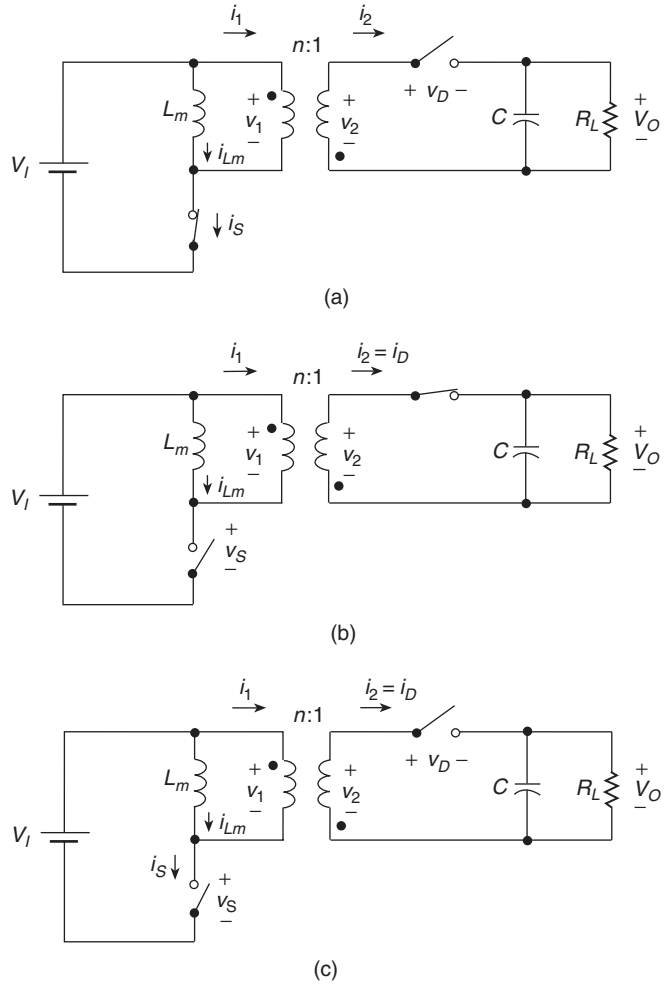


Figure 5.17 Equivalent circuits of the PWM flyback converter for DCM. (a) Equivalent circuit when the switch is ON and the diode is OFF. (b) Equivalent circuit when the switch is OFF and the diode is ON. (c) Equivalent circuit when both the switch and the diode are OFF.

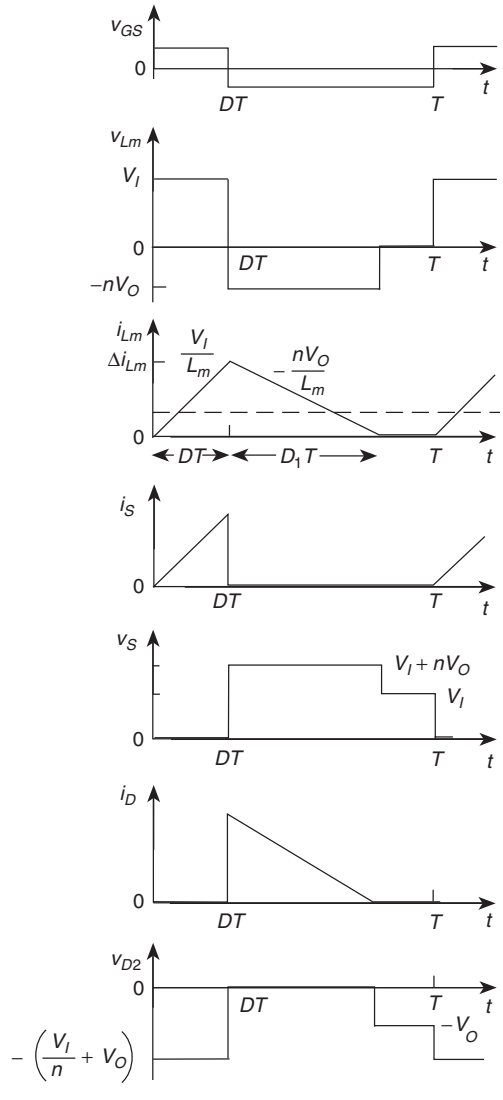


Figure 5.18 Idealized current and voltage waveforms in the PWM flyback converter for DCM.

5.4.1 Time Interval $0 < t \leq DT$

During this time interval, the switch is ON and the diode is OFF. The equivalent circuit is shown in Figure 5.17(a). The current through the diode and the secondary is $i_D = i_2 = 0$, resulting in the current $i_1 = -i_2/n = 0$ through the primary. The voltage across the primary and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = V_I = L_m \frac{di_{Lm}}{dt}, \qquad i_{Lm}(0) = 0, \tag{5.124}$$

and the magnetizing inductance and switch current is

$$i_S = i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt = \frac{1}{L_m}\int_0^t V_I\,dt = \frac{V_I}{L_m}t. \tag{5.125}$$

Hence, one obtains the peak value of the switch current and the magnetizing inductance current,

$$I_{SM} = i_{Lm(max)} = \Delta i_{Lm} = i_{Lm}(DT) = \frac{V_I DT}{L_m} = \frac{V_I D}{f_s L_m}. \tag{5.126}$$

The voltage across the secondary winding is

$$v_2 = -\frac{v_1}{n}, \tag{5.127}$$

resulting in the voltage across the diode

$$v_D = -\left(\frac{V_I}{n} + V_O\right), \tag{5.128}$$

from which

$$V_{DM(max)} = \frac{V_{Imax}}{n} + V_O. \tag{5.129}$$

This time interval ends when the switch is turned off by the driver.

5.4.2 Time Interval $DT < t \leq (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 5.17(b). The switch is OFF and the diode is ON. Hence, $i_S = 0$ and $v_D = 0$. Since

$$v_2 = V_O, \tag{5.130}$$

the voltage across the magnetizing inductance L_m and the primary of the transformer is

$$v_1 = v_{Lm} = -nv_2 = -nV_O = L_m \frac{di_{Lm}}{dt}. \tag{5.131}$$

From (5.126), the current through the magnetizing inductance is

$$\begin{aligned} i_{Lm} &= \frac{1}{L_m}\int_{DT}^{t} v_{Lm}\,dt + i_{Lm}(DT) = \frac{1}{L_m}\int_{DT}^{t} (-nV_O)dt + i_{Lm}(DT) \\ &= -\frac{nV_O}{L_m}(t - DT) + i_{Lm}(DT) = -\frac{nV_O}{L_m}(t - DT) + \frac{V_I DT}{L_m}. \end{aligned} \tag{5.132}$$

Hence, the peak value of this current is

$$\Delta i_{Lm} = \frac{1}{L_m}\int_{(D+D_1)T}^{DT} v_{Lm}dt = \frac{1}{L_m}\int_{(D+D_1)T}^{DT} (-nV_O)dt = \frac{nV_O D_1}{f_s L_m}. \tag{5.133}$$

Using (5.132), one arrives at the current through the primary of the transformer,

$$i_1 = -i_{Lm} = \frac{nV_O}{L_m}(t - DT) - \frac{V_I D}{f_s L_m}, \tag{5.134}$$

and the current through the diode and the secondary of the transformer,

$$i_D = i_2 = -ni_1 = -\frac{n^2 V_O}{L_m}(t - DT) + \frac{nV_I D}{f_s L_m}. \tag{5.135}$$

Thus, from (5.126), the peak value of the diode current is

$$I_{DM} = nI_{SM} = \frac{nV_I D}{f_s L_m}. \tag{5.136}$$

Because

$$v_1 = -nv_2 = -nV_O, \tag{5.137}$$

the peak voltage across the switch is

$$v_S = V_{SM} = V_I - v_1 = V_I + nV_O, \tag{5.138}$$

which leads to

$$V_{SMmax} = V_{Imax} + nV_O. \tag{5.139}$$

This time interval ends when the diode current reaches zero.

5.4.3 Time Interval $(D + D_1)T < t \leq T$

During this time interval, both the switch and the diode are OFF. The equivalent circuit is shown in Figure 5.17(c). For this circuit,

$$i_D = i_2 = 0, \tag{5.140}$$

resulting in

$$i_1 = 0. \tag{5.141}$$

Also

$$i_S = 0. \tag{5.142}$$

Because of (5.141) and (5.142),

$$i_{Lm} = 0. \tag{5.143}$$

Hence,

$$v_1 = v_{Lm} = L_m \frac{di_{Lm}}{dt} = 0, \tag{5.144}$$

resulting in

$$v_2 = 0. \tag{5.145}$$

The voltage across the switch is

$$v_S = V_I, \tag{5.146}$$

and the voltage across the diode is

$$v_D = -V_O. \tag{5.147}$$

This time interval ends when the switch is turned on by the driver.

5.4.4 DC Voltage Transfer Function for DCM

Method I. Referring to Figure 5.18 and using the volt-second balance for v_{Lm},

$$V_I DT = nV_O D_1 T, \tag{5.148}$$

which leads to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{nD_1}. \tag{5.149}$$

Using (5.126), the dc output current is found to be

$$I_O = \frac{1}{T}\int_0^T i_D\, dt = \frac{1}{T}\int_{DT}^{(D+D_1)T} i_D\, dt = \frac{D_1 n\, \Delta i_{Lm}}{2} = \frac{nDD_1 V_I}{2f_s L_m} = \frac{V_O}{R_L}, \tag{5.150}$$

resulting in

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{nDD_1 R_L}{2f_s L_m}. \tag{5.151}$$

Equating the right-hand sides of (5.149) and (5.151) gives

$$D_1 = \sqrt{\frac{2f_sL_m}{n^2R_L}} = \sqrt{\frac{2f_sL_mI_O}{n^2V_O}}, \tag{5.152}$$

and substitution of this into (5.149) yields

$$M_{V\,DC} = D\sqrt{\frac{V_O}{2f_sL_mI_O}} = D\sqrt{\frac{R_L}{2f_sL_m}}. \tag{5.153}$$

Hence,

$$\begin{aligned} D &= M_{V\,DC}\sqrt{\frac{2f_sL_mI_O}{V_O}} \\ &= M_{V\,DC}\sqrt{\frac{2f_sL_m}{R_L}}, \quad \text{for} \quad D < 1 - \sqrt{\frac{2f_sL_mI_O}{n^2V_O}} = 1 - \sqrt{\frac{2f_sL_m}{n^2R_L}}. \end{aligned} \tag{5.154}$$

Since the magnetizing inductance reflected to the transformer secondary is given by

$$L_{ms} = \frac{L_m}{n^2}, \tag{5.155}$$

one obtains

$$M_{V\,DC} = \frac{D}{n}\sqrt{\frac{V_O}{2f_sL_{ms}I_O}} = \frac{D}{n}\sqrt{\frac{R_L}{2f_sL_{ms}}} \tag{5.156}$$

and

$$\begin{aligned} D &= nM_{V\,DC}\sqrt{\frac{2f_sL_{ms}}{R_L}} \\ &= nM_{V\,DC}\sqrt{\frac{2f_sL_{ms}I_O}{V_O}}, \quad \text{for} \quad D < 1 - \sqrt{\frac{2f_sL_{ms}I_O}{V_O}} = 1 - \sqrt{\frac{2f_sL_{ms}}{R_L}}. \end{aligned} \tag{5.157}$$

At the CCM/DCM boundary,

$$M_{V\,DCB} = \frac{D_B}{n(1-D_B)} = \frac{D_B}{n}\sqrt{\frac{R_L}{2f_sL_{ms}}}. \tag{5.158}$$

Hence, one obtains the duty cycle at the boundary

$$D_B = 1 - \sqrt{\frac{2f_sL_mI_O}{n^2V_O}} = 1 - \sqrt{\frac{2f_sL_m}{n^2R_L}} = 1 - \sqrt{\frac{2f_sL_{ms}I_O}{V_O}} = 1 - \sqrt{\frac{2f_sL_{ms}}{R_L}}. \tag{5.159}$$

Using (5.154) and (5.159), the dc voltage transfer function at the boundary is obtained as

$$nM_{V\,DCB} = \sqrt{\frac{n^2V_O}{2f_sL_mI_O}} - 1 = \sqrt{\frac{n^2R_L}{2f_sL_m}} - 1 = \sqrt{\frac{V_O}{2f_sL_{ms}I_O}} - 1 = \sqrt{\frac{R_L}{2f_sL_{ms}}} - 1. \tag{5.160}$$

Figures 5.19 and 5.20 respectively depict plots of D versus $I_O/(V_O/2f_sL_{ms})$ and $R_L/(2f_sL_{ms})$ at various values of $nM_{V\,DC}$ for both CCM and DCM. Plots of $nM_{V\,DC}$ versus $I_O/(V_O/2f_sL_{ms})$ and $R_L/(2f_sL_{ms})$ at various values of D are shown in Figures 5.21 and 5.22.

Method II. The dc component of the input current equals the dc component of the switch current,

$$I_I = I_S = \frac{1}{T}\int_0^{DT} i_S\,dt = \frac{1}{T}\int_0^{DT}\left(\frac{V_I}{L_m}\right)tdt = \frac{D^2V_I}{2f_sL_m}. \tag{5.161}$$

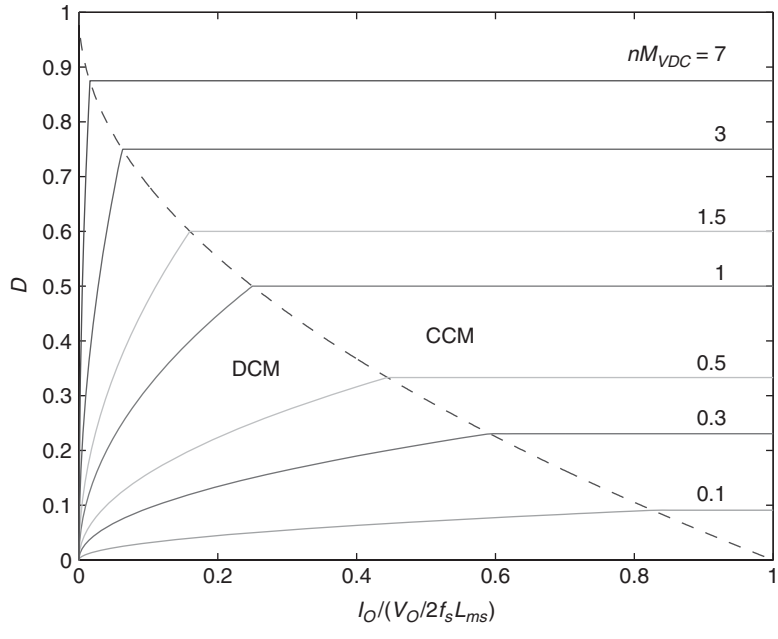


Figure 5.19 Duty cycle D as a function of normalized load current $I_O/(V_O/2f_sL_{ms})$ at fixed values of $M_{V\,DC}$ for the lossless flyback converter in CCM and DCM.

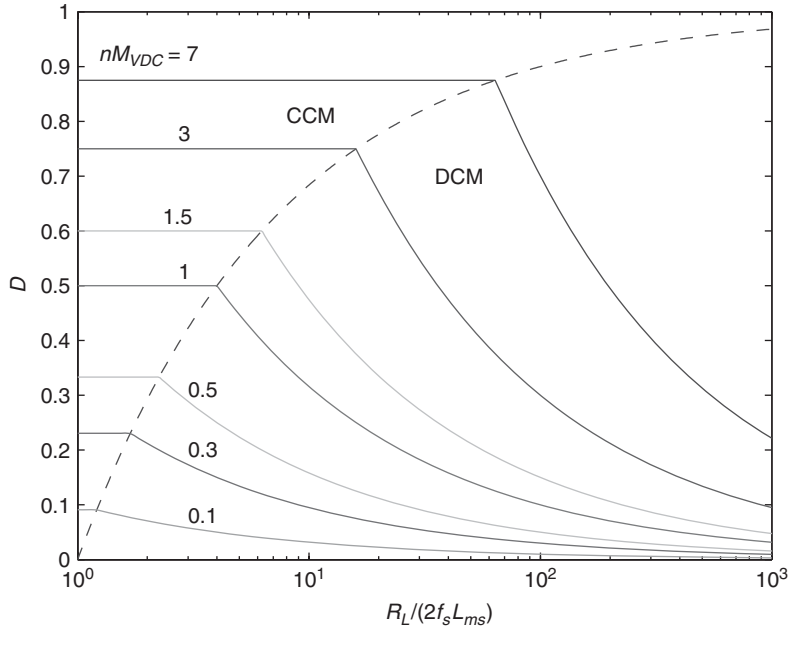


Figure 5.20 Duty cycle D as a function of load resistance $R_L/(2f_sL_{ms})$ at fixed values of $M_{V\,DC}$ for the lossless flyback converter in CCM and DCM.

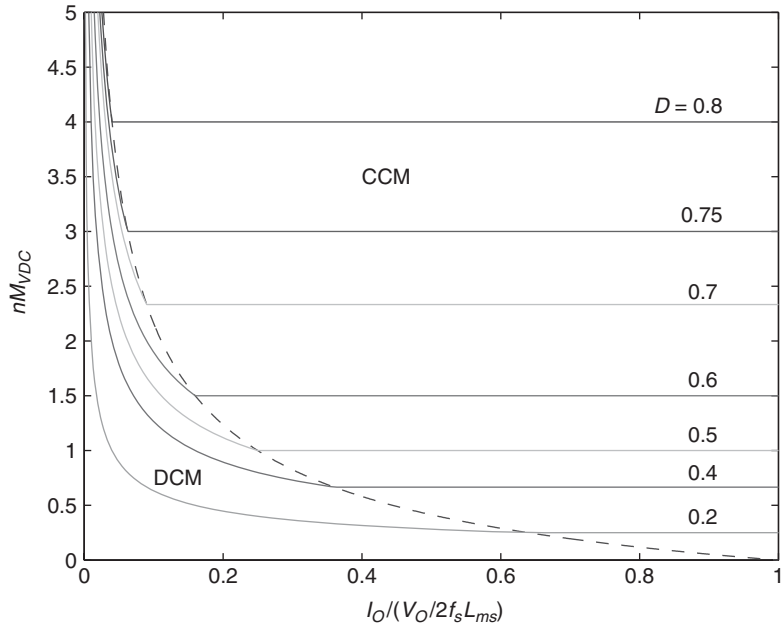


Figure 5.21 DC voltage transfer function $M_{V\,DC}$ as a function of normalized load current $I_O/(V_O/2f_sL_{ms})$ at fixed values of D for the lossless flyback converter.

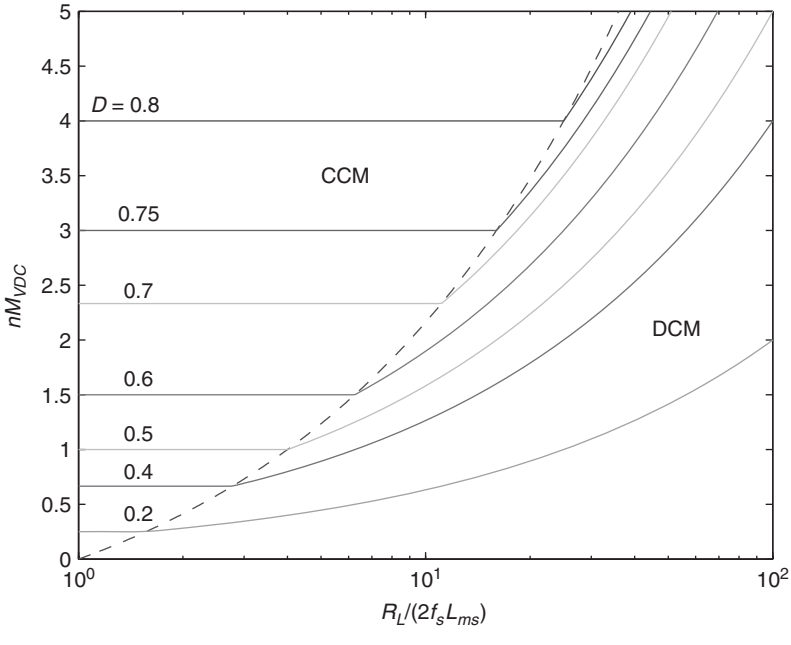


Figure 5.22 DC voltage transfer function $M_{V\,DC}$ as a function of normalized load resistance $R_L/(2f_sL_{ms})$ at fixed values of D for the lossless flyback converter.

Therefore, the dc input power is

$$P_I = V_I I_I = \frac{D^2 V_I^2}{2 f_s L_m}. \tag{5.162}$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{5.163}$$

Equating the right-hand sides of (5.162) and (5.163), one obtains (5.153).

5.4.5 Maximum Magnetizing Inductance for DCM

The minimum value of the magnetizing inductance peak current at the CCM/DCM boundary occurs at $D = D_{Bmax}$. From (5.43),

$$\Delta i_{Lm(min)} = \frac{n V_O (1 - D_{Bmax})}{f_s L_{m(max)}}. \tag{5.164}$$

The dc current through the magnetizing inductance at the CCM/DCM boundary is

$$I_{LmB} = \frac{\Delta i_{Lm(min)}}{2} = \frac{n V_O (1 - D_{Bmax})}{2 f_s L_{m(max)}}. \tag{5.165}$$

The energy transferred from the input dc voltage source V_I to the magnetizing inductance during one cycle for the boundary case is

$$W_{OB} = \frac{L_{m(max)} \Delta i_{Lm(min)}^2}{2}, \tag{5.166}$$

which results in dc output power at the boundary given by

$$\begin{aligned} P_{OB} &= \frac{W_{OB}}{T} = f_s W_{OB} = \frac{f_s L_{m(max)} \Delta i_{Lm(min)}^2}{2} \\ &= \frac{f_s L_{m(max)} n^2 V_O^2 (1 - D_{Bmax})^2}{2 f_s^2 L_{m(max)}^2} = \frac{n^2 V_O^2 (1 - D_{Bmax})^2}{2 f_s L_{m(max)}}. \end{aligned} \tag{5.167}$$

The dc power transferred from the converter to the load at the boundary can be expressed as

$$P_{OB} = \frac{V_O^2}{R_{Lmin}}. \tag{5.168}$$

Hence, the maximum value of the magnetizing inductance L_m is

$$L_{m(max)} = \frac{n^2 R_{Lmin} (1 - D_{Bmax})^2}{2 f_s} = \frac{n^2 V_O (1 - D_{Bmax})^2}{2 f_s I_{OB}}. \tag{5.169}$$

5.4.6 Ripple Voltage in Flyback Converter for DCM

The peak-to-peak value of the capacitor current is

$$I_{Cpp} = I_{DM} = \frac{n D V_I}{f_s L_m} = \frac{n V_O D_1}{f_s L_m}, \tag{5.170}$$

resulting in the peak-to-peak value of the voltage across r_C,

$$V_{rcpp} = r_C I_{DM} = \frac{r_C n D V_I}{f_s L_m} = \frac{r_C n V_O D_1}{f_s L_m}. \tag{5.171}$$

The voltage drop across the capacitor is

$$V_{cpp} \approx V_r - V_{rcpp}. \tag{5.172}$$

The voltage across the capacitance is

$$V_{cpp} = \frac{\Delta Q_{max}}{C_{min}} = \frac{I_{Omax} D_{max} T}{C_{min}} = \frac{V_O D_{max}}{f_s R_{Lmin} C_{min}}, \tag{5.173}$$

where ΔQ_{max} is the charge decrease during the time interval from zero to DT. Rearrangement of (5.55) gives

$$C_{min} = \frac{I_{Omax} D_{max}}{f_s V_{cpp}} = \frac{D_{max} V_O}{f_s R_{Lmin} V_{cpp}}. \tag{5.174}$$

5.4.7 Power Losses and Efficiency of Flyback Converter for DCM

The peak current through the magnetizing inductance and the switch is

$$\Delta i_{Lm} = I_{SM} = \frac{DV_I}{f_s L_m} = \frac{DV_O}{f_s L_m M_{V\,DC}} = V_O \sqrt{\frac{2}{f_s L_m R_L}}. \tag{5.175}$$

The rms value of the switch current is

$$I_{Srms} = \sqrt{\frac{1}{T} \int_0^{DT} i_S^2 \, dt} = \Delta i_{Lm} \sqrt{\frac{D}{3}} = V_O \sqrt{\frac{2D}{3 f_s L_m R_L}}. \tag{5.176}$$

Therefore, the MOSFET conduction loss is

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} \Delta i_{Lm}^2}{3} = \frac{2 r_{DS} D V_O^2}{3 f_s L_m R_L} = \frac{2 D r_{DS}}{3 f_s L_m} P_O, \tag{5.177}$$

and the conduction loss in the primary winding resistance r_{T1} is

$$P_{rT1} = r_{T1} I_{Srms}^2 = \frac{D r_{T1} \Delta i_{Lm}^2}{3} = \frac{2 r_{T1} D V_O^2}{3 f_s L_m R_L} = \frac{2 D r_{T1}}{3 f_s L_m} P_O. \tag{5.178}$$

The maximum conduction loss in r_{DS} and r_{T1} occurs at a full-load resistance R_{Lmin} and a low input voltage V_{Imin}. At low input voltage V_{Imin}, the duty cycle takes on a maximum value D_{max}. At a full-load resistance R_{Lmin}, a large current is drawn from the line. Both these effects result in a maximum value of the switch rms current I_{Srms}.

The switching loss is given by

$$\begin{aligned} P_{sw} &= f_s C_o V_{SM}^2 = f_s C_o (V_I + n V_O)^2 = n^2 f_s C_o V_O^2 \left(\frac{1}{n M_{V\,DC}} + 1 \right)^2 \\ &= n^2 f_s C_o R_L \left(\frac{1}{n M_{V\,DC}} + 1 \right)^2 P_O = n^2 f_s C_o R_L \left(\sqrt{\frac{2 f_s L_m}{n^2 D^2 R_L}} + 1 \right)^2 P_O. \end{aligned} \tag{5.179}$$

The maximum switching loss occurs at the maximum switch voltage $V_{SMmax} = V_{Imax} + nV_O$ and is independent of the load.

The peak diode current is

$$I_{DM} = n \Delta i_{Lm} = n V_O \sqrt{\frac{2}{f_s L_m R_L}}, \tag{5.180}$$

and the rms value of the diode current is

$$I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} i_D^2\, dt} = n\Delta i_{Lm}\sqrt{\frac{D_1}{3}} = V_O\left(\frac{8n^2}{9f_sL_mR_L^3}\right)^{0.25}. \tag{5.181}$$

Hence, the power loss in the diode due to R_F is

$$P_{RF} = R_F I_{Drms}^2 = \frac{D_1 R_F I_{DM}^2}{3} = \frac{D_1 R_F n^2 \Delta i_{Lm}^2}{3} = \frac{2nR_F V_O^2}{3R_L}\sqrt{\frac{2}{f_sL_mR_L}}$$

$$= \frac{2nR_F}{3}\sqrt{\frac{2}{f_sL_mR_L}}P_O, \tag{5.182}$$

and the conduction loss in the secondary winding resistance r_{T2} is

$$P_{rT2} = r_{T2} I_{Drms}^2 = \frac{D_1 r_{T2} I_{DM}^2}{3} = \frac{D_1 r_{T2} n^2 \Delta i_{Lm}^2}{3} = \frac{2nr_{T2}V_O^2}{3R_L}\sqrt{\frac{2}{f_sL_mR_L}}$$

$$= \frac{2nr_{T2}}{3}\sqrt{\frac{2}{f_sL_mR_L}}P_O. \tag{5.183}$$

The average diode current is $I_D = I_O$, resulting in the diode loss associated with V_F given by

$$P_{VF} = V_F I_D = V_F I_O = \frac{V_F}{V_O}P_O. \tag{5.184}$$

Thus the overall diode conduction loss is

$$P_D = P_{VF} + P_{RF} = \left(\frac{V_F}{V_O} + \frac{2nR_F}{3}\sqrt{\frac{2}{f_sL_mR_L}}\right)P_O. \tag{5.185}$$

Using (5.152), (5.154), and (5.175), the rms value of the current through the magnetizing inductance is

$$I_{Lm(rms)} = \sqrt{\frac{1}{T}\int_0^{(D+D_1)T} i_{Lm}^2 dt} = \Delta i_{Lm}\sqrt{\frac{D+D_1}{3}} = V_O\sqrt{\frac{2D}{3f_sL_mR_L}\left(1+\sqrt{\frac{2f_sL_m}{n^2D^2R_L}}\right)}. \tag{5.186}$$

The power loss in r_L is therefore given by

$$P_{rL} = r_L I_{Lm(rms)}^2 = \frac{r_L \Delta i_{Lm}^2 (D+D_1)}{3}$$

$$= \frac{2r_L D V_O^2}{3f_sL_mR_L}\left(1+\sqrt{\frac{2f_sL_m}{n^2D^2R_L}}\right) = \frac{2r_L D}{3f_sL_m}\left(1+\sqrt{\frac{2f_sL_m}{n^2D^2R_L}}\right)P_O. \tag{5.187}$$

The total power loss in the converter is

$$P_{LS} = P_{rDS} + P_{sw} + P_{rT1} + P_D + P_{rT2} + P_{rL}$$

$$= \left[\frac{2D(r_{DS}+r_{T1})}{3f_sL} + \frac{2n(R_F+r_{T2})}{3}\sqrt{\frac{2}{f_sL_mR_L}} + \frac{2Dr_L}{3f_sL_m}\left(1+\sqrt{\frac{2f_sL_m}{n^2D^2R_L}}\right)\right.$$

$$\left. + \frac{V_F}{V_O} + n^2 f_s C_o R_L\left(\sqrt{\frac{2f_sL_m}{n^2D^2R_L}}+1\right)^2\right]P_O. \tag{5.188}$$

This leads to the converter efficiency

$$\eta \equiv \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \frac{P_{LS}}{P_O}}$$

$$= \left[1 + \frac{2D(r_{DS} + r_{T1})}{3f_s L_m} + \frac{2n(R_F + r_{T2})}{3} \sqrt{\frac{2}{f_s L_m R_L}} + \frac{2Dr_L}{3f_s L_m} \left(\sqrt{\frac{2f_s L_m}{n^2 D^2 R_L}} + 1 \right) \right.$$

$$\left. + \frac{V_F}{V_O} + n^2 f_s C_o R_L \left(\sqrt{\frac{2f_s L_m}{n^2 D^2 R_L}} + 1 \right)^2 \right]^{-1}$$

$$= \left[1 + \frac{2M_{V\,DC}(r_{DS} + r_{T1})}{3} \sqrt{\frac{2}{f_s L_m R_L}} + \frac{2n(R_F + r_{T2})}{3} \sqrt{\frac{2}{f_s L_m R_L}} \right.$$

$$\left. + \frac{2r_L M_{V\,DC}}{3} \sqrt{\frac{2}{f_s L_m R_L}} \left(\frac{1}{nM_{V\,DC}} + 1 \right) + \frac{V_F}{V_O} + n^2 f_s C_o R_L \left(\frac{1}{nM_{V\,DC}} + 1 \right)^2 \right]^{-1}. \tag{5.189}$$

The dc input current is given by

$$I_I = \frac{1}{T} \int_0^{DT} i_{Lm} dt = \frac{1}{T} \int_0^{DT} \frac{V_I t}{L_m} dt = \frac{V_I D^2}{2f_s L_m}, \tag{5.190}$$

leading to the dc input power

$$P_I = V_I I_I = \frac{V_I^2 D^2}{2f_s L_m}. \tag{5.191}$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{5.192}$$

Since

$$P_O = \eta P_I, \tag{5.193}$$

the dc voltage transfer function of the lossy flyback converter is

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \sqrt{\eta} M_{V\ DC(lossless)} = D \sqrt{\frac{\eta R_L}{2f_s L_m}}$$

$$= D \sqrt{\frac{R_L}{2f_s L_m}} \left[1 + \frac{2D(r_{DS} + r_{T1})}{3f_s L_m} + \frac{2n(R_F + r_{T2})}{3} \sqrt{\frac{2}{f_s L_m R_L}} \right.$$

$$\left. + \frac{2Dr_L}{3f_s L_m} \left(\sqrt{\frac{2f_s L_m}{n^2 D^2 R_L}} + 1 \right) + \frac{V_F}{V_O} + n^2 f_s C_o R_L \left(\sqrt{\frac{2f_s L_m}{n^2 D^2 R_L}} + 1 \right)^2 \right]^{-\frac{1}{2}}. \tag{5.194}$$

Hence,

$$D = M_{V\,DC} \sqrt{\frac{2f_s L_m}{\eta R_L}} = M_{V\,DC} \sqrt{\frac{2f_s L_m I_O}{\eta V_O}}. \tag{5.195}$$

5.4.8 Design of Flyback Converter for DCM

Design a universal dc–dc converter for laptop computers that accepts a rectified single-phase voltage from 85 to 264 Vrms, $V_O = 15\,\text{V}$, $I_O = 0$ to 2 A, and $V_r/V_O \leq 1\,\%$.

Solution. The maximum output power is

$$P_{Omax} = V_O I_{Omax} = 15 \times 2 = 30\,\text{W}, \tag{5.196}$$

and the minimum output power is zero. The minimum load resistance is

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{15}{2} = 7.5\,\Omega, \tag{5.197}$$

and the maximum load resistance is infinity. The minimum and maximum values of the dc input voltage are

$$V_{Imin} = \sqrt{2}V_{rms(min)} = \sqrt{2} \times 85 = 120.21\,\text{V} \tag{5.198}$$

and

$$V_{Imax} = \sqrt{2}V_{rms(max)} = \sqrt{2} \times 264 = 373.35\,\text{V}. \tag{5.199}$$

Thus, the minimum and maximum dc voltage transfer functions are

$$M_{V\ DC(min)} = \frac{V_O}{V_{Imax}} = \frac{15}{373.35} = 0.0402 \tag{5.200}$$

and

$$M_{V\ DC(max)} = \frac{V_O}{V_{Imin}} = \frac{15}{120.21} = 0.125. \tag{5.201}$$

Assume that the duty cycle at the CCM/DCM boundary is $D_{Bmax} = 0.4$ and the converter efficiency is $\eta = 0.85$. Hence, one obtains the transformer turns ratio

$$n = \frac{\eta D_{Bmax}}{(1 - D_{Bmax})M_{V\,DCmax}} = \frac{0.85 \times 0.4}{(1 - 0.4) \times 0.125} = 4.533. \tag{5.202}$$

Pick $n = 5$. Assume that the switching frequency is $f_s = 100\,\text{kHz}$. From (5.169), the maximum magnetizing inductance required to maintain the converter in DCM is found to be

$$L_{m(max)} = \frac{n^2 R_{Lmin}(1 - D_{Bmax})^2}{2f_s} = \frac{5^2 \times 7.5 \times (1 - 0.4)^2}{2 \times 10^5} = 337.5\,\mu\text{H}. \tag{5.203}$$

Pick $L_m = 300\,\mu\text{H}$.

From (5.194), the minimum duty cycle occurs at V_{Imax},

$$D_{min} = M_{V\ DC(min)}\sqrt{\frac{2f_s L_m}{\eta R_{Lmin}}} = 0.0402\sqrt{\frac{2 \times 10^5 \times 300 \times 10^{-6}}{0.85 \times 7.5}} = 0.123, \tag{5.204}$$

and the maximum duty cycle occurs at V_{Imin},

$$D_{max} = M_{V\ DC(max)}\sqrt{\frac{2f_s L_m}{\eta R_{Lmin}}} = 0.125\sqrt{\frac{2 \times 10^5 \times 300 \times 10^{-6}}{0.85 \times 7.5}} = 0.383. \tag{5.205}$$

From (5.126) and (5.136), one obtains the maximum peak switch current,

$$I_{SMmax} = \Delta i_{Lm(max)} = \frac{D_{min} V_{Imax}}{f_s L_m} = \frac{0.123 \times 373.35}{10^5 \times 300 \times 10^{-6}} = 1.531\,\text{A}, \tag{5.206}$$

and the maximum peak diode current,

$$I_{DMmax} = n\,\Delta i_{Lm(max)} = 5 \times 1.531 = 7.655\,\text{A}. \tag{5.207}$$

Using (5.129) and (5.139), one can find the maximum value of the diode voltage,

$$V_{DMmax} = \frac{V_{Imax}}{n} + V_O = \frac{373.35}{5} + 15 = 89.67\,\text{V}, \tag{5.208}$$

and the maximum value of the switch voltage,

$$V_{SMmax} = V_{Imax} + nV_O = 373.35 + 5 \times 15 = 448.35\,\text{V}. \tag{5.209}$$

The maximum ripple voltage is

$$V_r = \frac{15}{100} = 150\,\text{mV}. \tag{5.210}$$

Assuming that the ESR of the filter capacitor is $r_C = 10\,\text{m}\Omega$, the voltage drop across r_C is found to be

$$V_{rcpp} = r_C I_{DM(max)} = 10 \times 10^{-3} \times 7.655 = 76.55\,\text{mV}. \tag{5.211}$$

Hence, the maximum voltage across the filter capacitance is

$$V_{cpp} = V_r - V_{rcpp} = 150 - 76.55 = 73.45\,\text{mV}. \tag{5.212}$$

Therefore, the minimum filter capacitance is

$$C_{min} = \frac{D_{max}V_O}{f_s R_{Lmin} V_{cpp}} = \frac{0.383 \times 15}{10^5 \times 7.5 \times 0.07345} = 104.28\,\mu\text{F}. \tag{5.213}$$

Let $C = 120\,\mu\text{F}/25\,\text{V}/10\,\text{m}\Omega$.

Choose an International Rectifier IRF840 power MOSFET with $r_{DS} = 0.85\,\Omega$, $V_{DSS} = V_{SM} = 500\,\text{V}$, $I_{SM} = 8\,\text{A}$, $Q_g = 42\,\text{nC}$, and $C_o = 100\,\text{pF}$. Also, select an MBR10100 Schottky diode with $V_{DM} = 100\,\text{V}$, $I_{DM} = I_{F(AV)} = 10\,\text{A}$, $V_F = 0.35\,\text{V}$ at 25°C, $V_F = 0.24\,\text{V}$ at 100°C, and $R_F = 30\,\text{m}\Omega$.

The maximum conduction loss in the MOSFET occurs at full load $R_{Lmin} = 7.5\,\Omega$ and at $D = D_{max} = 0.383$, which corresponds to the low line $V_I = V_{Imin} = 120.21\,\text{V}$. This power is given by

$$P_{rDS(max)} = \frac{2r_{DS}D_{max}V_O^2}{3f_s L_m R_{Lmin}} = \frac{2 \times 0.85 \times 0.383 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5} = 0.217\,\text{W}. \tag{5.214}$$

The conduction loss in the MOSFET at $D = D_{min} = 0.123$, which corresponds to the high line $V_I = V_{Imax} = 373.35\,\text{V}$, is

$$P_{rDS} = \frac{2r_{DS}D_{min}V_O^2}{3f_s L_m R_{Lmin}} = \frac{2 \times 0.85 \times 0.123 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5} = 0.070\,\text{W}. \tag{5.215}$$

The transistor output capacitance is $C_o = 100\,\text{pF}$. Hence, the switching loss at $V_{Imin} = 120.21\,\text{V}$ is

$$P_{sw} = f_s C_o V_{SM(min)}^2 = 10^5 \times 100 \times 10^{-12} \times 120.21^2 = 0.144\,\text{W}, \tag{5.216}$$

and the switching loss at $V_{Imax} = 373.35\,\text{V}$ is

$$P_{sw} = f_s C_o V_{SM(max)}^2 = 10^5 \times 100 \times 10^{-12} \times 373.35^2 = 1.394\,\text{W}. \tag{5.217}$$

The power loss in the MOSFET at V_{Imin} is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 0.217 + \frac{0.1445}{2} = 0.217 + 0.072 = 0.289\,\text{W} \tag{5.218}$$

and the power loss in the MOSFET at V_{Imax} is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 0.069 + \frac{1.394}{2} = 0.069 + 0.697 = 0.766\,\text{W}. \tag{5.219}$$

The conduction power loss in the diode due to R_F is

$$P_{RF} = \frac{2nR_F V_O^2}{3R_{Lmin}}\sqrt{\frac{2}{f_s L_m R_{Lmin}}}$$

$$= \frac{2 \times 5 \times 0.03 \times 15^2}{3 \times 7.5}\sqrt{\frac{2}{10^5 \times 300 \times 10^{-6} \times 7.5}} = 0.283\,\text{W}, \tag{5.220}$$

and the diode conduction loss due to V_F is

$$P_{VF} = V_F I_{Omax} = 0.35 \times 2 = 0.7\,\text{W}, \tag{5.221}$$

which gives the total diode conduction loss

$$P_D = P_{RF} + P_{VF} = 0.283 + 0.7 = 0.983\,\text{W}. \tag{5.222}$$

Let $r_{T1} = 1\,\Omega$ and $r_{T2} = 0.03\,\Omega$. Hence, the conduction loss in the primary at V_{Imin} is

$$P_{rT1(max)} = \frac{2r_{T1}D_{max}V_O^2}{3f_s L_m R_{Lmin}} = \frac{2 \times 1 \times 0.383 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5} = 0.255\,\text{W}, \tag{5.223}$$

and at V_{Imax} is

$$P_{rT1} = \frac{2r_{T1}D_{min}V_O^2}{3f_s L_m R_{Lmin}} = \frac{2 \times 1 \times 0.123 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5} = 0.082\,\text{W}, \tag{5.224}$$

and the conduction loss in the secondary winding is

$$P_{rT2} = \frac{2nr_{T2}V_O^2}{3R_{Lmin}}\sqrt{\frac{2}{f_s L_m R_{Lmin}}}$$

$$= \frac{2 \times 5 \times 0.03 \times 15^2}{3 \times 7.5}\sqrt{\frac{2}{10^5 \times 300 \times 10^{-6} \times 7.5}} = 0.283\,\text{W}. \tag{5.225}$$

Assume that $r_L = 0.5\,\Omega$. Thus, the power loss in r_L at V_{Imin} is

$$P_{rL(max)} = \frac{2r_L D_{max}V_O^2}{3f_s L_m R_{Lmin}}\left(1 + \sqrt{\frac{2f_s L_m}{n^2 D_{max}^2 R_{Lmin}}}\right)$$

$$= \frac{2 \times 0.5 \times 0.383 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5}\left(1 + \sqrt{\frac{2 \times 10^5 \times 300 \times 10^{-6}}{5^2 \times 0.383^2 \times 7.5}}\right) = 0.314\,\text{W}, \tag{5.226}$$

and at V_{Imax} is

$$P_{rL} = \frac{2r_L D_{min}V_O^2}{3f_s L_m R_{Lmin}}\left(1 + \sqrt{\frac{2f_s L_m}{n^2 D_{min}^2 R_{Lmin}}}\right)$$

$$= \frac{2 \times 0.5 \times 0.123 \times 15^2}{3 \times 10^5 \times 300 \times 10^{-6} \times 7.5}\left(1 + \sqrt{\frac{2 \times 10^5 \times 300 \times 10^{-6}}{5^2 \times 0.123^2 \times 7.5}}\right) = 0.2296\,\text{W}. \tag{5.227}$$

The total power loss and the converter efficiency at V_{Imin} and R_{Lmin} are

$$P_{LS} = P_{rDS(max)} + P_{sw} + P_D + P_{rT1(max)} + P_{rT2} + P_{rL(max)}$$
$$= 0.217 + 0.1445 + 0.983 + 0.255 + 0.283 + 0.314 = 2.1965\,\text{W} \tag{5.228}$$

and

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{30}{30 + 2.1965} = 93.18\,\%. \tag{5.229}$$

The total power loss and the converter efficiency at V_{Imax} and R_{Lmin} are

$$P_{LS} = P_{rDS} + P_{sw} + P_D + P_{rT1} + P_{rT2} + P_{rL}$$
$$= 0.069 + 1.394 + 0.982 + 0.082 + 0.283 + 0.2296 = 3.0396\,\text{W} \tag{5.230}$$

and

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{30}{30 + 3.0396} = 90.8\,\%. \tag{5.231}$$

Assuming that the rectangular gate-to-source voltage changes from 0 to $V_{GSpp} = 7\,\text{V}$, the gate-drive power is

$$P_G = f_s Q_g V_{GSpp} = 10^5 \times 42 \times 10^{-9} \times 7 = 29.4\,\text{mW}. \tag{5.232}$$

The efficiency η can be calculated from (5.189) and the duty cycle D from (5.195). Figures 5.23–5.28 show the efficiency η and the duty cycle D versus the dc input voltage V_I, load current I_O, and load resistance R_L for the flyback converter designed in the above example for DCM.

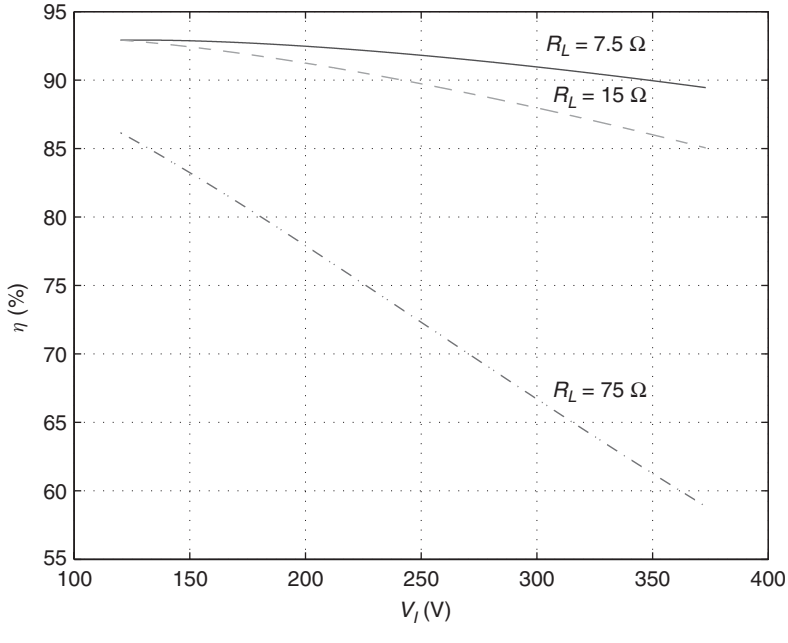


Figure 5.23 Efficiency η as a function of dc input voltage V_I at fixed load resistances for the flyback converter in DCM.

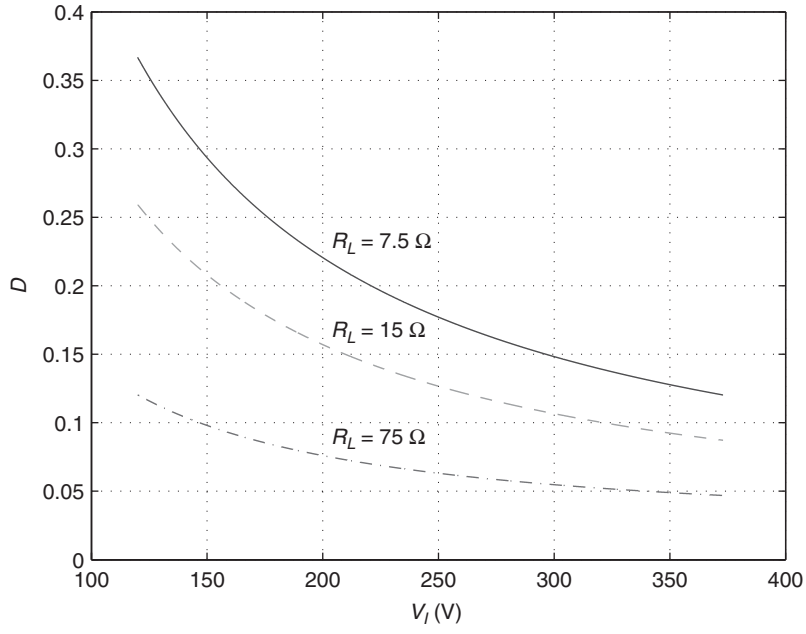


Figure 5.24 Duty cycle D as a function of dc input voltage V_I at fixed load resistances for the flyback converter in DCM.

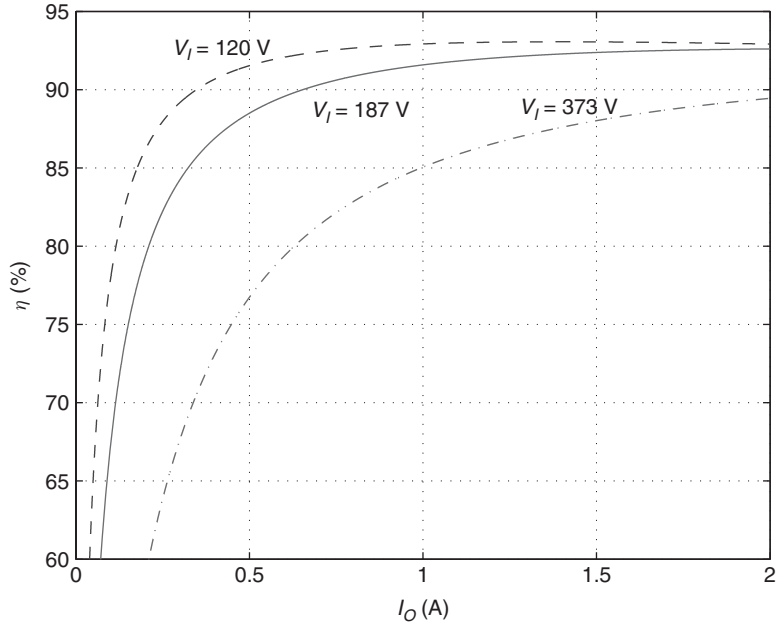


Figure 5.25 Efficiency η as a function of dc load current I_O at fixed load resistances for the flyback converter in DCM.

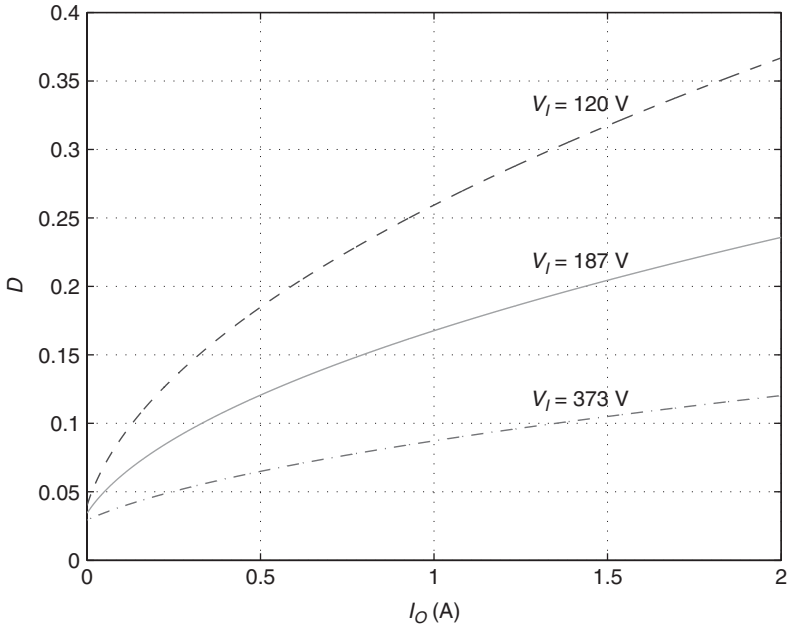


Figure 5.26 Duty cycle D as a function of dc load current I_O at fixed load resistances for the flyback converter in DCM.

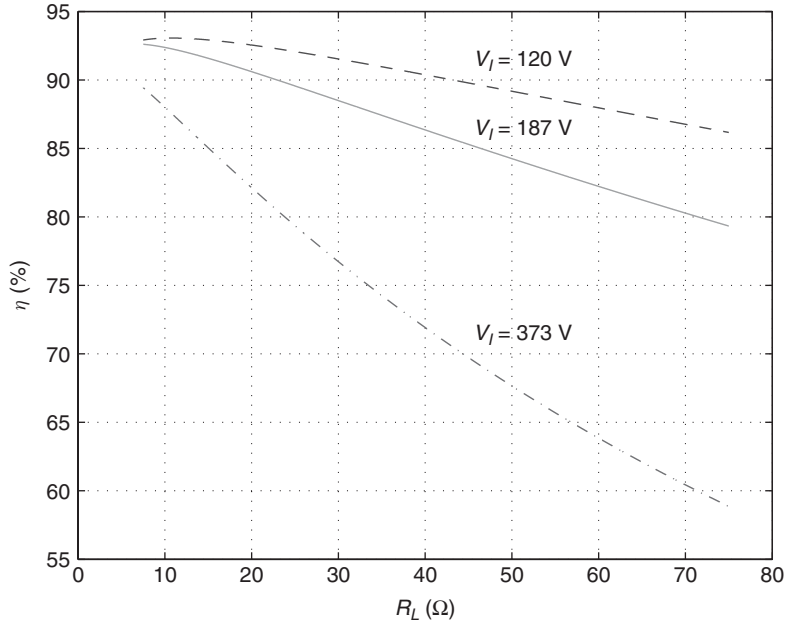


Figure 5.27 Efficiency η as a function of load resistance R_L at fixed dc input voltages for the flyback converter in DCM.

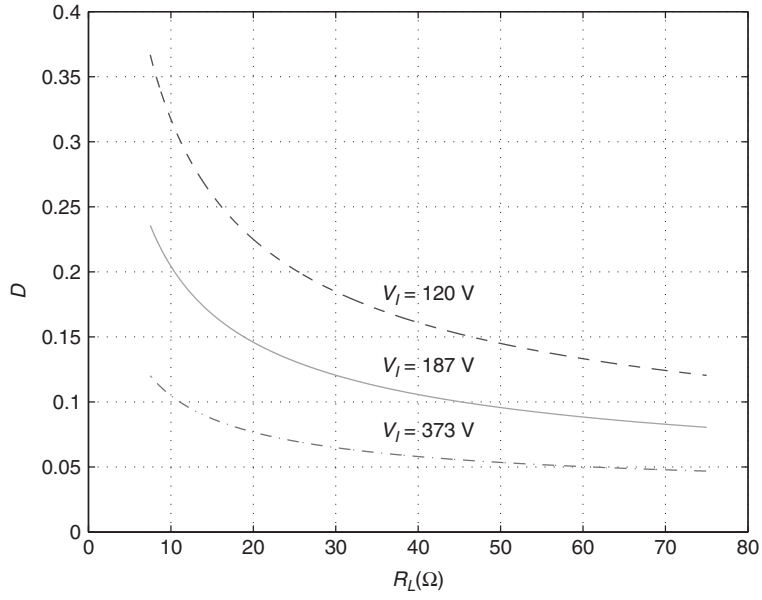


Figure 5.28 Duty cycle D as a function of load resistance R_L at fixed dc input voltages for the flyback converter in DCM.

5.5 Multiple-output Flyback Converter

In many applications such as computers, power supplies are required to provide several outputs at different voltages, which can be both positive and negative, and may be required to be isolated from each other. Multiple outputs can be obtained by adding additional secondary windings to the transformer, each with its own rectifier and output low-pass filter. Figure 5.29 shows an example of a two-output flyback converter. However, only one of the outputs can be regulated with a negative feedback loop by controlling the duty cycle D of the transistor, and other outputs are not regulated. Normally, the output with the highest output power is regulated. Other outputs will follow according to the duty cycle determined by the control loop of the main output. If the input voltage V_I increases, the duty cycle D is reduced for all outputs. If other outputs need to be regulated, a linear regulator or a magamp post-regulator may be added on each low-power output.

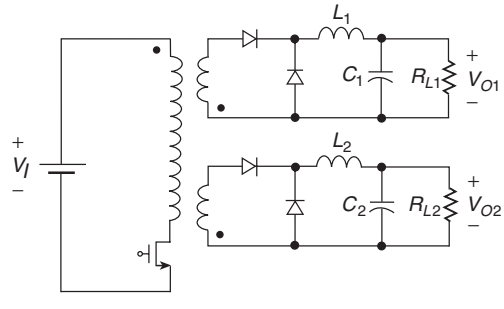


Figure 5.29 Multiple-output flyback converter.

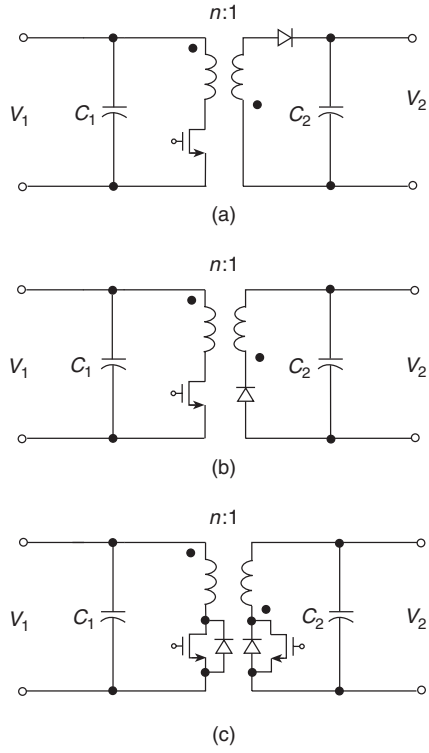


Figure 5.30 Derivation of a bidirectional flyback converter. (a) Unidirectional noninverting flyback converter. (b) Unidirectional noninverting flyback converter with the cathode of the diode connected to ground. (c) Bidirectional flyback converter.

5.6 Bidirectional Flyback Converter

A derivation of a bidirectional flyback converter is shown in Figure 5.30. A unidirectional noninverting flyback converter is depicted in Figure 5.30(a). Figure 5.30(b) shows the same converter with the cathode of the diode connected to ground. If the diode in this circuit is replaced by a MOSFET, a bidirectional flyback converter is obtained as depicted in Figure 5.30(c).

5.7 Ringing in Flyback Converter

The leakage inductance of transformers of all isolated dc–dc converters may lead to ringing, increased voltage stresses, and increased power loss, resulting in a significant degradation of circuit performance. The leakage inductance on the primary side of the transformer is given by

$$L_l = (1 - k)L_p, \tag{5.233}$$

where L_p is the inductance of the primary winding and k is the coupling coefficient. Typical values of k are in the range 0.98–0.99. For example, for $L_p = 2.5\,\text{mH}$ and $k = 0.98$, we obtain $L_l = (1 - 0.98) \times 2.5 \times 10^{-3} = 50\,\mu\text{H}$.

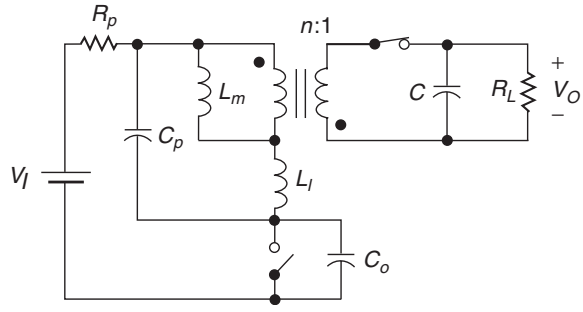


Figure 5.31 Equivalent circuit of flyback converter when the transistor is OFF.

In a single-transistor flyback converter, a voltage spike and ringing occur at the leading edge of the switch voltage v_S at each transistor turn-off due to the transformer leakage inductance L_l. A high voltage spike and ringing are superimposed on the steady-state transistor voltage $V_I + nV_O$. When the transistor is turned off, the transformer leakage inductance L_l, the transistor output capacitance $C_o = C_{oss} = C_{ds} + C_{gd}$, and the transformer stray input capacitance C_p form a resonant circuit, as shown in Figure 5.31. The current through the leakage inductance L_l is

$$i_{L_l} = I_{L_l}(0)e^{-\frac{R_p}{2L_l}t}\cos\omega_o t, \tag{5.234}$$

the voltage across the leakage inductance is

$$v_{L_l} = I_{L_l}(0)Z_o e^{-\frac{R_p}{2L_l}t}\sin\omega_o t = I_{SM}Z_o e^{-\frac{R_p}{2L_l}t}\sin\omega_o t = V_{L_l(pk)}e^{-\frac{R_p}{2L_l}t}\sin\omega_o t, \tag{5.235}$$

and the voltage across the switch is

$$v_S = V_I + nV_O + v_{L_l} = V_I + nV_O + I_{SM}Z_o e^{-\frac{R_p}{2L_l}t}\sin\omega_o t, \tag{5.236}$$

where $I_{L_l}(0) = I_{SM}$ is the current in the leakage inductance L_l just before the switch turns off, R_p is the primary winding resistance, $V_{L_l(pk)} = I_{SM}Z_o$, the frequency of ringing is

$$\omega_o = \frac{1}{\sqrt{L_l(C_o + C_p)}}, \tag{5.237}$$

and the characteristic impedance of the resonant circuit is

$$Z_o = \omega_o L_l = \frac{1}{\omega_o(C_o + C_p)} = \sqrt{\frac{L_l}{C_o + C_p}}. \tag{5.238}$$

Hence, the peak voltage across the switch is

$$V_{SM} = V_I + nV_O + I_{SM}Z_o. \tag{5.239}$$

The energy stored in the leakage inductance just before the transistor turns off is

$$W_{L_l} = \frac{1}{2}L_l I_{L_l}(0)^2 = \frac{1}{2}L_l I_{SM}^2, \tag{5.240}$$

resulting in power loss due to ringing

$$P_{ring} = \frac{W_{L_l}}{T} = f_s W_{L_l} = \frac{1}{2}f_s L_l I_{SM}^2. \tag{5.241}$$

Example 5.1

A flyback converter (designed for CCM) has $L_l = 50\,\mu\text{H}$, $C_o = 470\,\text{pF}$, $C_p = 30\,\text{pF}$, $I_{SMmax} = 1.418\,\text{A}$, $V_{SMmax} = 373\,\text{V}$, $n = 11$, $V_O = 5\,\text{V}$, and $f_s = 100\,\text{kHz}$. Find the ringing frequency, the maximum switch voltage, and the power loss due to ringing.

Solution. The ringing frequency is

$$f_o = \frac{1}{2\pi\sqrt{L_l(C_o + C_p)}} = \frac{1}{2\pi\sqrt{50 \times 10^{-6}(470 + 30) \times 10^{-12}}} = 1\,\text{MHz}, \tag{5.242}$$

the characteristic impedance is

$$Z_o = \sqrt{\frac{L_l}{C_o + C_p}} = \sqrt{\frac{50 \times 10^{-6}}{(470 + 30) \times 10^{-12}}} = 316.23\,\Omega, \tag{5.243}$$

the peak value of the voltage across the leakage inductance is

$$V_{L_l(pk)} = I_{SMmax} Z_o = 1.418 \times 316.23 = 448.4\,\text{V}, \tag{5.244}$$

the maximum value of the voltage across the switch is

$$V_{SMmax} = V_{Imax} + nV_O + Z_o I_{SMmax} = 373 + 11 \times 5 + 448.4 = 876.4\,\text{V}, \tag{5.245}$$

and the power loss due to ringing is

$$P_{ring} = \tfrac{1}{2} f_s L_l I_{SMmax}^2 = \tfrac{1}{2} \times 100 \times 10^3 \times 50 \times 10^{-6} \times 1.418^2 = 5.02\,\text{W}. \tag{5.246}$$

The switch conduction loss also increases because a transistor with a much higher breakdown voltage V_{DSS} and a much higher on resistance r_{DS} must be used.

One way to reduce the magnitude of ringing is to use a dissipative snubber, as shown in Figure 5.32. A large capacitance acts as a voltage source whose average voltage is nV_O. When the ringing voltage increases, the diode turns on and a constant voltage is dropped across the primary winding and a transistor. The peak voltage of the transistor is

$$V_{SM} = V_I + nV_O. \tag{5.247}$$

Most of the energy stored in the leakage inductance is lost in the snubber resistor R and the snubber diode.

In order to reduce the magnitude of the ringing, a voltage limiter (or voltage clamp) in the form of a Zener diode in series with a diode connected back-to-back may be

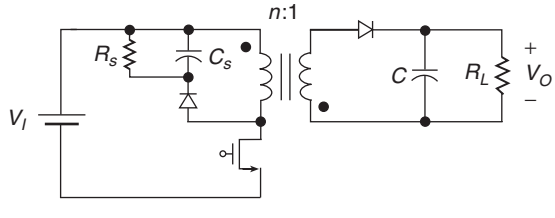


Figure 5.32 Flyback converter with dissipative snubber.

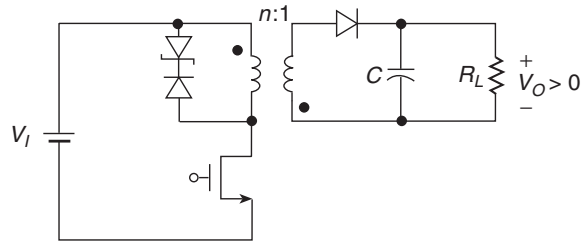


Figure 5.33 Flyback converter with a Zener diode voltage clamp across the transformer primary winding.

added across the transformer winding as shown in Figure 5.33. This is also a dissipative voltage clamp. When the transistor is turned off, the voltage across the primary winding reverses, and the diodes conduct. The voltage across the magnetizing inductance is $v_{Lm} = nV_O$. The Zener diode behaves like a dc voltage source with its voltage V_z. The voltage across the leakage inductance after the switch is turned off and the Zener diode turns on is $v_{L_l} = V_z + 0.7\,\text{V}$. The voltage across the switch after it is turned off is given by

$$V_{SM} = V_I + v_{Lm} + v_{L_l} = V_I + nV_O + V_z + 0.7\,\text{V}. \tag{5.248}$$

The current through the leakage inductance and the diodes decreases linearly. When the diode current reaches zero, the diodes turns off, and the voltage across the switch is expressed by

$$V_{SM} = V_I + nV_O. \tag{5.249}$$

The Zener diode voltage clamp is used in low-voltage converters, where $V_z \leq 50\,\text{V}$. It is not used in universal-input, off-line flyback converters.

5.8 Flyback Converter with Active Clamping

Figure 5.34 shows three nearly lossless active clamp circuits. These circuits may also provide zero-voltage switching, reducing switching losses, reducing EMI, and increasing the efficiency. The clamping circuit consists of transistor Q_2 and the coupling capacitor C_c. In the converter depicted in Figure 5.34(a), the clamping circuit is connected across the primary. This circuit is called the high-end n-channel active clamp. The main transistor Q_1 is driven with the duty cycle D, and the clamp transistor is driven with the duty cycle $1 - D$. The voltage across the clamp capacitor is

$$V_{Cc(H)} = nV_O + V_{Ll}, \tag{5.250}$$

where V_{Ll} is the voltage across the leakage inductance, which can be up to $0.4nV_O$. In the converter shown Figure 5.34(b), the clamping circuit is connected across the main switch. It is called the low-end n-channel active clamp. The voltage across the clamping capacitor C_c is

$$V_{Cc(H)} = V_I + nV_O + V_{Ll}. \tag{5.251}$$

In the converter shown Figure 5.34(c), the clamping circuit contains a p-channel MOSFET. This circuit is called the low-end p-channel active clamp.

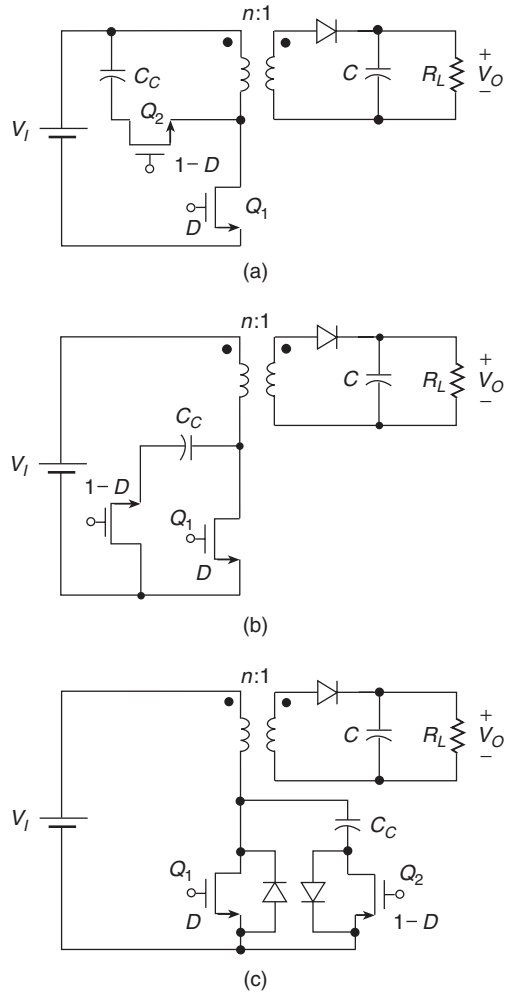


Figure 5.34 Flyback converter with clamp circuits to avoid ringing. (a) High-end n-channel active clamp. (b) Low-end n-channel active clamp. (c) Low-end p-channel active clamp.

5.9 Two-transistor Flyback Converter

A two-switch flyback converter with two fast diodes is shown in Figure 5.35. Both transistors are controlled by the same gate-to-drive voltage. When the transistors are turned off, the two clamping diodes D_2 and D_3 are forced to turn on by the current of the magnetizing inductance L_m and clamp the voltage across the transistor and the primary winding to V_I. Therefore, the magnitude of the ringing voltage is reduced, reducing the peak value at the leading edge transistor voltage. The current of the magnetizing inductance flows through the clamping diodes D_2 and D_3, and also through the rectifier diode D_1. The current of the two diodes decreases to zero with slope V_I/L_m. When the current of the clamping diodes reaches zero, the diodes turn off. The converter is used in DCM, especially at high dc input voltages V_I. The dc voltage transfer function of the two-transistor flyback converter is identical to that of the single-transistor flyback converter. The disadvantage of the two-transistor flyback converter is the floating gate driver of the high-side transistor.

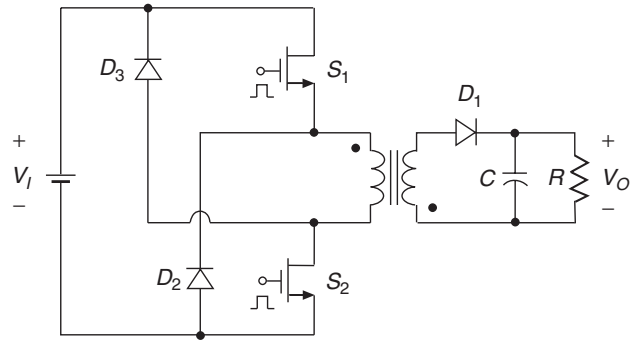


Figure 5.35 Two-transistor flyback converter.

5.10 Summary

- The flyback converter is the lowest-cost regulator because it has the lowest parts count and the output filter inductor is not required. It consists of only four components.
- The transformer provides dc isolation, its magnetizing inductance stores the energy, and no extra inductor is required.
- The flyback converter can be derived from the buck-boost converter by replacing the inductor with a transformer.
- The equations for the flyback converter are similar to those for the buck-boost converter. To obtain the equations for the flyback converter from the buck-boost converter, $M_{V\,DC}$ should be replaced by $nM_{V\,DC}$, V_I reflected to the secondary side of the transformer should be replaced by V_I/n, and the load current I_O reflected to the primary side of the transformer should be replaced by I_O/n.
- The flyback converter can be used as either a step-down or a step-up converter.
- It can be either an inverting or noninverting converter, depending on the polarity of the transformer, the rectifier diode, and the filter capacitor.
- The flyback converter may be used to build multiple-output power supplies.
- The voltage and current stresses are high in the flyback converter.
- The typical power range of the flyback converter is from 20 to 2000 W.
- For the lossless flyback converter, the dc voltage transfer function is $M_{V\,DC} = D/n(1 - D)$ for CCM.
- For the lossy converter, the dc voltage transfer has lower values than those for the lossless converter, especially for the duty cycle D close to 1. For this reason, the maximum value of the dc voltage transfer function is limited.
- The converter should not be used at D close to 1 because its efficiency is poor for D from 0.9 to 1.
- The peak-to-peak value of the current through the filter capacitor is large, equal to the peak-to-peak value of the diode current I_{DM}.

- The input current is pulsating.
- The corner frequency of the output filter $f_o = 1/(2\pi CR_L)$ depends on the load resistance R_L.
- It is very easy to drive the transistor in the flyback converter because the source is connected to ground.
- In the flyback converter, only one-half of the $B-H$ curve of the transformer core is utilized. Therefore, a core with an air gap and a relatively large volume is normally required to avoid saturation.

5.11 References

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5.12 Review Questions

5.1 What are the roles of the transformer in the flyback PWM converter?

5.2 Is the flyback converter a step-down or a step-up converter?

5.3 What is the useful range of the duty cycle for the flyback converter?

5.4 What is the useful range of the dc voltage transfer function for the flyback converter?

5.5 Is the transformer required to store energy in the flyback converter?

5.6 Is it difficult to drive the transistor in the flyback converter?

5.7 Is the peak-to-peak value of the current through the filter capacitor large in the flyback converter?

5.8 Is the flyback converter a complicated converter?

5.9 What is the typical range of the output power of the flyback converter?

5.10 Is the flyback converter an inverting or a noninverting converter?

5.11 Can the flyback converter be used in multiple-output power supplies? Draw an example circuit for such a converter.

5.12 Is the switch voltage stress low in the flyback converter?

5.13 Is the size of the magnetic core small in the flyback converter?

5.14 Is it useful to use a core with an air gap in the flyback converter?

5.13 Problems

5.1 The dc input voltage of a flyback PWM converter operating in CCM is the US single-phase rectified voltage and the dc output voltage is $V_O = 800\,\text{V}$. Find the transformer turns ratio n.

5.2 The dc input voltage of a flyback PWM converter is the US single-phase rectified voltage, the dc output voltage is $V_O = 800\,\text{V}$, and the transformer turns ratio is $n = 1/3$. Find the voltage stresses of the switch and the diode.

5.3 The dc input voltage of a flyback PWM converter is the US single-phase rectified voltage, the dc output voltage is $V_O = 800\,\text{V}$, the minimum load current is $I_{Omin} = 0.2\,\text{A}$, the maximum input voltage $V_{Imax} = 187\,\text{V}$, the switching frequency is $f_s = 50\,\text{kHz}$, the efficiency is $\eta = 0.95$, and the transformer turns ratio is $n = 1/3$. Find the minimum magnetizing inductance of the transformer to maintain the operation in CCM.

5.4 A flyback PWM converter is supplied by the US single-phase rectified line voltage, $V_O = 800\,\text{V}$, $I_O = 0.2$ to $0.5\,\text{A}$, the minimum input voltage $V_{Imin} = 127\,\text{V}$, the minimum duty cycle $D_{min} = 0.6$, $n = 1/3$, $L_m = 2\,\text{mH}$, and $f_s = 50\,\text{kHz}$. Find the current stresses of the switch and the diode.

5.5 A flyback PWM converter is supplied by the US single-phase rectified line voltage, $V_O = 800\,\text{V}$, $I_O = 0.2$ to $0.5\,\text{A}$, $n = 1/3$, the maximum dc input current is $I_{Imax} = 3.15\,\text{A}$, $M_{V\,DC} = 6.299$, $f_s = 50\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$. Find the filter capacitance.

5.6 Design a flyback PWM converter to meet the following specifications: $V_I = 270\,\text{Vdc} \pm 10\,\%$, $V_O = 28\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Find n, L_m, C, and η.

5.7 The dc input voltage of a flyback PWM converter is the US single-phase rectified voltage, the dc output voltage is $V_O = 800\,\text{V}$, the minimum load current is $I_{Omin} = 0\,\text{A}$, the maximum load current is $I_{Omax} = 0.5\,\text{A}$, the switching frequency is $f_s = 50\,\text{kHz}$, the efficiency is $\eta = 0.95$, and the transformer turns ratio is $n = 1/3$. Find the maximum magnetizing inductance of the transformer to maintain the operation in DCM.

5.8 Design a flyback converter to meet the following specifications: $V_I = 240$ to $300\,\text{Vdc}$, $V_O = 28\,\text{V}$, $I_O = 0.2$ to $2\,\text{A}$, $f_s = 200\,\text{kHz}$, $V_r/V_O \leq 1\,\%$, $r_L = 2\,\Omega$, $r_{DS} = 0.5\,\Omega$, $r_{T1} = 50\,\text{m}\Omega$, $r_{T2} = 10\,\text{m}\Omega$, $r_C = 50\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, $R_F = 25\,\text{m}\Omega$, and $C_o = 100\,\text{pF}$. Find n, D_{min}, D_{max}, L, C, and η.

5.9 Design a flyback converter whose V_I is the US rectified line voltage 92 to 132 Vrms, $V_O = 800\,\text{V}$, $I_O = 50$ to $500\,\text{mA}$, $V_r/V_O \leq 1\,\%$. Find L_m, C, r_C, I_{SM}, V_{SM}, and n.

5.10 Design a universal power supply that accepts a single-phase line voltage from 85 to 264 Vrms at $f = 50$ to $440\,\text{Hz}$, $V_O = 5\,\text{V}$, $I_O = 0$ to $10\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Assume $r_{DS} = 0.85\,\Omega$, $R_F = 10\,\text{m}\Omega$, $V_F = 0.3\,\text{V}$, $r_C = 2.5\,\text{m}\Omega$, $r_L = 0.35\,\Omega$, $r_{T1} = 0.9\,\Omega$, $r_{T2} = 0.02\,\Omega$, $f_s = 100\,\text{kHz}$, $C_o = 100\,\text{pF}$, and the initial efficiency $\eta = 80\,\%$.

5.11 Draw a circuit of a multiple-output flyback converter with $V_{O1} = 5\,\text{V}$, $V_{O2} = 12\,\text{V}$, and $V_{O3} = 12\,\text{V}$.

6

Forward PWM DC–DC Converter

6.1 Introduction

The PWM forward converter [1]–[20] is one of the most widely used converters. It is a single-ended isolated (i.e., transformer) converter and can be derived from the buck converter. Therefore, it belongs to the family of buck-derived converters. A core reset circuit is required in this converter. The transformer is not required to store magnetic energy. The switch must withstand high voltage stress. The forward converter is suitable for low- and medium-power applications, usually from 30 to 500 W. It is used in either single-output or multiple-output power supplies. This chapter presents a steady-state analysis of the PWM forward converter for both CCM and DCM. Design examples are given for both modes.

6.2 DC Analysis of PWM Forward Converter for CCM

6.2.1 Derivation of Forward PWM Converter

The forward converter can be derived from the buck converter by adding the transformer and diode D_1 between the switch and the diode D_2. Therefore, the forward converter is one of the buck-derived converters. Figure 6.1 shows the derivation of the forward converter. The buck converter is depicted in Figure 6.1(a). It is a transformerless converter. Its disadvantage is that the gate of the MOSFET is driven with respect to a 'hot point'. In Figure 6.1(b), an inductor L_m and a diode D_1 are added between the switch and the freewheeling diode D_2. Notice that the inductor L_m cannot be connected directly in parallel with the diode D_2 because the average steady-state voltage across the inductor is zero, whereas the average voltage across the diode is negative. To remove this contradiction, the diode D_1 is added between the inductor L_m and the diode D_2. The average voltage across the diode D_2 is

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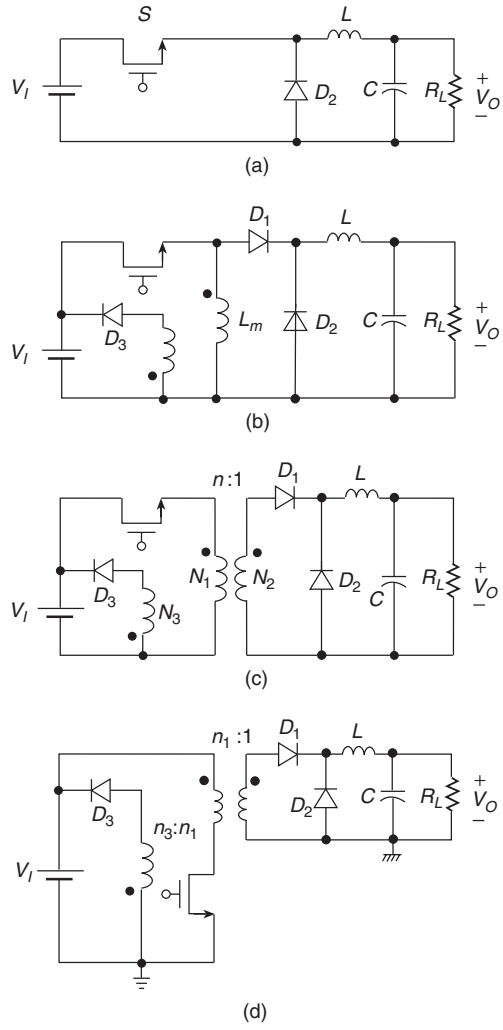


Figure 6.1 Derivation of the forward PWM converter. (a) Buck converter. (b) An inductor L_m, diode D_1, an additional winding, and diode D_3 are added to the buck converter. (c) Forward converter with the MOSFET gate driven with respect to a 'hot point'. (d) Forward converter with the MOSFET gate driven with respect to ground.

equal to the average voltage across the diode D_1. The switch and the diode D_1 are either ON or OFF during the same time intervals. In contrast, the diode D_2 is in the opposite state to both the switch and the diode D_1 for CCM. When the switch is ON, the voltage across the inductor L_m is equal to V_I and therefore the inductor current increases linearly. When the switch is turned off, the diode D_1 also turns off, making an open circuit for the inductor L_m. The current and the energy stored in the inductor L_m at this time are nonzero. Therefore, some provision must be made to demagnetize the inductor L_m. One way is to add an extra winding coupled to the inductor L_m and a diode D_3, as shown in Figure 6.1(b). The polarity of the extra winding must be such that the voltage across L_m is negative in order to cause the current through L_m to decrease. In addition, the switch must be held off long enough to allow the inductor current to decrease to zero. The energy stored in the inductor L_m at

the time the switch is turned off is returned to the dc input source V_I. The inductor L_m can be replaced by a transformer, resulting in the forward converter shown in Figure 6.1(c). Because the MOSFET is connected in series with the primary of the transformer, it can be shifted so that the gate is driven with respect to ground, as shown in Figure 6.1(d). The transformer core reset is obtained by adding a tertiary winding to the transformer (also called a clamp winding) in series with a diode D_3. It generally has the same number of turns as the primary in most applications and is usually bifilar wound. It clamps the voltage across the switch at twice the line voltage V_I if the number of turns if the primary and the tertiary are the same. Its main function is to return energy stored in the magnetizing inductance to the input voltage source V_I and therefore reset the core after each cycle of operation. The duty cycle of the switch is limited to allow the core to reset. Its maximum value is 50 % if the number of turns of the primary and the tertiary are the same. There are other core reset circuits, but most of them are lossy circuits.

A negative output voltage can be obtained by reversing the secondary and diodes D_1 and D_2. A multiple-output converter can be obtained by adding extra secondary windings, diodes D_1 and D_2, an inductor L, and a filter capacitor C.

The magnetizing inductance in the forward converter is not required to store energy. The transformer employs only one-half of the $B-H$ curve of the magnetic core. Therefore, the core usually requires an air gap and may be bulky. The input current waveform is pulsating, but an LC input filter can be added to obtain a nonpulsating input current. The forward converter is usually suitable for applications where the power level is between 30 and 500 W.

The analysis of the forward PWM converter of Figure 6.1(d) is based on the following assumptions:

1. The power MOSFET and the diode are ideal switches.
2. The transistor output capacitance, the diode capacitance, and the lead inductances are zero, which implies zero switching losses.
3. The transformer leakage inductances and stray capacitances are neglected.
4. Passive components are linear, time-invariant, and frequency-independent.
5. The output impedance of the input voltage source V_I is zero for both dc and ac components.

6.2.2 Time Interval $0 < t \leq DT$

During the time interval $0 < t \leq DT$, the switch and the diode D_1 are ON, and the diodes D_2 and D_3 are OFF. An ideal equivalent circuit for this time interval is shown in Figure 6.2(a). The actual transformer is modeled by an ideal transformer and the magnetizing inductance L_m. The relationship among the transformer voltages and the transformer turns ratio is

$$v_1 : v_2 : v_3 = N_1 : N_2 : (-N_3), \tag{6.1}$$

where N_1, N_2, and N_3 are the numbers of turns of the primary, secondary, and tertiary, respectively. The voltage ratio can also be expressed as

$$v_1 : v_2 : v_3 = \frac{N_1}{N_2} : 1 : \left(-\frac{N_3}{N_2}\right), \tag{6.2}$$

from which

$$v_1 : v_2 : v_3 = n_1 : 1 : (-n_3) \tag{6.3}$$

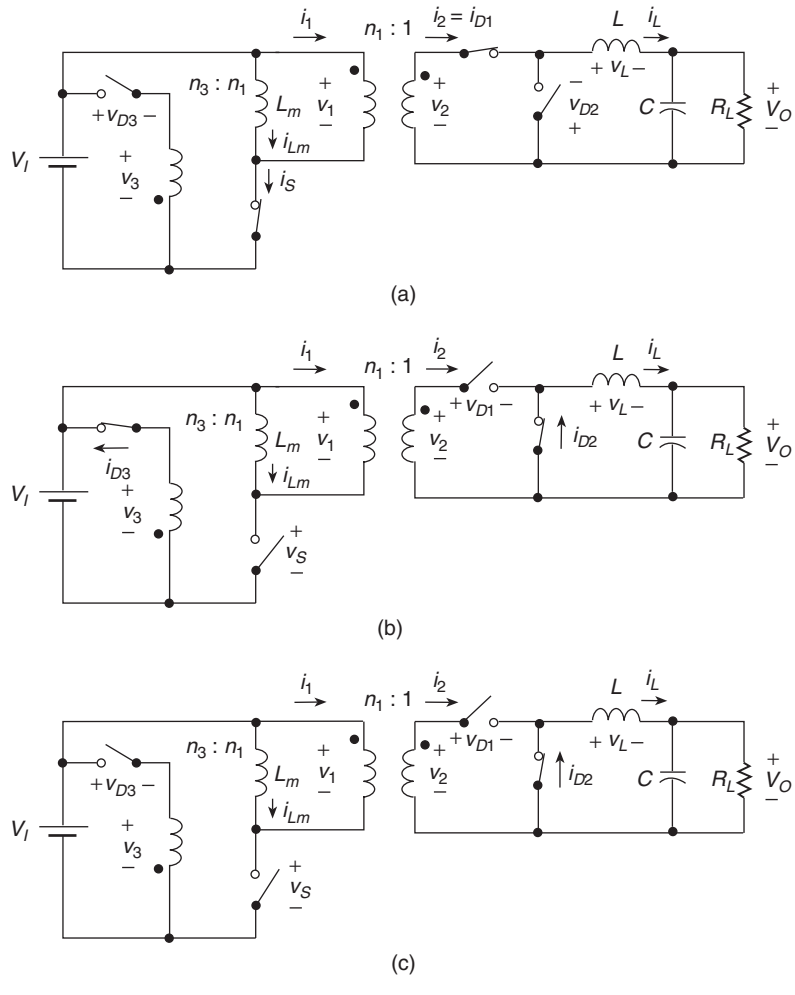


Figure 6.2 Equivalent circuits for different time intervals for the forward PWM converter operating in CCM. (a) For $0 < t \le DT$. (b) For $DT < t \le DT + t_m$. (c) For $DT + t_m < t \le T$.

where $n_1 = N_1/N_2$ and $n_3 = N_3/N_2$. The power balance for the ideal transformer is $i_1 v_1 = i_2 v_2 + i_3 v_3$, where $i_3 = i_{D3}$.

When the switch is ON, the voltage across the primary of the ideal transformer and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = V_I = L_m \frac{di_{Lm}}{dt}. \tag{6.4}$$

The boundary condition of the magnetizing inductance is $i_{Lm}(0) = 0$, as shown later. Hence, one obtains the current through the magnetizing inductance L_m,

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt = \frac{1}{L_m}\int_0^t V_I\,dt = \frac{V_I}{L_m}t. \tag{6.5}$$

The peak value of the magnetizing current is given by

$$\Delta i_{Lm} = i_{Lm}(DT) = \frac{V_I DT}{L_m} = \frac{DV_I}{f_s L_m}, \tag{6.6}$$

whose maximum value occurs at V_{Imax} and D_{min} or at V_{Imin} and D_{max},

$$\Delta i_{Lm(max)} = \frac{D_{min} V_{Imax}}{f_s L_{m(min)}}. \tag{6.7}$$

Thus, the minimum magnetizing inductance is

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{f_s \Delta i_{Lm(max)}}, \tag{6.8}$$

where $\Delta i_{Lm(max)}$ is usually 5–10 % of the maximum peak current of the ideal transformer primary I_{1max}.

The voltage across the secondary of the transformer is found to be

$$v_2 = \frac{v_1}{n_1} = \frac{V_I}{n_1}. \tag{6.9}$$

Thus, the voltage across inductance L is

$$v_L = \frac{V_I}{n_1} - V_O = L\frac{di_L}{dt}. \tag{6.10}$$

This leads to the current through the secondary, diode D_1, and inductance L,

$$i_2 = i_{D1} = i_L = \frac{1}{L}\int_0^t v_L\, dt + i_L(0) = \frac{\frac{V_I}{n_1} - V_O}{L} t + i_L(0). \tag{6.11}$$

Hence, one obtains the current through the primary of the transformer,

$$i_1 = \frac{i_2}{n_1} = \frac{\frac{V_I}{n_1} - V_O}{n_1 L} t + \frac{i_L(0)}{n_1}, \tag{6.12}$$

and the current through the switch,

$$i_S = i_1 + i_{Lm} = \frac{\frac{V_I}{n_1} - V_O}{n_1 L} t + \frac{i_L(0)}{n_1} + \frac{V_I}{L_m} t. \tag{6.13}$$

The voltage across the diode D_2 is

$$v_{D2} = -v_L - V_O = -\frac{V_I}{n_1}. \tag{6.14}$$

Using (6.4), one obtains the voltage across the tertiary winding,

$$v_3 = -\left(\frac{n_3}{n_1}\right) v_1 = -\left(\frac{n_3}{n_1}\right) V_I, \tag{6.15}$$

and the voltage across the diode D_3,

$$v_{D3} = v_3 - V_I = -\left(\frac{n_3}{n_1} + 1\right) V_I. \tag{6.16}$$

The waveforms in the forward converter for CCM are shown in Figure 6.3.

6.2.3 Time Interval $DT < t \leq DT + t_m$

Figure 6.2(b) shows an ideal equivalent circuit for the forward converter during the time interval $DT < t \leq DT + t_m$. During this time interval, the switch and diode D_1 are OFF,

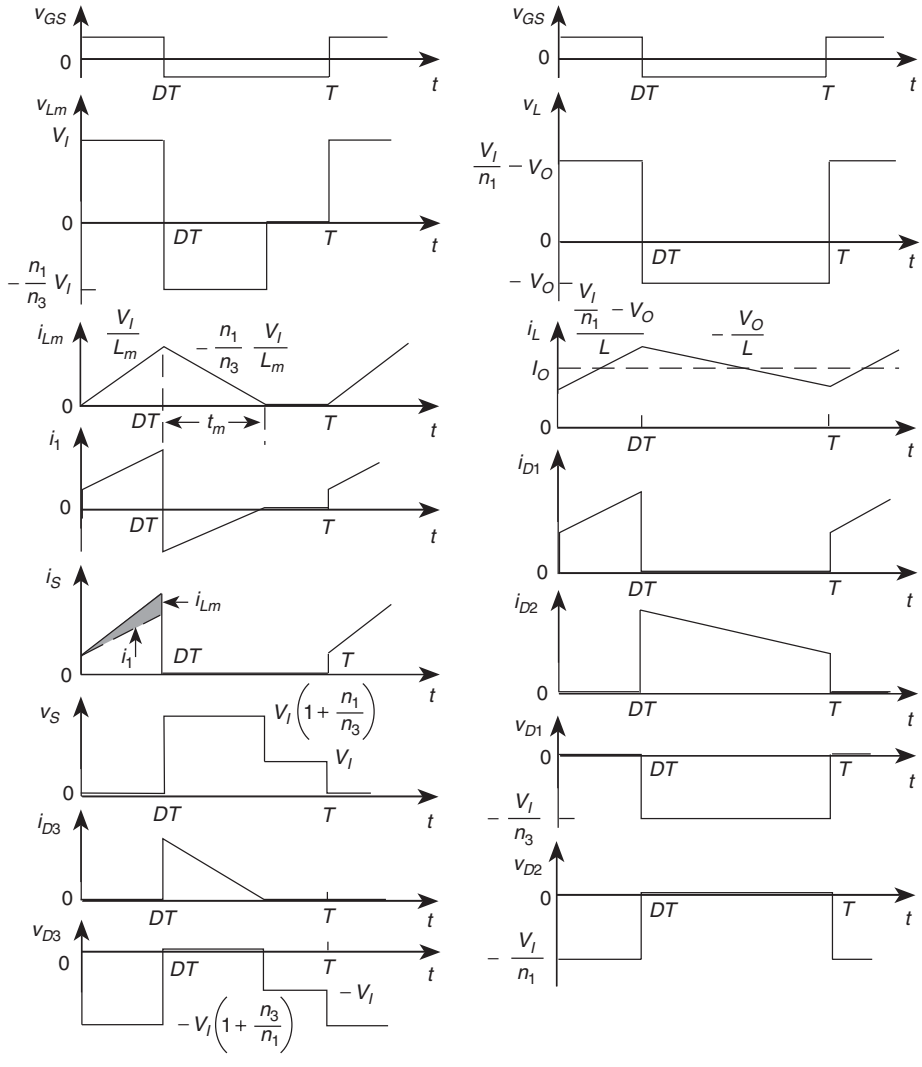


Figure 6.3 Waveforms in the PWM forward converter for CCM.

and the diodes D_2 and D_3 are ON. The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}. \tag{6.17}$$

Hence, the current through the inductor L and the diode D_2 can be found to be

$$i_{D2} = i_L = \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = -\frac{V_O}{L}\int_{DT}^{t} dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT), \tag{6.18}$$

where $i_L(DT)$ is the initial condition of the inductor L at $t = DT$. The peak-to-peak value of the current ripple through the inductor L is

$$\Delta i_L = i_L(DT) - i_L(T) = \frac{V_O T(1-D)}{L} = \frac{V_O(1-D)}{f_s L}. \tag{6.19}$$

Referring to Figure 6.2(b), the voltage across the tertiary is

$$v_3 = V_I. \tag{6.20}$$

Hence, the voltage across the primary and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = -\left(\frac{n_1}{n_3}\right) v_3 = -\left(\frac{n_1}{n_3}\right) V_I = L_m \frac{di_{Lm}}{dt}. \tag{6.21}$$

Hence,

$$i_{Lm} = \frac{1}{L_m}\int_{DT}^{t} v_{Lm}\, dt + i_{Lm}(DT) = -\frac{n_1 V_I}{n_3 L_m}(t - DT) + \frac{DV_I}{f_s L_m}, \tag{6.22}$$

$$i_1 = -i_{Lm} = \frac{n_1 V_I}{n_3 L_m}(t - DT) - \frac{DV_I}{f_s L_m}, \tag{6.23}$$

and

$$i_{D3} = -\left(\frac{n_1}{n_3}\right) i_1 = \left(\frac{n_1}{n_3}\right) i_{Lm} = -\frac{n_1^2 V_I}{n_3^2 L_m}(t - DT) + \frac{n_1 DV_I}{n_3 f_s L_m}. \tag{6.24}$$

The peak current of the diode D_3 occurs at $t = DT$ and is given by

$$I_{D3M} = i_{D3}(DT) = \left(\frac{n_1}{n_3}\right)\frac{DV_I}{f_s L_m}. \tag{6.25}$$

The voltages across the secondary and the diode D_1 are

$$v_{D1} = v_2 = -\frac{v_3}{n_3} = -\frac{V_I}{n_3}, \tag{6.26}$$

and the voltage across the switch is

$$v_S = V_I - v_1 = \left(\frac{n_1}{n_3} + 1\right) V_I. \tag{6.27}$$

At time $t = DT + t_m$, the current through the magnetizing inductance i_{Lm} and the diode current i_{D3} reach zero, terminating this time interval. Since $i_{Lm}(DT + t_m) = 0$,

$$t_m = \frac{n_3 D}{n_1 f_s} = \frac{n_3}{n_1} DT, \tag{6.28}$$

from which

$$t_{m(max)} = \frac{n_3 D_{max}}{n_1 f_s} = \frac{n_3}{n_1} D_{max} T. \tag{6.29}$$

For $n_3 = n_1$, $t_m = DT$ and $t_{m(max)} = D_{max}T$.

6.2.4 Time Interval $DT + t_m < t \leq T$

An equivalent circuit of the forward converter for the time interval $DT + t_m < t \leq T$ is shown in Figure 6.2(c). During this time interval, the switch, the diode D_1, and the diode D_3 are OFF and the diode D_2 is ON. The voltages across the transformer windings and the diode D_2 are $v_1 = v_2 = v_3 = v_{Lm} = 0$. The voltage across the switch is

$$v_S = V_I, \tag{6.30}$$

and the voltage across the diode D_3 is

$$v_{D3} = -V_I. \tag{6.31}$$

The voltage across the inductor L and the current through the diode D_2 and inductor L are given by (6.17) and (6.18), respectively.

6.2.5 Maximum Duty Cycle

To ensure the transformer core reset, the current through the magnetizing inductance L_m must decrease to zero in every cycle during steady-state operation. Otherwise, the current and the energy stored in the magnetizing inductance L_m at the end of each cycle would be greater than at the end of the previous cycle. This would lead to a catastrophic failure of the converter. Therefore, the duty cycle for the forward converter has its maximum permissible value D_{MAX}. The transformer core reset condition can be expressed as

$$DT + t_m \leq T \tag{6.32}$$

or

$$t_m \leq (1 - D)T. \tag{6.33}$$

For the worst case, this condition is

$$D_{MAX}T + t_m = T \tag{6.34}$$

or

$$t_m = (1 - D_{MAX})T. \tag{6.35}$$

The voltage across the magnetizing inductance v_{Lm} is V_I for $0 < t \leq DT$ and $-(n_1/n_3)V_I$ for $DT < t \leq DT + t_m$. Using the volt-second balance,

$$V_I D_{MAX} T = \left(\frac{n_1}{n_3}\right) V_I (1 - D_{MAX})T. \tag{6.36}$$

Rearranging this equation yields

$$D_{MAX} = \frac{\dfrac{n_1}{n_3}}{\dfrac{n_1}{n_3} + 1} = \frac{1}{\dfrac{n_3}{n_1} + 1}. \tag{6.37}$$

As the ratio n_3/n_1 increases from 0.25 to 4, D_{MAX} decreases from 0.8 to 0.2. For $n_3 = n_1$, $D_{MAX} = 0.5$. From (6.37),

$$\frac{n_3}{n_1} = \frac{1}{D_{MAX}} - 1. \tag{6.38}$$

Hence, from (6.27), the peak switch voltage becomes

$$V_{SM} = \left(\frac{n_1}{n_3} + 1\right) V_I = \frac{V_I}{1 - D_{MAX}}. \tag{6.39}$$

As n_3/n_1 increases from 0.25 to 4, V_{SM} increases from $1.25V_I$ to $5V_I$. For $n_3 = n_1$, $V_{SM} = 2V_I$. The peak switch voltage V_{SM} increases with increasing D_{MAX} (i.e., with increasing ratio n_1/n_3) and becomes very high at D_{MAX} close to 1. Therefore, one should avoid $D_{MAX} > 0.8$. In many applications, $n_3 = n_1$ is used.

6.2.6 Device Stresses

The peak switch voltage and current through the switch have maximum values

$$V_{SMmax} = \left(\frac{n_1}{n_3} + 1\right) V_{Imax} = \frac{V_{Imax}}{1 - D_{MAX}} \tag{6.40}$$

and

$$I_{SMmax} = \frac{I_{D1Mmax}}{n_1} + \Delta i_{Lm(max)} = \frac{I_{Omax}}{n_1} + \frac{\Delta i_{Lmax}}{2n_1} + \Delta i_{Lm(max)}. \tag{6.41}$$

The maximum value of the peak voltage across the diode D_1 is

$$V_{D1Mmax} = \frac{V_{Imax}}{n_3}, \tag{6.42}$$

the maximum value of the peak voltage across the diode D_2 is

$$V_{D2Mmax} = \frac{V_{Imax}}{n_1}, \tag{6.43}$$

and the peak values of the currents through the diodes D_1 and D_2 are

$$I_{D1Mmax} = I_{D2Mmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2}. \tag{6.44}$$

The maximum value of the peak voltage across the diode D_3 is

$$V_{D3Mmax} = \left(\frac{n_3}{n_1} + 1\right) V_{Imax} = \frac{V_{Imax}}{D_{MAX}}, \tag{6.45}$$

and the peak value of the current through diode D_3 is

$$I_{D3Mmax} = \left(\frac{n_1}{n_3}\right) \Delta i_{Lm(max)} = \left(\frac{n_1}{n_3}\right) \frac{D_{min} V_{Imax}}{f_s L_m}. \tag{6.46}$$

As n_3/n_1 increases from 0.25 to 4, V_{D3M} increases from $1.25V_I$ to $5V_I$. For $n_3 = n_1$, $V_{D3M} = 2V_I$.

6.2.7 DC Voltage Transfer Function for CCM

From Figure 6.3, the voltage across the inductor L is $v_L = V_I/n_1 - V_O$ for $0 < t \leq DT$ and $v_L = -V_O$ for $DT < t \leq T$. Applying the volt-second balance,

$$\left(\frac{V_I}{n_1} - V_O\right) DT = V_O(1 - D)T, \tag{6.47}$$

from which the dc voltage transfer function of the lossless converter is obtained:

$$M_{V\ DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{n_1}, \qquad \text{for } D \leq D_{MAX}. \tag{6.48}$$

The output voltage V_O is independent of the load resistance R_L. It depends only on the dc input voltage V_I. In most practical situations, $V_O = DV_I/n_1$ is constant. If V_I is increased, D should be decreased by a control circuit to keep V_O constant, and vice versa.

The dc current transfer function is given by

$$M_{I\ DC} \equiv \frac{I_O}{I_I} = \frac{n_1}{D}, \qquad \text{for } D \leq D_{MAX}. \tag{6.49}$$

From (6.40), (6.41), and (6.48), the switch and the diode utilization in the forward converter is characterized by the output-power capability

$$c_p \equiv \frac{P_O}{V_{SM} I_{SM}} = \frac{V_O I_O}{V_{SM} I_{SM}} = D. \tag{6.50}$$

As D is increased from 0 to 1, so does c_p.

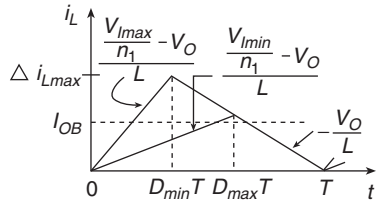


Figure 6.4 Waveforms of the inductor current at the CCM/DCM boundary V_{Imin} and V_{Imax}.

6.2.8 Boundary between CCM and DCM

Figure 6.4 shows the inductor current waveform i_L at the CCM/DCM boundary. This waveform can be described by

$$i_L = -\frac{V_O}{L}(t - DT) + i_L(DT), \qquad \text{for } DT < t \le T, \tag{6.51}$$

resulting in

$$i_L(T) = -\frac{V_O T(1-D)}{L} + i_L(DT) = 0, \tag{6.52}$$

from which

$$\Delta i_{Lmax} = \frac{V_O T(1 - D_{min})}{L_{min}} = \frac{V_O(1 - D_{min})}{f_s L_{min}}. \tag{6.53}$$

The dc output current at the CCM/DCM boundary is

$$I_{OB} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O(1 - D_{min})}{2f_s L_{min}} = \frac{V_O}{R_{Lmax}}. \tag{6.54}$$

The load resistance at the CCM/DCM boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{1 - D}, \quad \text{for } D \le D_{MAX}. \tag{6.55}$$

Hence, the minimum value of the inductance L is found to be

$$L_{min} = \frac{V_O(1 - D_{min})}{2f_s I_{OB}} = \frac{R_{Lmax}(1 - D_{min})}{2f_s} = \frac{D_{min}(\frac{V_{Imax}}{n_1} - V_O)}{2f_s I_{OB}}, \tag{6.56}$$

where $D_{min} = n_1 M_{V\,DCmin} = n_1 V_O / V_{Imax}$. Equation (6.56) is the same as that for the buck converter. Figures 6.5 and 6.6 respectively show the normalized load current $I_{OB}/(V_O/2f_s L) = 1 - D$ and load resistance $R_{LB}/(2f_s L) = 1/(1 - D)$ at the CCM/DCM boundary as functions of the duty cycle D for $D_{MAX} = 0.5$.

6.2.9 Ripple Voltage in Forward Converter for CCM

The ripple voltage for the forward converter can be found in the same way as for the buck converter. The peak-to-peak ripple on the output voltage is independent of the voltage across the filter capacitance and is determined only by the ripple voltage across the ESR if the following condition is satisfied:

$$C \ge C_{min} = \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{1 - D_{min}}{2f_s r_C}\right\}. \tag{6.57}$$

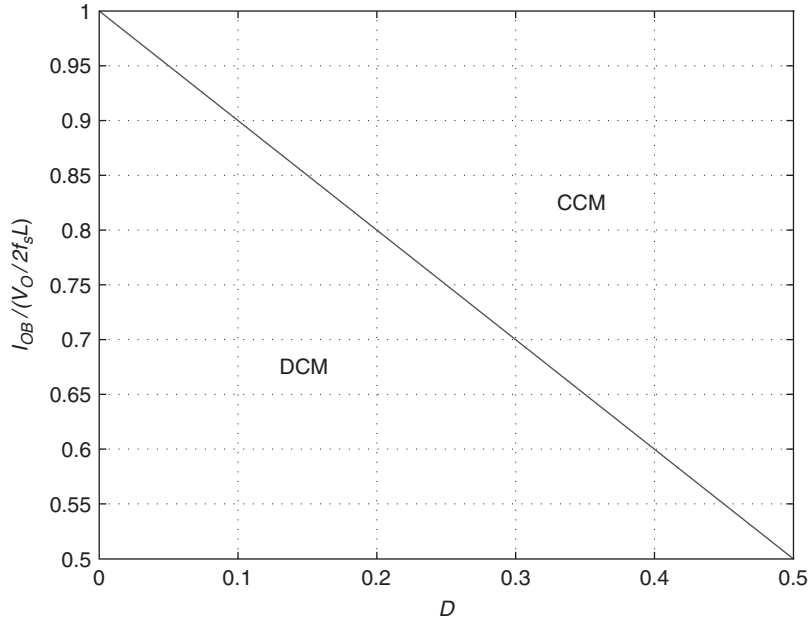


Figure 6.5 Normalized load current $I_{OB}/(V_O/2f_sL)$ at the CCM/DCM boundary as a function of the duty cycle for the forward converter at $D_{MAX} = 0.5$.

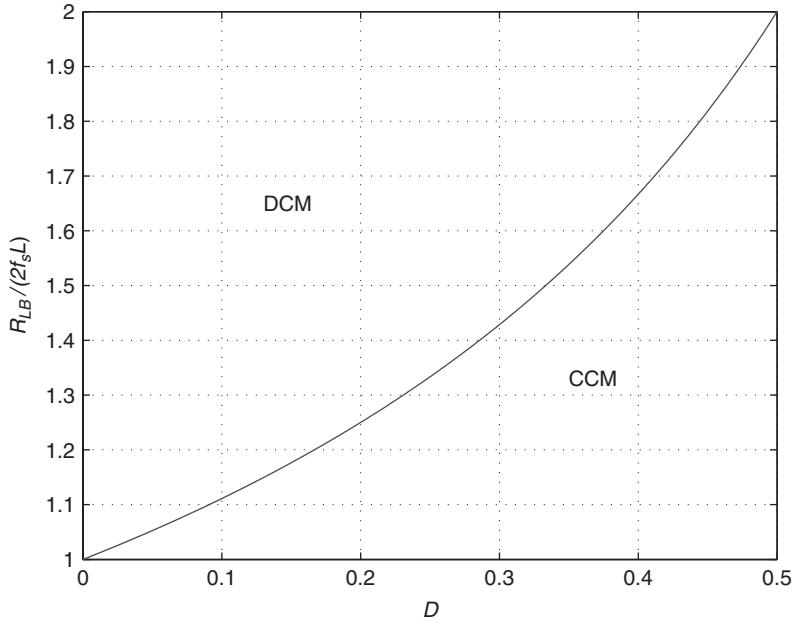


Figure 6.6 Normalized load Resistance $R_{LB}/(2f_sL)$ at the CCM/DCM boundary as a function of the duty cycle for the forward converter at $D_{MAX} = 0.5$.

In the worst case, $D_{min} = 0$. Thus, condition (6.57) is satisfied at any value of D if

$$C \geq C_{min} = \frac{1}{2r_C f_s}. \tag{6.58}$$

If condition (6.57) is satisfied, the peak-to-peak ripple voltage of the forward converter is

$$V_r = r_C \Delta i_{Lmax} = \frac{r_C V_O (1 - D_{min})}{f_s L}. \tag{6.59}$$

If condition (6.57) is not met, the voltages across the filter capacitance and the ESR contribute to the total output voltage ripple. The maximum increase in the charge stored in the filter capacitor is

$$\Delta Q = \frac{1}{2} \frac{T}{2} \frac{\Delta i_{Lmax}}{2} = \frac{\Delta i_{Lmax}}{8f_s}. \tag{6.60}$$

Hence, using (6.53), the peak-to-peak ripple voltage across the filter capacitance C is

$$V_{Cpp} = \frac{\Delta Q}{C} = \frac{\Delta i_{Lmax}}{8f_s C} = \frac{V_O (1 - D_{min})}{8f_s^2 LC} = \frac{(1 - D_{min})\pi^2 V_O f_o^2}{2f_s^2}, \tag{6.61}$$

where $f_o = 1/(2\pi\sqrt{LC})$ is the corner frequency of the output low-pass filter. The minimum capacitance is

$$C_{min} = \frac{\Delta i_{Lmax}}{8f_s V_{Cpp}} = \frac{(1 - D_{min})V_O}{8f_s^2 L V_{Cpp}}. \tag{6.62}$$

The peak-to-peak ripple voltage across the ESR is

$$V_{rcpp} = r_C \Delta i_{Lmax} = \frac{r_C V_O (1 - D_{min})}{f_s L}. \tag{6.63}$$

The total ripple of the output voltage is given by

$$V_r \approx V_{Cpp} + V_{rcpp} = \frac{V_O (1 - D_{min})}{8f_s^2 LC} + \frac{r_C V_O (1 - D_{min})}{f_s L}. \tag{6.64}$$

6.2.10 Power Losses and Efficiency of Forward Converter for CCM

Figure 6.7 depicts an equivalent circuit of the forward converter with parasitic resistances; r_{DS} is the MOSFET on-resistance, r_{T1} is the winding resistance of the primary, r_{T2} is the

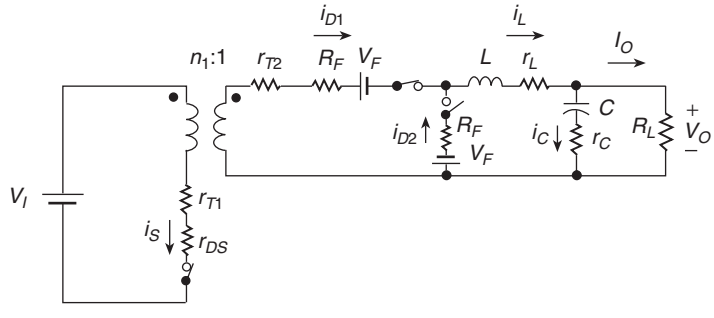


Figure 6.7 Equivalent circuit of the forward converter with parasitic resistances to determine component losses.

winding resistance of the secondary, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. Neglecting the ripple of the inductor current, the switch current can be approximated by

$$i_S = \begin{cases} \frac{I_O}{n_1}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{6.65}$$

which results in its rms value,

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \sqrt{\frac{1}{T}\int_0^{DT} \frac{I_O^2}{n_1^2}\, dt} = \frac{I_O\sqrt{D}}{n_1}, \tag{6.66}$$

and the conduction loss in the power MOSFET,

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{r_{DS} D I_O^2}{n_1^2} = \frac{D r_{DS}}{n_1^2 R_L} P_O. \tag{6.67}$$

Assuming that the transistor output capacitance C_o is linear, the switching loss is

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o V_O^2}{M_{V\ DC}^2} = \frac{f_s C_o R_L P_O}{M_{V\ DC}^2} = \frac{n_1^2 f_s C_o R_L}{D^2} P_O. \tag{6.68}$$

Hence, one obtains the total power dissipation in the MOSFET (excluding the drive power),

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \frac{D r_{DS} I_O^2}{n_1} + \frac{1}{2} f_s C V_I^2 = \left(\frac{D r_{DS}}{n_1^2 R_L} + \frac{f_s C_o R_L}{2 M_{V\ DC}^2} \right) P_O. \tag{6.69}$$

The conduction loss in the winding of the primary is

$$P_{rT1} = r_{T1} I_{Srms}^2 = \frac{r_{T1} D I_O^2}{n_1^2} = \frac{D r_{T1}}{n_1^2 R_L} P_O. \tag{6.70}$$

Let us assume that the diodes D_1 and D_2 are identical. The current through the diode D_1 and the secondary winding of the transformer can be approximated by

$$i_{D1} = \begin{cases} I_O, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{6.71}$$

producing its rms value,

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^T i_{D1}^2\, dt} = \sqrt{\frac{1}{T}\int_0^{DT} I_O^2\, dt} = I_O\sqrt{D}, \tag{6.72}$$

and the power losses in R_F,

$$P_{RF1} = R_F I_{D1rms}^2 = D R_F I_O^2 = \frac{D R_F}{R_L} P_O. \tag{6.73}$$

The average value of the current through the diode D_1 is

$$I_{D1} = \frac{1}{T}\int_0^T i_{D1}\, dt = \frac{1}{T}\int_0^{DT} I_O\, dt = D I_O, \tag{6.74}$$

which gives the power loss associated with the voltage V_F of diode D_1,

$$P_{VF1} = V_F I_{D1} = V_F I_O D = \frac{D V_F}{V_O} P_O. \tag{6.75}$$

Thus, the total conduction loss in diode D_1 is given by

$$P_{D1} = P_{VF1} + P_{RF1} = V_F I_O D + R_F I_O^2 D = P_O D \left(\frac{V_F}{V_O} + \frac{R_F}{R_L} \right). \tag{6.76}$$

The power loss in r_{T2} is

$$P_{rT2} = r_{T2} I_{D1rms}^2 = D r_{T2} I_O^2 = \frac{D r_{T2}}{R_L} P_O. \tag{6.77}$$

The power loss in both the primary and secondary winding is

$$P_{rT} = P_{rT1} + P_{rT2} = \left(\frac{r_{T1}}{n_1^2} + r_{T2} \right) \frac{D}{R_L} P_O. \tag{6.78}$$

The current of diode D_2 can be approximated by

$$i_{D2} = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ I_O, & \text{for } DT < t \le T, \end{cases} \tag{6.79}$$

yielding its rms value,

$$I_{D2rms} = \sqrt{\frac{1}{T} \int_0^T i_{D1}^2 \, dt} = \sqrt{\frac{1}{T} \int_{DT}^T I_O^2 \, dt} = I_O \sqrt{1 - D}, \tag{6.80}$$

and the power loss in R_F,

$$P_{RF2} = R_F I_{D2rms}^2 = (1 - D) R_F I_O^2 = \frac{(1 - D) R_F}{R_L} P_O. \tag{6.81}$$

The average value of the current through the diode D_2 is found to be

$$I_{D2} = \frac{1}{T} \int_0^T i_{D2} \, dt = \frac{1}{T} \int_{DT}^T I_O \, dt = (1 - D) I_O, \tag{6.82}$$

from which the power loss associated with the voltage V_F of diode D_2 is obtained as

$$P_{VF2} = V_F I_{D2} = V_F I_O (1 - D) = \frac{(1 - D) V_F}{V_O} P_O. \tag{6.83}$$

Thus, the overall conduction loss in diode D_2 is

$$P_{D2} = P_{VF2} + P_{RF2} = V_F I_O (1 - D) + R_F I_O^2 (1 - D) = P_O (1 - D) \left(\frac{V_F}{V_O} + \frac{R_F}{R_L} \right). \tag{6.84}$$

The power losses in the diode D_3 and the tertiary winding as well as the power transferred back from the magnetizing inductance to the input voltage source V_I are neglected.

The inductor current is

$$i_L \approx I_O, \tag{6.85}$$

leading to its rms value,

$$I_{Lrms} = I_O, \tag{6.86}$$

and the inductor conduction loss,

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 = \frac{r_L}{R_L} P_O. \tag{6.87}$$

The current through the filter capacitor can be expressed as

$$i_C = \begin{cases} \dfrac{\Delta i_L t}{DT} - \dfrac{\Delta i_L}{2}, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L (t - DT)}{(1 - D)T} + \dfrac{\Delta i_L}{2}, & \text{for } DT < t \le T. \end{cases} \tag{6.88}$$

Using (6.19) and (6.88), the rms current through the filter capacitor is found to be

$$I_{Crms} = \sqrt{\frac{1}{T} \int_0^T i_C^2 \, dt} = \frac{\Delta i_L}{\sqrt{12}} = \frac{V_O (1 - D)}{\sqrt{12} f_s L}, \tag{6.89}$$

and the power loss in the filter capacitor is

$$P_{rC} = r_C I_{Crms}^2 = \frac{r_C(\Delta i_L)^2}{12} = \frac{r_C V_O^2(1-D)^2}{12 f_s^2 L^2} = \frac{r_C R_L(1-D)^2}{12 f_s^2 L^2} P_O. \tag{6.90}$$

Neglecting the power loss in the transformer core reset circuit, the overall power loss is given by

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_{D1} + P_{D2} + P_{rT1} + P_{rT2} + P_{rL} + P_{rC} \\ &= \frac{D(r_{DS} + r_{T1})I_O^2}{n_1^2} + f_s C_o V_I^2 + V_F I_O + R_F I_O^2 + D r_{T2} I_O^2 + r_L I_O^2 + \frac{r_C \Delta i_L^2}{12} \\ &= P_O \left[\frac{D(r_{DS} + r_{T1})}{n_1^2 R_L} + \frac{r_L + R_F + D r_{T2}}{R_L} + \frac{V_F}{V_O} + \frac{f_s C_o R_L}{M_{V\ DC}^2} + \frac{r_C R_L (1-D)^2}{12 f_s^2 L^2} \right]. \end{aligned} \tag{6.91}$$

Thus, the converter efficiency is

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \frac{P_{LS}}{P_O}} \\ &= \frac{1}{1 + \frac{V_F}{V_O} + \frac{D(r_{DS} + r_{T1})}{n_1^2 R_L} + \frac{r_L + R_F + D r_{T2}}{R_L} + \frac{f_s C_o R_L}{M_{V\ DC}^2} + \frac{r_C R_L (1-D)^2}{12 f_s^2 L^2}}. \end{aligned} \tag{6.92}$$

6.2.11 DC Voltage Transfer Function of Lossy Converter for CCM

The dc component of the input current is

$$I_I = \frac{1}{T}\int_0^T i_S\, dt = \frac{1}{T}\int_0^T \frac{I_O}{n_1}\, dt = \frac{D I_O}{n_1}, \tag{6.93}$$

yielding the dc current transfer function of the forward converter,

$$M_{I\ DC} \equiv \frac{I_O}{I_I} = \frac{n_1}{D}. \tag{6.94}$$

This transfer function is the same for both lossless and lossy converters. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\ DC} M_{I\ DC} = \frac{n_1 M_{V\ DC}}{D}, \tag{6.95}$$

from which the dc voltage transfer function of the lossy forward converter is

$$\begin{aligned} M_{V\ DC} &= \frac{\eta}{M_{I\ DC}} = \frac{\eta D}{n_1} \\ &= \frac{D}{n_1 \left[1 + \frac{V_F}{V_O} + \frac{D(r_{DS} + r_{T1})}{n_1^2 R_L} + \frac{R_F + r_L + D r_{T2}}{R_L} + \frac{f_s C_o R_L}{M_{V\ DC}^2} + \frac{r_C R_L (1-D)^2}{12 f_s^2 L^2} \right]}. \end{aligned} \tag{6.96}$$

From (6.96), the on-duty cycle is

$$D = \frac{n_1 M_{V\ DC}}{\eta}. \tag{6.97}$$

The duty cycle D is greater for the lossy converter than for the lossless converter at a given dc voltage transfer function.

Substituting (6.97) into (6.92), one obtains the efficiency for the forward converter in CCM,

$$\eta = \frac{N_\eta}{D_\eta}, \tag{6.98}$$

where

$$\begin{aligned} N_\eta = 1 &- n_1 M_{V\ DC}\left(\frac{r_{DS}+r_{T1}}{n_1^2 R_L} + \frac{r_{T2}}{R_L} - \frac{r_C R_L}{6 f_s^2 L^2}\right) \\ &+ \left\{\left[n_1 M_{V\ DC}\left(\frac{r_{DS}+r_{T1}}{n_1^2 R_L} + \frac{r_{T2}}{R_L} - \frac{r_C R_L}{6 f_s^2 L^2}\right) - 1\right]^2 \right. \\ &\left. - \left[\frac{R_L r_C n_1^2 M_{V\ DC}^2}{3 f_s^2 L^2}\left(1 + \frac{V_F}{V_O} + \frac{r_L + R_F}{R_L} + \frac{f_s C_o R_L}{M_{V\ DC}^2} + \frac{r_C R_L}{12 f_s^2 L^2}\right)\right]\right\}^{\frac{1}{2}} \end{aligned} \tag{6.99}$$

and

$$D_\eta = 2\left(1 + \frac{V_F}{V_O} + \frac{r_L + R_F}{R_L} + \frac{f_s C_o R_L}{M_{V\ DC}^2} + \frac{r_C R_L}{12 f_s^2 L^2}\right). \tag{6.100}$$

6.2.12 Design of Forward Converter for CCM

Design a PWM forward converter operating in CCM to meet the following specifications: $V_O = 5\,\text{V}$, $I_{Omin} = 2\,\text{A}$, $I_{Omax} = 20\,\text{A}$, $V_r/V_O \leq 1\,\%$, and the input voltage is the US single-phase utility line rectified voltage.

Solution. The minimum, nominal, and maximum values of the input voltage are

$$V_{Imin} = \sqrt{2} \times V_{rms(min)} = \sqrt{2} \times 90 = 127\,\text{V}, \tag{6.101}$$

$$V_{Inom} = \sqrt{2} \times V_{rms(nom)} = \sqrt{2} \times 110 = 156\,\text{V}, \tag{6.102}$$

and

$$V_{Imax} = \sqrt{2} \times V_{rms(max)} = \sqrt{2} \times 132 = 187\,\text{V}. \tag{6.103}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{5}{187} = 0.02674 = \frac{1}{37.4}, \tag{6.104}$$

$$M_{V\ DCnom} = \frac{V_O}{V_{Inom}} = \frac{5}{156} = 0.03205 = \frac{1}{31.2}, \tag{6.105}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{5}{127} = 0.03937 = \frac{1}{25.4}. \tag{6.106}$$

The maximum and minimum values of the dc output power are

$$P_{Omax} = V_O I_{Omax} = 5 \times 20 = 100\,\text{W} \tag{6.107}$$

and

$$P_{Omin} = V_O I_{Omin} = 5 \times 2 = 10\,\text{W}. \tag{6.108}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{5}{20} = 0.25\,\Omega \tag{6.109}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{5}{2} = 2.5\,\Omega. \tag{6.110}$$

Let us assume the switching frequency $f_s = 100\,\text{kHz}$, the converter efficiency $\eta = 80\,\%$ and $D_{max} \approx 0.4$. The transformer turns ratio is

$$n_1 = \frac{\eta D_{max}}{M_{V\,DCmax}} = \frac{0.8 \times 0.4}{0.03937} = 8.128. \tag{6.111}$$

Pick $n_1 = n_3 = 8$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{n_1 M_{V\,DCmin}}{\eta} = \frac{8 \times 0.02674}{0.8} = 0.2674 \tag{6.112}$$

$$D_{nom} = \frac{n_1 M_{V\ DCnom}}{\eta} = \frac{8 \times 0.03205}{0.8} = 0.3205 \tag{6.113}$$

and

$$D_{max} = \frac{n_1 M_{V\,DCmax}}{\eta} = \frac{8 \times 0.03937}{0.8} = 0.3937. \tag{6.114}$$

Hence, $t_{m(max)}/T = D_{max} = 0.3937$. The maximum permissible duty cycle is

$$D_{MAX} = \frac{1}{\dfrac{n_3}{n_1} + 1} = \frac{1}{1+1} = 0.5. \tag{6.115}$$

Thus, $D_{max} < D_{MAX}$.

The minimum inductance is

$$L_{min} = \frac{R_{Lmax}(1 - D_{min})}{2f_s} = \frac{2.5 \times (1 - 0.2674)}{2 \times 10^5} = 9.1575\,\mu\text{H}. \tag{6.116}$$

Let $L = 20\,\mu\text{H}$.

The maximum peak-to-peak value of the inductor ripple current is

$$\Delta i_{Lmax} = \frac{V_O(1 - D_{min})}{f_s L} = \frac{5 \times (1 - 0.2674)}{10^5 \times 20 \times 10^{-6}} = 1.832\,\text{A}. \tag{6.117}$$

The ripple voltage is

$$V_r = 0.01 V_O = 0.01 \times 5 = 50\,\text{mV}. \tag{6.118}$$

The maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{50}{1.832} = 27.29\,\text{m}\Omega. \tag{6.119}$$

Let $r_C = 25\,\text{m}\Omega$. Thus, the filter capacitance is

$$\begin{aligned} C_{min} &= \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{1 - D_{min}}{2f_s r_C}\right\} = \max\left\{\frac{0.3937}{2f_s r_C}, \frac{1 - 0.2674}{2f_s r_C}\right\} \\ &= \frac{1 - D_{min}}{2f_s r_C} = \frac{1 - 0.2674}{2 \times 10^5 \times 0.025} = 146.52\,\mu\text{F}. \end{aligned} \tag{6.120}$$

Pick $C = 200\,\mu\text{F}/16\,\text{V}/25\,\text{m}\Omega$.

The corner frequency of the low-pass output filter is

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{20\times10^{-6}\times200\times10^{-6}}} = 2.516\,\text{kHz}. \tag{6.121}$$

Hence, $f_s/f_o = 100/2.516 = 39.74$.

The voltage stresses of the rectifier diodes are

$$V_{D1Mmax} = \frac{V_{Imax}}{n_3} = \frac{187}{8} = 23.375\,\text{V}, \tag{6.122}$$

$$V_{D2Mmax} = \frac{V_{Imax}}{n_1} = \frac{187}{8} = 23.375\,\text{V}, \tag{6.123}$$

and the current stresses of these diodes are

$$I_{D1Mmax} = I_{D2Mmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = 20 + \frac{1.832}{2} = 20.916\,\text{A}. \tag{6.124}$$

The maximum peak current through the primary of the ideal transformer is

$$I_{1max} = \frac{I_{D1Mmax}}{n_1} = \frac{20.916}{8} = 2.615\,\text{A}. \tag{6.125}$$

Assume that the maximum peak current through the magnetizing inductance is less than 10 % of the maximum peak current through the primary of the ideal transformer. Thus,

$$\Delta i_{Lm(max)} = 0.1 I_{1max} = 0.1\times2.615 = 0.262\,\text{A}. \tag{6.126}$$

The minimum magnetizing inductance is then

$$L_{m(min)} = \frac{D_{min}V_{Imax}}{f_s\,\Delta i_{Lm(max)}} = \frac{0.2674\times187}{100\times10^3\times0.262} = 1.9\,\text{mH}. \tag{6.127}$$

Pick $L_m = 2$ mH.

The stresses of the diode D_3 are

$$V_{D3Mmax} = \left(\frac{n_3}{n_1}+1\right)V_{Imax} = 2V_{Imax} = 2\times187 = 374\,\text{V} \tag{6.128}$$

and

$$I_{D3Mmax} = \left(\frac{n_1}{n_3}\right)\Delta i_{Lm(max)} = 0.262\,\text{A}. \tag{6.129}$$

The voltage and current stresses of the switch are

$$V_{SMmax} = \left(\frac{n_1}{n_3}+1\right)V_{Imax} = 2V_{Imax} = 2\times187 = 374\,\text{V} \tag{6.130}$$

and

$$I_{SMmax} = I_{1max} + \Delta i_{Lm(max)} = 2.614 + 0.262 = 2.877\,\text{A}. \tag{6.131}$$

An International Rectifier IRF740 power MOSFET is selected, which has $V_{DSS} = 400\,\text{V}$, $I_{SM} = 10\,\text{A}$, $r_{DS} = 0.55\,\Omega$, $Q_{g(typ)} = 41$ nC, $Q_{gmax} = 60$ nC, and $C_o = 100$ pF. Two MBR2540 Schottky barrier diodes are chosen, each having $I_{DM} = 25\,\text{A}$, $V_{DM} = 40\,\text{V}$, $V_F = 0.3\,\text{V}$, and $R_F = 16\,\text{m}\Omega$. A fast recovery MR826 diode is selected with $V_{DM} = 600\,\text{V}$ and $I_{DM(AV)} = 5\,\text{A}$.

We will calculate power losses for $P_{Omax} = 100\,\text{W}$ and $V_{Imax} = 373\,\text{V}$. The conduction power loss in the MOSFET is

$$P_{rDS} = \frac{r_{DS}D_{max}I_{Omax}^2}{n_1^2} = \frac{0.55\times0.3937\times20^2}{8^2} = 1.353\,\text{W}, \tag{6.132}$$

and the switching loss is

$$P_{sw} = f_s C_o V_{Imin}^2 = 10^5 \times 100 \times 10^{-12} \times 127^2 = 0.161\,\text{W}. \tag{6.133}$$

Assuming $r_{T1} = 50\,\text{m}\Omega$,

$$P_{rT1} = \frac{r_{T1} D_{max} I_{Omax}^2}{n_1^2} = \frac{0.05 \times 0.3937 \times 20^2}{8^2} = 0.123\,\text{W}. \tag{6.134}$$

The power loss due to R_F in diode D_1 is

$$P_{RF1} = D_{max} R_F I_{Omax}^2 = 0.3937 \times 0.016 \times 20^2 = 2.52\,\text{W}, \tag{6.135}$$

and the power loss due to V_F in diode D_1 is

$$P_{VF1} = V_F I_{Omax} D_{max} = 0.3 \times 20 \times 0.3937 = 2.362\,\text{W}, \tag{6.136}$$

resulting in the conduction loss in diode D_1,

$$P_{D1} = P_{RF1} + P_{VF1} = 2.52 + 2.362 = 4.882\,\text{W}. \tag{6.137}$$

Assuming $r_{T2} = 10\,\text{m}\Omega$,

$$P_{rT2} = D_{max} r_{T2} I_{Omax}^2 = 0.3937 \times 0.01 \times 20^2 = 1.575\,\text{W}. \tag{6.138}$$

Hence, the power loss in both primary and secondary windings is

$$P_{rT} = P_{rT1} + P_{rT2} = 0.123 + 1.575 = 1.698\,\text{W}. \tag{6.139}$$

The power loss due to R_F in diode D_2 is

$$P_{RF2} = (1 - D_{max}) R_F I_{Omax}^2 = (1 - 0.3937) \times 0.016 \times 20^2 = 3.88\,\text{W}, \tag{6.140}$$

the power loss due to V_F in diode D_2 is

$$P_{VF2} = (1 - D_{max}) V_F I_{Omax} = (1 - 0.3937) \times 0.3 \times 20 = 3.64\,\text{W}, \tag{6.141}$$

and the conduction loss in diode D_2 is

$$P_{D2} = P_{RF2} + P_{VF2} = 3.88 + 3.64 = 7.52\,\text{W}. \tag{6.142}$$

Assuming that the dc ESR of the inductor is $r_L = 15\,\text{m}\Omega$, one obtains the power loss in the inductor ESR

$$P_{rL} = r_L I_{Omax}^2 = 0.015 \times 20^2 = 6\,\text{W}, \tag{6.143}$$

the power loss in the capacitor ESR

$$P_{rC} = \frac{r_C (\Delta i_{Lmax})^2}{12} = \frac{0.025 \times 1.832^2}{12} = 7\,\text{mW}, \tag{6.144}$$

the total power loss

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_{rT1} + P_{rT2} + P_{D1} + P_{D2} + P_{rL} + P_{rC} \\ &= 1.353 + 0.161 + 0.123 + 1.575 + 4.882 + 7.52 + 6 + 0.007 = 21.621\,\text{W}, \end{aligned} \tag{6.145}$$

and the efficiency of the converter

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{100}{100 + 21.621} = 82.22\,\%. \tag{6.146}$$

If the magnitude of the gate-to-source voltage is $V_{GSm} = 7$ V, then the gate-drive power is

$$P_G = f_s Q_{gmax} V_{GSm} = 10^5 \times 60 \times 10^{-9} \times 7 = 42\,\text{mW}. \tag{6.147}$$

The efficiency η can be calculated from (6.98)–(6.100). Once the efficiency is known, the duty cycle D can be computed from (6.97). Figures 6.8–6.13 show the characteristics of the forward converter designed. It can be seen that the efficiency η decreases as I_O increases (or R_L decreases). The minimum efficiency η_{min} occurs at I_{Omax}. The duty cycle D increases as

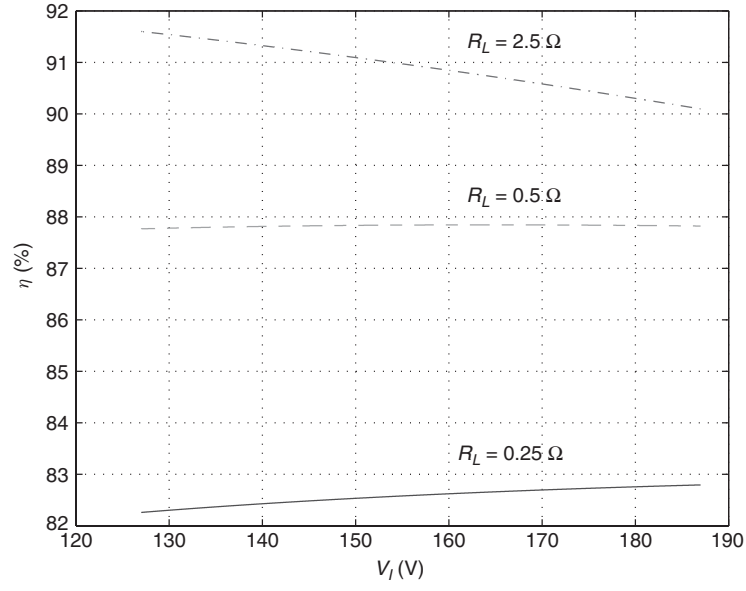


Figure 6.8 Efficiency η as a function of the dc input voltage V_I at $R_L = 0.25\,\Omega$, $0.5\,\Omega$, and $2.5\,\Omega$ for the forward converter in CCM.

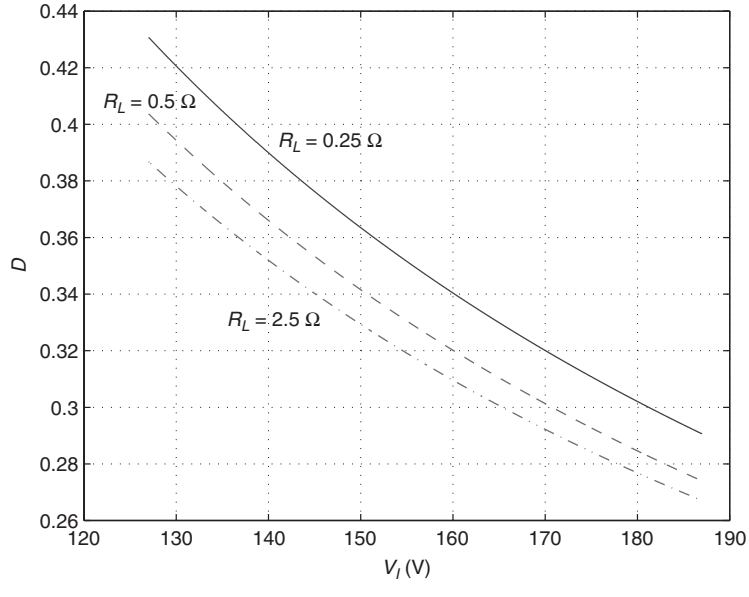


Figure 6.9 Duty cycle D as a function of the dc input voltage V_I for the forward converter at fixed load resistances R_L in CCM.

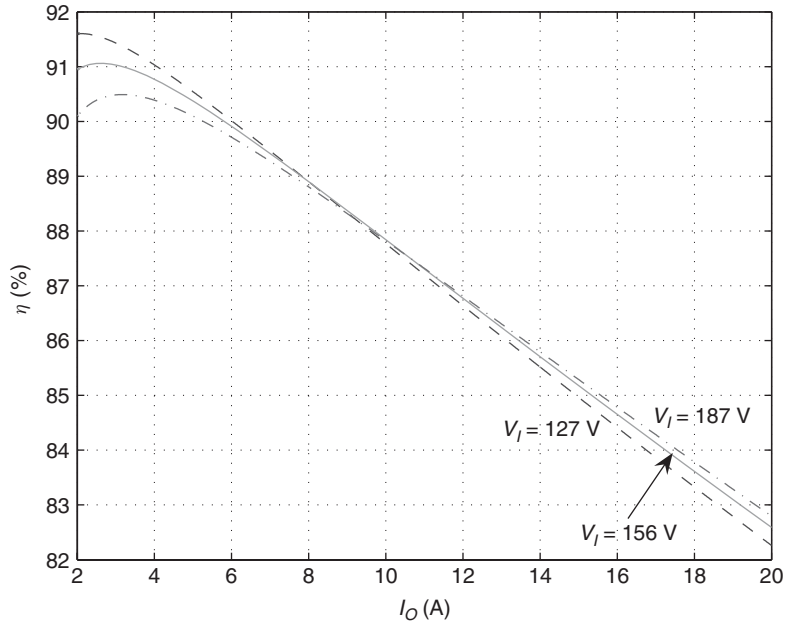


Figure 6.10 Efficiency η as a function of the dc load current I_O at $V_I = 127\,\text{V}$, $156\,\text{V}$, and $187\,\text{V}$ for the forward converter in CCM.

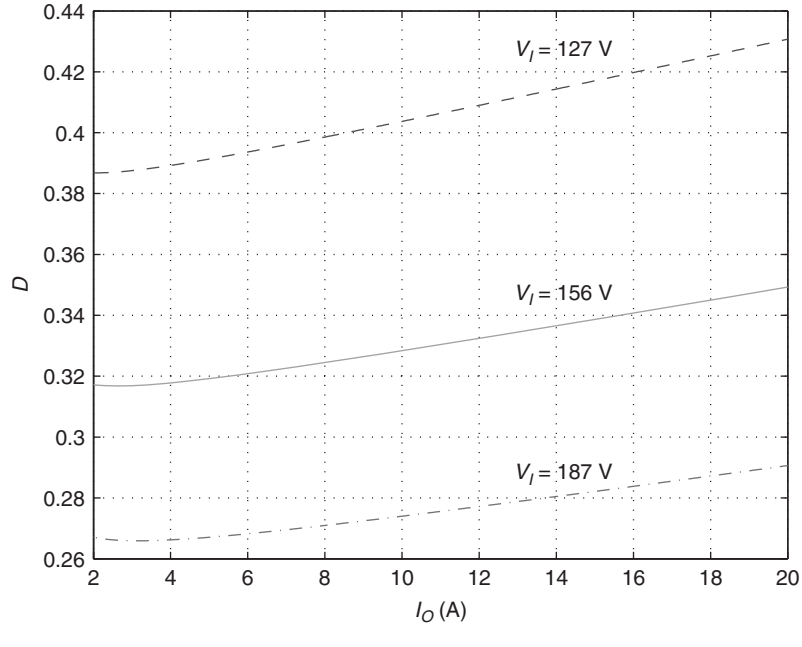


Figure 6.11 Duty cycle D as a function of the dc load current I_O at $V_I = 127\,\text{V}$, $156\,\text{V}$, and $187\,\text{V}$ for the forward converter in CCM.

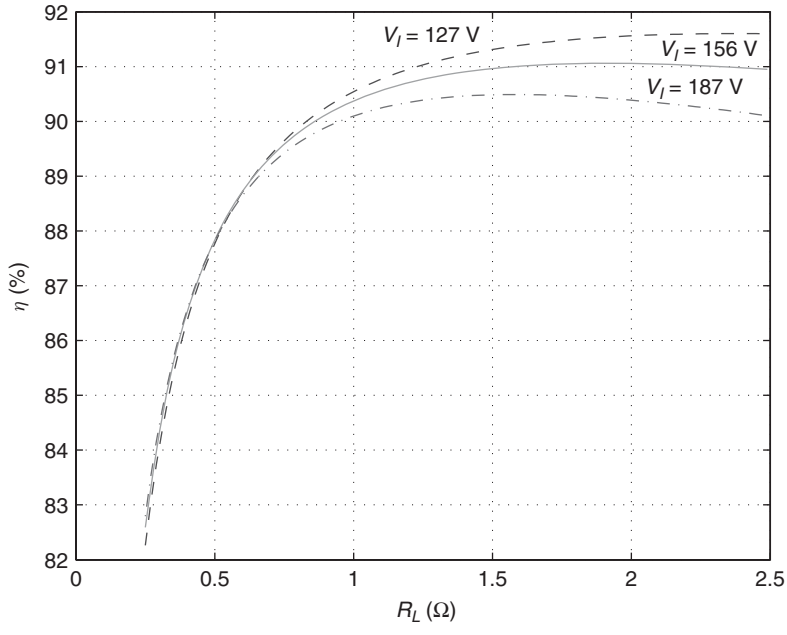


Figure 6.12 Efficiency η as a function of the load resistance R_L at $V_I = 127\,\text{V}$, 156 V, and 187 V for the forward converter in CCM.

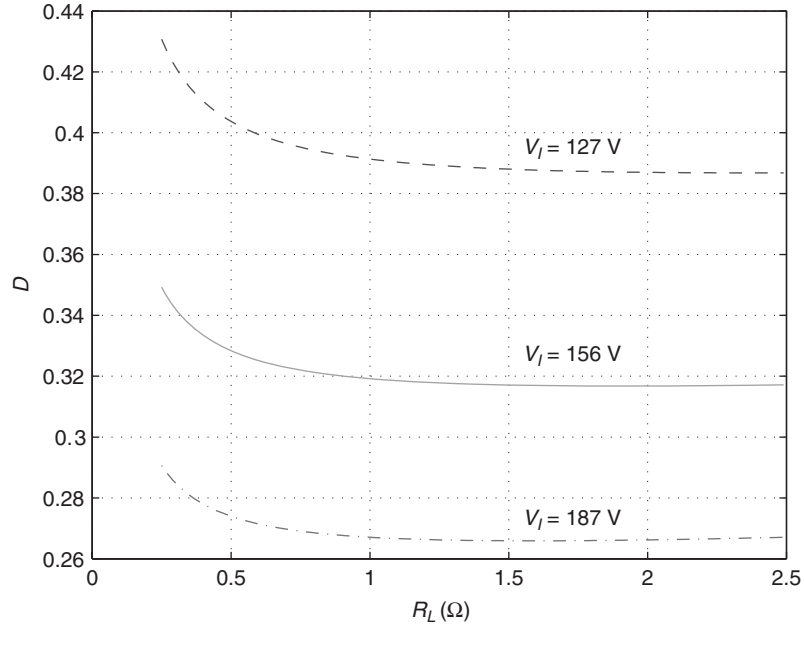


Figure 6.13 Duty cycle D as a function of the load resistance R_L at $V_I = 127\,\text{V}$, 156 V, and 187 V for the forward converter in CCM.

V_I decreases and I_O increases (or R_L decreases). The plots are similar to those of the buck converter.

6.3 DC Analysis of PWM Forward Converter for DCM

Figure 6.14 shows equivalent circuits for the PWM forward converter operating in DCM. Idealized current and voltage waveforms are depicted in Figure 6.15. At time $t = 0$, when the switch is turned on, the inductor current is zero. For the time interval $0 < t \le DT$, the switch and the diode D_1 are ON, and the diodes D_2 and D_3 are OFF as shown in Figure 6.14(a). The voltage across the primary is V_I and across the secondary is V_I/n_1. The voltage across the inductor is $V_I/n_1 - V_O$, causing the inductor current to increase linearly from zero.

At time $t = DT$, the switch is turned off, turning the diode D_1 off and the diodes D_2 and D_3 on. The equivalent circuit is shown in Figure 6.14(b) for the time interval $DT < t \le DT + t_m$. The voltage across the switch is V_I. The voltage across the inductor is $-V_O$, causing the inductor current to decrease linearly. The voltage across the magnetizing inductance is $v_{Lm} = -(n_1/n_3)V_I$. Therefore, the current through the magnetizing inductance and the diode D_3 decreases linearly. At time $t = DT + t_m$, these two currents reach zero and the diode D_3 turns off.

The equivalent circuit for the time interval $DT + t_m < t \le (D + D_1)T$ is shown in Figure 6.14(c). The voltage across the inductance L is $-V_O$ and therefore the current through this inductance and the diode D_2 decreases linearly. At time $t = (D + D_1)T$, the current through the inductor L and the diode D_2 reaches zero and the diode D_3 turns off. The inductor current remains zero until the switch is turned on at time $t = T$.

Figure 6.14(d) displays the equivalent circuit for the time interval $(D + D_1)T < t \le T$. The voltage across the inductor is zero because its current is zero. At time $t = T$, the switch is turned on and the inductor current begins to increase from zero.

6.3.1 Time Interval $0 < t \le DT$

During this time interval, the switch and the diode D_1 are ON, and the diodes D_2 and D_3 are OFF. The equivalent circuit is shown in Figure 6.14(a). The switch voltage v_S and the diode currents i_{D2} and i_{D3} are zero. The voltage across the primary and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = V_I = L_m \frac{di_{Lm}}{dt}, \quad i_{Lm}(0) = 0, \tag{6.148}$$

resulting in the current through the magnetizing inductance,

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt + 0 = \frac{1}{L_m}\int_0^t V_I\,dt = \frac{V_I}{L_m}t, \tag{6.149}$$

and the peak current of the magnetizing inductance,

$$\Delta i_{Lm} = i_{Lm}(DT) = \frac{V_I DT}{L_m} = \frac{DV_I}{f_s L_m}. \tag{6.150}$$

The voltage across the tertiary winding is

$$v_3 = -\frac{n_3}{n_1}v_1 = -\frac{n_3}{n_1}V_I, \tag{6.151}$$

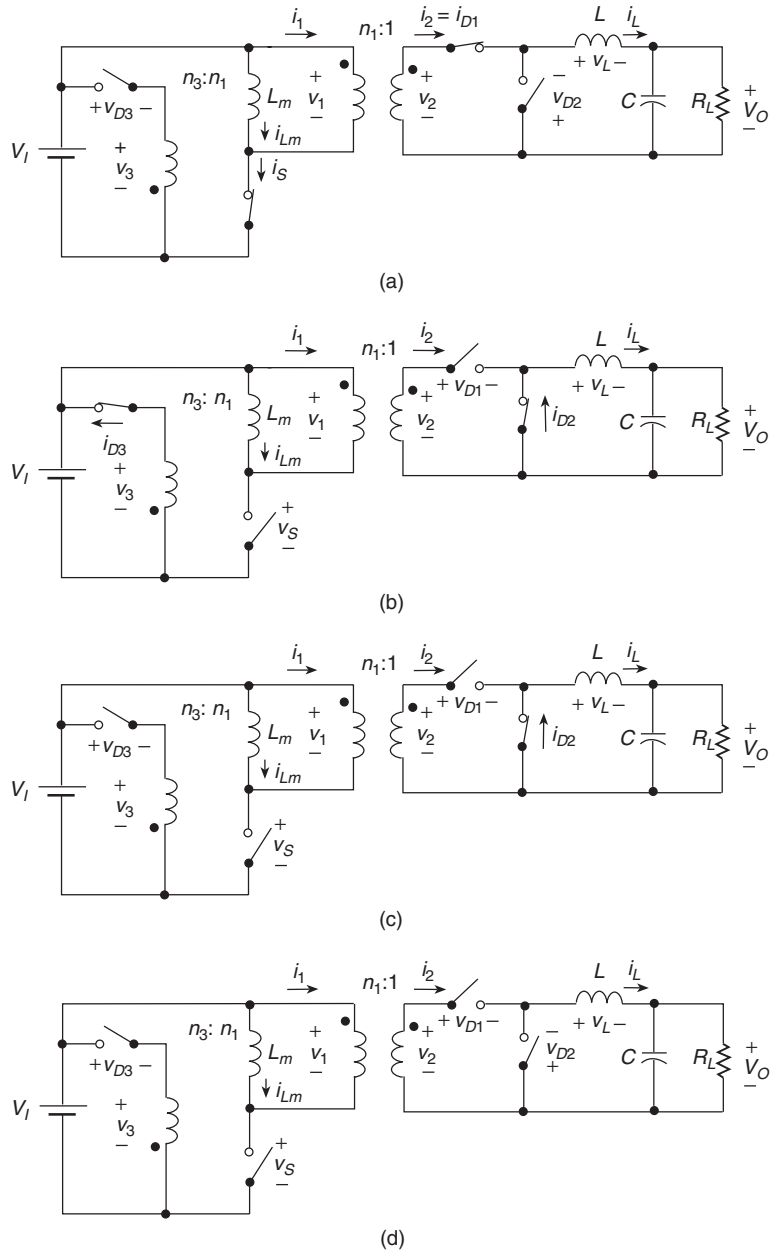


Figure 6.14 Equivalent circuits for different time intervals for the forward PWM converter operating in DCM. (a) For $0 < t \leq DT$. (b) For $DT < t \leq DT + t_m$. (c) For $DT + t_m < t \leq (D + D_1)T$. (d) For $(D + D_1)T < t \leq T$.

which gives the voltage across the diode D_3,

$$v_{D3} = v_3 - V_I = -V_I \left(\frac{n_3}{n_1} + 1 \right). \tag{6.152}$$

Since the voltage v_{D3} is negative, the diode D_3 is OFF.

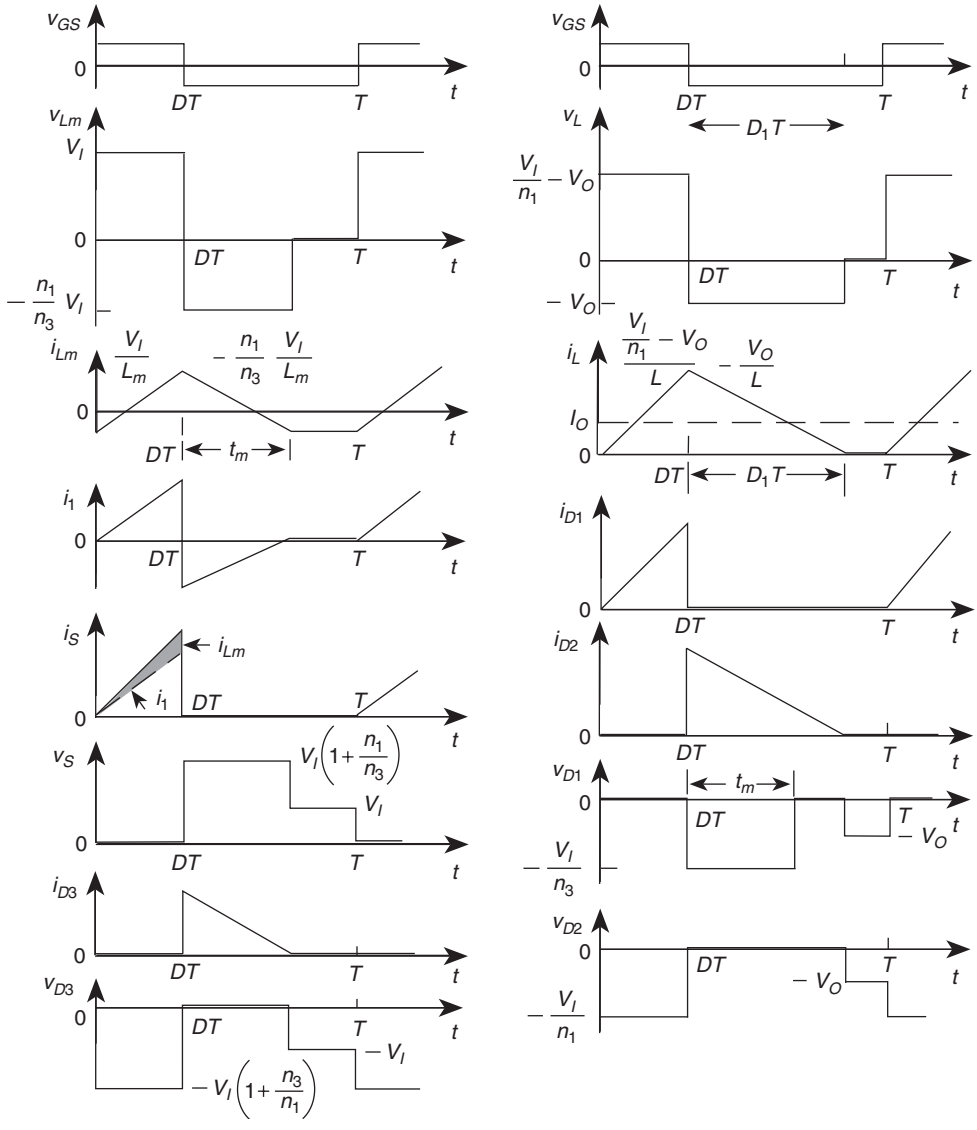


Figure 6.15 Waveforms in the PWM forward converter for DCM.

The voltage across the secondary is

$$v_2 = \frac{v_1}{n_1} = \frac{V_I}{n_1}, \tag{6.153}$$

and the voltage across the diode D_2 is

$$v_{D2} = -v_2 = -\frac{V_I}{n_1}, \tag{6.154}$$

which maintains this diode in the off-state.

The voltage across the inductor L is

$$v_L = \frac{V_I}{n_1} - V_O = L\frac{di_L}{dt}, \qquad i_L(0) = 0, \tag{6.155}$$

and the inductor and switch current is

$$i_2 = i_{D1} = i_L = \frac{1}{L}\int_0^t v_L\,dt = \frac{1}{L}\int_0^t \left(\frac{V_I}{n_1} - V_O\right) dt = \frac{\dfrac{V_I}{n_1} - V_O}{L}t, \tag{6.156}$$

resulting in the peak inductor current

$$\Delta i_L = i_L(DT) = \frac{\left(\dfrac{V_I}{n_1} - V_O\right)DT}{L} = \frac{\left(\dfrac{V_I}{n_1} - V_O\right)D}{f_s L}. \tag{6.157}$$

The current through the primary is

$$i_1 = \frac{i_2}{n_1} = \frac{\dfrac{V_I}{n_1} - V_O}{n_1 L}t, \tag{6.158}$$

yielding the current through the switch,

$$i_S = i_1 + i_{Lm} = \frac{\dfrac{V_I}{n_1} - V_O}{n_1 L}t + \frac{V_I}{L_m}t. \tag{6.159}$$

6.3.2 Time Interval $DT < t \le DT + t_m$

The equivalent circuit for this time interval is shown in Figure 6.14(b). The switch and the diode D_1 are OFF, and the diodes D_2 and D_3 are ON. The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{6.160}$$

resulting in the current through the inductor L and diode D_2,

$$i_{D2} = i_L = \frac{1}{L}\int_{DT}^t v_L\,dt + i_L(DT) = \frac{1}{L}\int_{DT}^t (-V_O)\,dt + i_L(DT)$$

$$= -\frac{V_O}{L}(t - DT) + i_L(DT) = -\frac{V_O}{L}(t - DT) + \frac{\left(\dfrac{V_I}{n_1} - V_O\right)DT}{L}. \tag{6.161}$$

The peak inductor current is found to be

$$\Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^{DT} (-V_O)\,dt = \frac{V_O D_1 T}{L}. \tag{6.162}$$

The voltage across the tertiary winding is

$$v_3 = V_I, \tag{6.163}$$

which gives the voltage across the primary and the magnetizing inductance

$$v_1 = v_{Lm} = -\frac{n_1}{n_3}v_3 = -\frac{n_1}{n_3}V_I = L_m\frac{di_{Lm}}{dt}, \tag{6.164}$$

the current through the magnetizing inductance,

$$i_{Lm} = \frac{1}{L_m}\int_{DT}^t v_{Lm}\,dt + i_{Lm}(DT) = -\frac{n_1 V_I}{n_3 L_m}(t - DT) + i_{Lm}(DT)$$

$$= -\frac{n_1 V_I}{n_3 L_m}(t - DT) + \frac{DV_I}{f_s L_m}, \tag{6.165}$$

the current through the primary,

$$i_1 = -i_{Lm} = \frac{n_1 V_I}{n_3 L_m}(t - DT) - i_{Lm}(DT), \tag{6.166}$$

and the current through the diode D_3,

$$i_{D3} = -\frac{n_1}{n_3} i_1 = -\frac{n_1^2 V_I}{n_3^2 L_m}(t - DT) + \frac{n_1}{n_3} i_{Lm}(DT). \tag{6.167}$$

The voltage across the secondary is

$$v_2 = -\frac{v_3}{n_3} = -\frac{V_I}{n_3}, \tag{6.168}$$

the voltage across the diode D_1 is

$$v_{D1} = -\frac{V_I}{n_3}, \tag{6.169}$$

and the voltage across the switch is

$$v_S = V_I - v_1 = V_I - \left(-\frac{n_1}{n_2} V_I\right) = V_I \left(\frac{n_1}{n_3} + 1\right). \tag{6.170}$$

This time interval ends when the current through the magnetizing inductance and therefore through the diode D_3 reaches zero.

6.3.3 Time Interval $DT + t_m < t \leq (D + D_1)T$

It is assumed that $t_m < D_1 T$. During this time interval, the switch and the diodes D_1 and D_3 are OFF, and the diode D_2 is ON. The equivalent circuit is shown in Figure 6.14(c). The voltages across the transformer windings and diodes D_1 and D_2 are $v_{Lm} = v_1 = v_2 = v_3 = v_{D1} = v_{D2} = 0$, the currents are $i_{Lm} = i_1 = i_2 = i_{D1} = i_3 = i_{D3} = 0$, the voltage across the diode D_3 is

$$v_{D3} = -V_I, \tag{6.171}$$

and the voltage across the switch is

$$v_S = V_I. \tag{6.172}$$

The inductor voltage and current waveforms are given by (6.160) and (6.161). This time interval is terminated when the current through the diode D_2 reaches zero.

6.3.4 Time Interval $(D + D_1)T < t \leq T$

During this time interval, the switch and all the diodes are OFF. The equivalent circuit is shown in Figure 6.14(d). The inductor current i_L, the inductor voltage v_L, the switch current i_S, and the diode currents i_{D1}, i_{D2}, and i_{D3} are zero. The voltage across the switch is

$$v_S = V_I, \tag{6.173}$$

the voltages across the diodes D_1 and D_2 are

$$v_{D1} = v_{D2} = -V_O, \tag{6.174}$$

and the voltage across the diode D_3 is

$$v_{D3} = -V_I. \tag{6.175}$$

This time interval ends when the switch is turned on by the driver.

6.3.5 DC Voltage Transfer Function for DCM

Referring to the inductor voltage waveform in Figure 6.15 and using the volt-second balance,

$$\left(\frac{V_I}{n_1} - V_O\right) DT = V_O D_1 T, \tag{6.176}$$

which gives the dc–dc voltage transfer function

$$M_{V\ DC} = \frac{V_O}{V_I} = \frac{D}{n_1(D + D_1)}. \tag{6.177}$$

From (6.157) and (6.177), the peak inductor current is

$$\Delta i_L = \frac{\left(\frac{V_I}{n_1} - V_O\right) DT}{L} = \frac{V_O D(1 - n_1 M_{V\ DC})}{n_1 M_{V\ DC} f_s L}. \tag{6.178}$$

The dc output current is equal to the average value of the inductor current and, from (6.177) and (6.178), can be expressed as

$$I_O = \frac{1}{T}\int_0^T i_L\, dt = \frac{(D + D_1)\Delta i_L}{2} = \frac{V_O D(D + D_1)(1 - n_1 M_{V\ DC})}{2 f_s L n_1 M_{V\ DC}}. \tag{6.179}$$

Using (6.177) and (6.178),

$$I_O = \frac{V_O D^2 (1 - n_1 M_{V\ DC})}{2 f_s L n_1^2 M_{V\ DC}^2} = \frac{V_O}{R_L}. \tag{6.180}$$

Solving for D gives

$$D = \sqrt{\frac{2 f_s L n_1^2 M_{V\ DC}^2}{R_L(1 - n_1 M_{V\ DC})}} = \sqrt{\frac{2 f_s L I_O n_1^2 M_{V\ DC}^2}{V_O(1 - n_1 M_{V\ DC})}}, \qquad \text{for } D \le 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}. \tag{6.181}$$

At the CCM/DCM boundary,

$$n_1 M_{V\ DCB} = D_B \tag{6.182}$$

as in CCM. Substitution of this into (6.181) yields the duty cycle D_B at the boundary,

$$D_B = 1 - \frac{2 f_s L}{R_L} = 1 - \frac{2 f_s L I_O}{V_O}. \tag{6.183}$$

Figures 6.16 and 6.17 respectively show plots of D versus normalized load current $I_O/(V_O/2 f_s L)$ and normalized load resistance $R_L/(2 f_s L)$ at various values of $n_1 M_{V\ DC}$ and $n_3 = n_1$ for the lossless forward converter.

From (6.181),

$$\frac{2 f_s L}{D^2 R_L} n_1^2 M_{V\ DC}^2 + n_1 M_{V\ DC} - 1 = 0, \tag{6.184}$$

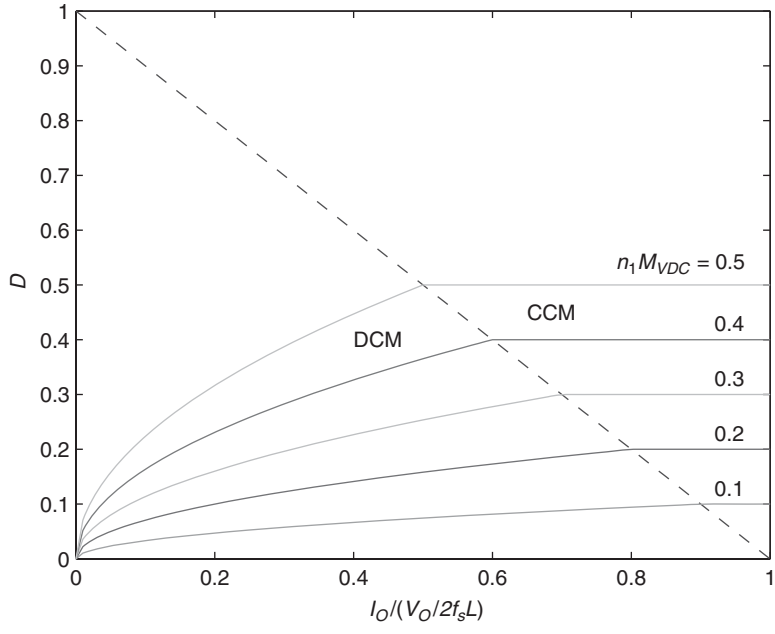


Figure 6.16 Duty cycle D as a function of $I_O/(V_O/2f_sL)$ at constant values of $n_1M_{V\ DC}$ and $n_3 = n_1$ for the lossless forward converter.

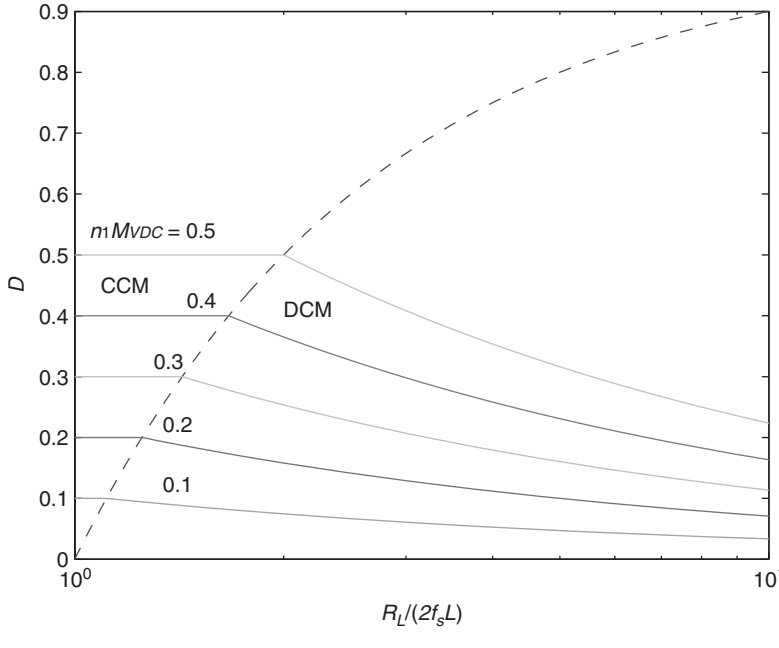


Figure 6.17 Duty cycle D as a function of $R_L/(2f_sL)$ at constant values of $n_1M_{V\ DC}$ and $n_3 = n_1$ for the lossless forward converter.

which yields the dc–dc voltage transfer function of the forward converter for DCM,

$$M_{V\ DC} = \frac{V_O}{V_I} = \frac{2}{n_1\left(1+\sqrt{1+\dfrac{8f_sL}{D^2R_L}}\right)}$$

$$= \frac{2}{n_1\left(1+\sqrt{1+\dfrac{8f_sLI_O}{D^2V_O}}\right)}, \quad \text{for } D \le 1-\frac{2f_sL}{R_L} = 1-\frac{2f_sLI_O}{V_O}. \quad (6.185)$$

It can be seen that $M_{V\ DC}$ depends on D, R_L, L, and f_s for DCM. Figures 6.18 and 6.19 respectively show plots of $n_1M_{V\ DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of D and $n_3 = n_1$ (i.e., $D_{MAX} = 0.5$) for the lossless forward converter.

From (6.177) and (6.185),

$$D_1 = D\left(\frac{1}{n_1M_{V\ DC}}-1\right) = \frac{D}{2}\left(\sqrt{1+\frac{8f_sL}{D^2R_L}}-1\right) = \frac{D}{2}\left(\sqrt{1+\frac{8f_sLI_O}{D^2V_O}}-1\right). \quad (6.186)$$

Neglecting the current through the magnetizing inductance i_{Lm}, that is, $i_{Lm} \ll i_1$, the converter input current i_I is equal to the current through the primary i_1 for $0 < t \le DT$,

$$i_I = i_1 + i_{Lm} \approx i_1 = \frac{i_2}{n_1} = \frac{\dfrac{V_I}{n_1}-V_O}{n_1L}t, \quad (6.187)$$

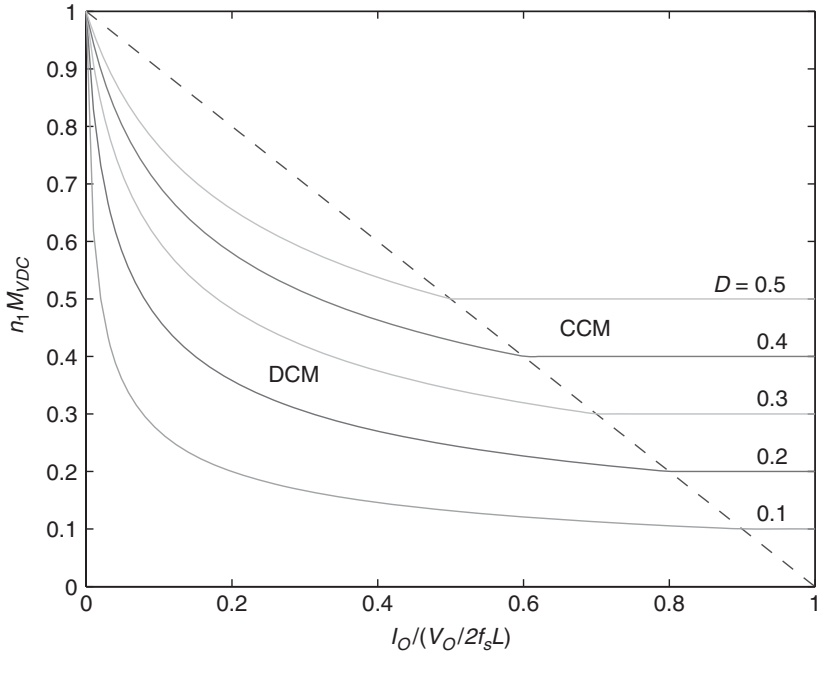


Figure 6.18 $n_1M_{V\ DC}$ as a function of $R_L/(2f_sL)$ at constant values of D for the lossless forward converter for $n_3 = n_1$.

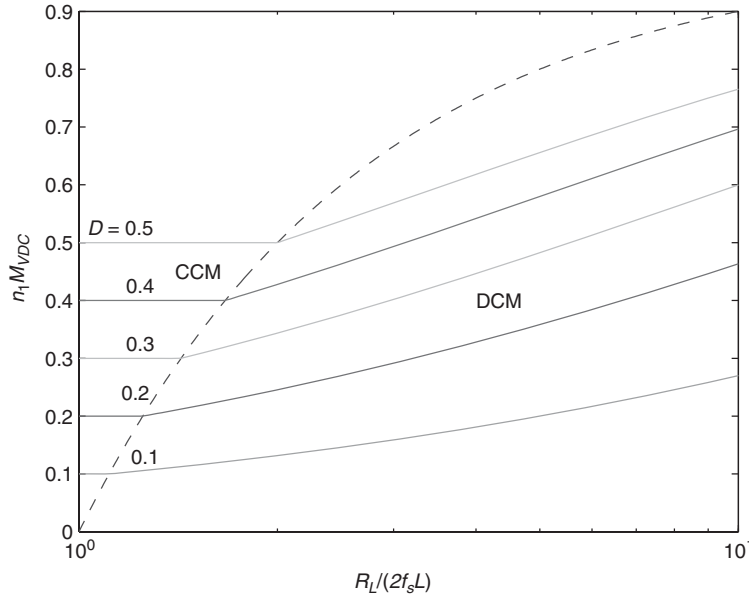


Figure 6.19 $n_1 M_{V\ DC}$ as a function of $R_L/(2f_sL)$ at constant values of D for the lossless forward converter for $n_3 = n_1$.

yielding the average value of the converter input current,

$$I_I = \frac{1}{T}\int_0^{DT} \frac{\frac{V_I}{n_1} - V_O}{n_1 L} t\, dt = \frac{D^2\left(\frac{V_I}{n_1} - V_O\right)}{2n_1 f_s L}, \tag{6.188}$$

and the dc input power,

$$P_I = V_I I_I = \frac{D^2 V_I\left(\frac{V_I}{n_1} - V_O\right)}{2n_1 f_s L}. \tag{6.189}$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{6.190}$$

The converter efficiency is

$$\eta = \frac{P_O}{P_I} = \frac{2f_s L n_1^2 M_{V\ DC}^2}{D^2 R_L(1 - n_1 M_{V\ DC})}. \tag{6.191}$$

Rearrangement of this equation gives the duty cycle of the lossy forward converter for DCM,

$$\begin{aligned} D &= \sqrt{\frac{2f_s L n_1^2 M_{V\ DC}^2}{\eta R_L(1 - n_1 M_{V\ DC})}} \\ &= \sqrt{\frac{2f_s L I_O n_1^2 M_{V\ DC}^2}{\eta V_O(1 - n_1 M_{V\ DC})}}, \qquad \text{for } D < 1 - \frac{2f_s L}{R_L} = 1 - \frac{2f_s L I_O}{V_O}, \end{aligned} \tag{6.192}$$

and the voltage transfer function

$$M_{V\ DC} = \frac{V_O}{V_I} = \frac{2}{n_1\left(1+\sqrt{1+\dfrac{8f_sL}{\eta D^2 R_L}}\right)}$$

$$= \frac{2}{n_1\left(1+\sqrt{1+\dfrac{8f_sLI_O}{\eta D^2 V_O}}\right)}, \quad \text{for } D < 1-\frac{2f_sL}{R_L} = 1-\frac{2f_sLI_O}{V_O}. \quad (6.193)$$

6.3.6 Maximum Inductance for DCM

The waveforms of the inductor current i_L at the CCM/DCM boundary at the minimum input voltage V_{Imin} and at the maximum input voltage V_{Imax} are depicted in Figure 6.20. The minimum value of the inductor peak current at the DCM/CCM boundary occurs at $D_B = D_{Bmax}$ and can be obtained from (6.19):

$$\Delta i_{Lmin} = \frac{V_O(1-D_{Bmax})}{f_s L_{max}}. \quad (6.194)$$

The dc output current I_{OB} at the CCM/DCM boundary is equal to the maximum load current I_{Omax} and is given by

$$I_{OB} = I_{Omax} = \frac{\Delta i_{Lmin}}{2} = \frac{V_O(1-D_{Bmax})}{2f_s L_{max}} = \frac{V_O}{R_{Lmin}}. \quad (6.195)$$

Thus, the maximum inductance required to maintain the converter operation in DCM is

$$L_{max} = \frac{R_{Lmin}(1-D_{Bmax})}{2f_s} = \frac{V_O(1-D_{Bmax})}{2f_s I_{Omax}}, \quad (6.196)$$

where

$$D_{Bmax} = \frac{n_1 M_{V\,DCmax}}{\eta} = \frac{n_1 V_O}{\eta V_{Imin}}. \quad (6.197)$$

6.3.7 Power Losses and Efficiency of Forward Converter for DCM

The peak inductor current is

$$\Delta i_L = V_O\sqrt{\frac{2(1-n_1 M_{V\ DC})}{f_s L R_L}}. \quad (6.198)$$

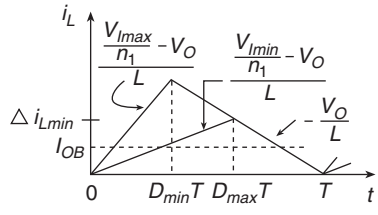


Figure 6.20 Waveforms of the inductor current at the boundary between DCM and CCM for V_{Imin} and V_{Imax}.

The rms switch current is

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2\, dt} = \frac{\Delta i_L}{n_1}\sqrt{\frac{D}{3}} = \frac{V_O}{n_1}\sqrt{\frac{2}{3R_L}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}}}, \quad (6.199)$$

resulting in MOSFET conduction power loss

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS}\Delta i_L^2}{3n_1^2} = \frac{2r_{DS}}{3n_1^2}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} P_O. \quad (6.200)$$

The switching loss is

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o V_O^2}{M_{V\ DC}^2} = \frac{f_s C_o R_L}{M_{V\ DC}^2} P_O. \quad (6.201)$$

The power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \left[\frac{2r_{DS}}{3n_1^2}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{2M_{V\ DC}^2}\right] P_O. \quad (6.202)$$

The power loss in the winding resistance of the primary is

$$P_{rT1} = r_{T1} I_{Srms}^2 = \frac{D r_{T1}\Delta i_L^2}{3n_1^2} = \frac{2r_{T1}}{3n_1^2}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} P_O. \quad (6.203)$$

The rms value of the current through diode D_1 is

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^{DT} i_{D1}^2\, dt} = \Delta i_L\sqrt{\frac{D}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}}}, \quad (6.204)$$

yielding the power loss in the forward resistance of D_1,

$$P_{RF1} = R_F I_{D1rms}^2 = \frac{R_F D\Delta i_L^2}{3} = \frac{2R_F}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} P_O. \quad (6.205)$$

The average current through diode D_1 is

$$I_{D1} = \frac{1}{T}\int_0^{DT} i_{D1}\, dt = I_O n_1 M_{V\ DC}, \quad (6.206)$$

resulting in the power loss in V_F of D_1,

$$P_{VF1} = V_F I_{D1} = n_1 M_{V\ DC} I_O V_F = \frac{n_1 M_{V\ DC} V_F}{V_O} P_O. \quad (6.207)$$

Hence, the power loss in diode D_1 is

$$P_{D1} = P_{VF1} + P_{RF1} = P_O\left[\frac{n_1 M_{V\ DC} V_F}{V_O} + \frac{2R_F}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}}\right]. \quad (6.208)$$

The power loss in the winding resistance of the secondary is

$$P_{rT2} = r_{T2} I_{D1rms}^2 = \frac{r_{T2} D\Delta i_L^2}{3} = \frac{2r_{T2}}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} P_O. \quad (6.209)$$

The winding power loss in both primary and secondary is given by

$$P_{rT} = P_{rT1} + P_{rT2} = \left(\frac{r_{T1}}{n_1^2} + r_{T2}\right)\frac{2}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}}P_O. \tag{6.210}$$

The rms value of the current through the diode D_2 is

$$I_{D2rms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} i_{D2}^2\, dt} = \Delta i_L\sqrt{\frac{D_1}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2(1 - n_1 M_{V\ DC})^3}{f_s L R_L}}}, \tag{6.211}$$

yielding the power loss in R_F of D_2,

$$P_{RF2} = R_F I_{D2rms} = \frac{D_1 R_F \Delta i_L^2}{3} = \frac{2R_F}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})^3}{f_s L R_L}}P_O. \tag{6.212}$$

The average current through diode D_2 is

$$I_{D2} = \frac{1}{T}\int_0^T i_{D2}\, dt = \frac{D^2 V_O}{2f_s L}\left(\frac{1}{M_{V\ DC}} - 1\right)^2 = I_O(1 - n_1 M_{V\ DC}), \tag{6.213}$$

which leads to the power loss in V_F of diode D_2,

$$P_{VF2} = V_F I_{D2} = V_F I_O(1 - n_1 M_{V\ DC}) = \frac{V_F(1 - n_1 M_{V\ DC})}{V_O}P_O. \tag{6.214}$$

Hence, the conduction power loss in diode D_2 is

$$P_{D2} = P_{VF2} + P_{RF2} = \left[\frac{V_F(1 - n_1 M_{V\ DC})}{V_O} + \frac{2R_F}{3}\sqrt{\frac{2(1 - M_{V\ DC})^3}{f_s L R_L}}\right]P_O. \tag{6.215}$$

The rms value of the inductor current is

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^{(D+D_1)T} i_L^2\, dt} = \Delta i_L\sqrt{\frac{D + D_1}{3}} = V_O\sqrt{\frac{2}{3R_L}\sqrt{\frac{2(1 - n_1 M_{V\ DC})}{f_s L R_L}}}, \tag{6.216}$$

yielding the power loss in the inductor winding,

$$P_{rL} = r_L I_{Lrmas}^2 = \frac{r_L \Delta i_L^2(D + D_1)}{3} = \frac{2r_L}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})}{f_s L R_L}}P_O. \tag{6.217}$$

The total converter power loss is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_{D1} + P_{D2} + P_{rL} + P_{rT1} + P_{rT2} \\ &= \left[\left(\frac{r_{DS} + r_{T1}}{n_1^2} + R_F + r_{T2}\right)\frac{2}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{M_{V\ DC}^2}\right. \\ &\quad \left. + \frac{2R_F}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})^3}{f_s L R_L}} + \frac{V_F}{V_O} + \frac{2r_L}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})}{f_s L R_L}}\right]P_O. \end{aligned} \tag{6.218}$$

The efficiency of the forward converter for DCM is given by

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}$$

$$= \left[1 + \left(\frac{r_{DS} + r_{T1}}{n_1^2} + R_F + r_{T2}\right)\frac{2}{3}\sqrt{\frac{2n_1^2 M_{V\ DC}^2(1 - n_1 M_{V\ DC})}{f_s L R_L}} + \frac{f_s C_o R_L}{M_{V\ DC}^2}\right.$$
$$\left. + \frac{2R_F}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})^3}{f_s L R_L}} + \frac{V_F}{V_O} + \frac{2r_L}{3}\sqrt{\frac{2(1 - n_1 M_{V\ DC})}{f_s L R_L}}\right]^{-1}. \quad (6.219)$$

6.3.8 Design of Forward Converter for DCM

Design a universal PWM forward converter operating in DCM to meet the following specifications: $V_O = 5\,\text{V}$, $I_{Omin} = 0\,\text{A}$, $I_{Omax} = 20\,\text{A}$, $V_r/V_O \leq 10\,\%$, and the input voltage is the single-phase utility line rectified voltage anywhere in the world whose rms voltage is in the range from 85 to 264 Vrms.

Solution. The minimum and maximum values of the dc input voltage are

$$V_{Imin} = \sqrt{2} \times V_{rms(min)} = \sqrt{2} \times 85 = 120\,\text{V} \quad (6.220)$$

and

$$V_{Imax} = \sqrt{2} \times V_{rms(max)} = \sqrt{2} \times 264 = 373\,\text{V}. \quad (6.221)$$

The minimum and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{5}{373} = 0.0134 = \frac{1}{74.6} \quad (6.222)$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{5}{120} = 0.04167 = \frac{1}{24}. \quad (6.223)$$

The maximum value of the dc output power is

$$P_{Omax} = V_O I_{Omax} = 5 \times 20 = 100\,\text{W}. \quad (6.224)$$

The minimum load resistance is

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{5}{20} = 0.25\,\Omega. \quad (6.225)$$

Let us assume the switching frequency is $f_s = 100\,\text{kHz}$, the converter efficiency $\eta = 80\,\%$, and $D_{max} \approx 0.4$. In this case, the transformer turns ratio is

$$n_1 = \frac{\eta D_{max}}{M_{V\,DCmax}} = \frac{0.8 \times 0.4}{0.04167} = 7.679. \quad (6.226)$$

Pick $n_1 = n_3 = 8$. The maximum permissible duty cycle is

$$D_{MAX} = \frac{1}{\frac{n_3}{n_1} + 1} = \frac{1}{1 + 1} = 0.5. \quad (6.227)$$

Thus, $D_{max} < D_{MAX}$.

The minimum and maximum values of the duty cycle at the CCM/DCM boundary are

$$D_{Bmin} = \frac{n_1 M_{V\,DCmin}}{\eta} = \frac{8 \times 0.0134}{0.8} = 0.134 \quad (6.228)$$

and

$$D_{Bmax} = \frac{n_1 M_{V\,DCmax}}{\eta} = \frac{8 \times 0.04167}{0.8} = 0.4167. \tag{6.229}$$

Hence, $t_{m(max)}/T = D_{max} = 0.4167$.

The maximum inductance is

$$L_{max} = \frac{R_{Lmin}(1 - D_{Bmax})}{2f_s} = \frac{0.25 \times (1 - 0.4167)}{2 \times 10^5} = 0.729\,\mu\text{H}. \tag{6.230}$$

Pick a standard inductance $L = 0.56\,\mu$H.

The maximum duty cycle at R_{Lmin} is

$$D_{max} = \sqrt{\frac{2f_s L n_1^2 M_{V\,DCmax}^2}{\eta(1 - n_1 M_{V\,DCmax})R_{Lmin}}} = \sqrt{\frac{2 \times 10^5 \times 0.56 \times 10^{-6} \times 8^2 \times 0.04167^2}{0.8 \times (1 - 8 \times 0.04167) \times 0.25}} = 0.3055, \tag{6.231}$$

resulting in

$$D_{1min} = D_{max}\left(\frac{1}{n_1 M_{V\,DCmax}} - 1\right) = 0.3055\left(\frac{1}{8 \times 0.04167} - 1\right) = 0.6109 \tag{6.232}$$

and, hence,

$$D_{max} + D_{1min} = 0.3055 + 0.6109 = 0.9164 < 1. \tag{6.233}$$

The minimum duty cycle at R_{Lmin} is

$$D_{min} = \sqrt{\frac{2f_s L n_1^2 M_{V\,DCmin}^2}{\eta(1 - n_1 M_{V\,DCmin})R_{Lmin}}} = \sqrt{\frac{2 \times 10^5 \times 0.56 \times 10^{-6} \times 8^2 \times 0.0134^2}{0.8 \times (1 - 8 \times 0.0134) \times 0.25}} = 0.0849, \tag{6.234}$$

which gives

$$D_{1max} = D_{min}\left(\frac{1}{n_1 M_{V\,DCmin}} - 1\right) = 0.0849\left(\frac{1}{8 \times 0.0134} - 1\right) = 0.707 \tag{6.235}$$

and

$$D_{min} + D_{1max} = 0.0134 + 0.707 = 0.7204 < 1. \tag{6.236}$$

The maximum inductor current is

$$\Delta i_{Lmax} = \frac{\left(\frac{V_{Imax}}{n_1} - V_O\right) D_{min}}{f_s L} = \frac{\left(\frac{373}{8} - 5\right) 0.0849}{10^5 \times 0.56 \times 10^{-6}} = 63.106\,\text{A}. \tag{6.237}$$

The ripple voltage is

$$V_r = 0.1 \times V_O = 0.1 \times 5 = 500\,\text{mV}. \tag{6.238}$$

The maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{500}{63.106} = 7.92\,\text{m}\Omega. \tag{6.239}$$

Let $r_C = 7\,\text{m}\Omega$. Thus, the filter capacitance is

$$C_{min} = \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{1 - D_{min}}{2f_s r_C}\right\} = \max\left\{\frac{0.3055}{2f_s r_C}, \frac{1 - 0.0849}{2f_s r_C}\right\} = \frac{1 - D_{min}}{2f_s r_C} = \frac{1 - 0.0849}{2 \times 10^5 \times 0.007} = 653.64\,\mu F. \tag{6.240}$$

Pick $C = 1\,\text{mF}/16\,\text{V}/7\,\text{m}\Omega$.

The current and voltage stresses of the rectifier diodes are

$$I_{D1Mmax} = I_{D2Mmax} = \Delta i_{Lmax} = 63.106\,\text{A}, \tag{6.241}$$

$$V_{D1Mmax} = \frac{V_{Imax}}{n_3} = \frac{373}{8} = 46.625\,\text{V}, \tag{6.242}$$

and

$$V_{D2Mmax} = \frac{V_{Imax}}{n_1} = \frac{373}{8} = 46.625\,\text{V}. \tag{6.243}$$

The maximum peak current through the primary of the ideal transformer

$$I_{1max} = \frac{I_{D1Mmax}}{n_1} = \frac{63.106}{8} = 7.888\,\text{A} \tag{6.244}$$

and the maximum peak current through the magnetizing inductance is

$$\Delta i_{Lm(max)} = 0.1 I_{1max} = 0.1 \times 7.888 = 0.7888\,\text{A} \tag{6.245}$$

producing the minimum magnetizing inductance

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{f_s \Delta i_{Lm(max)}} = \frac{0.0849 \times 373}{10^5 \times 0.7888} = 0.4\,\text{mH}. \tag{6.246}$$

The current and voltage stresses of the switch are

$$I_{SMmax} = I_{1max} + \Delta i_{Lm(max)} = 7.888 + 0.7888 = 8.6768\,\text{A} \tag{6.247}$$

and

$$V_{SMmax} = \left(\frac{n_1}{n_3} + 1\right) V_{Imax} = 2V_{Imax} = 2 \times 373 = 746\,\text{V}. \tag{6.248}$$

The current and voltage stresses of diode D_3 are

$$I_{D3Mmax} = \left(\frac{n_3}{n_1}\right) \Delta i_{Lm(max)} = 0.7888\,\text{A} \tag{6.249}$$

and

$$V_{D3Mmax} = \left(\frac{n_3}{n_1} + 1\right) V_{Imax} = 2V_{Imax} = 2 \times 373 = 746\,\text{V}. \tag{6.250}$$

An International Rectifier IRF740 power MOSFET is selected, which has $V_{DSS} = 400\,\text{V}$, $I_{SM} = 10\,\text{A}$, $r_{DS} = 0.55\,\Omega$, $Q_{g(typ)} = 41\,\text{nC}$, $Q_{gmax} = 60\,\text{nC}$, and $C_o = 100\,\text{pF}$. Two MBR2540 Schottky barrier diodes are chosen, each having $I_{DM} = 25\,\text{A}$, $V_{DM} = 40\,\text{V}$, $V_F = 0.3\,\text{V}$, and $R_F = 16\,\text{m}\Omega$. A fast recovery MR826 diode is selected with $V_{DM} = 600\,\text{V}$ and $I_{DM(AV)} = 5\,\text{A}$.

The power losses will be calculated for full load $R_{Lmin} = 0.25\,\Omega$ and the maximum input voltage $V_{Imax} = 373\,\text{V}$. The MOSFET conduction power loss is

$$\begin{aligned} P_{rDS} &= \frac{2r_{DS}}{3n_1^2}\sqrt{\frac{2n_1^2 M_{V\,DCmin}^2 (1 - n_1 M_{V\,DCmin})}{f_s L R_{Lmin}}} P_{Omax} \\ &= \frac{2 \times 0.55}{3 \times 8^2}\sqrt{\frac{2 \times 8^2 \times 0.0134^2 (1 - 8 \times 0.0134)}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 0.694\,\text{W}. \end{aligned} \tag{6.251}$$

The switching loss is

$$P_{sw} = f_s C_o V_{Imax}^2 = 10^5 \times 100 \times 10^{-12} \times 373^2 = 1.391\,\text{W}. \tag{6.252}$$

The power loss in the MOSFET is

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = 0.694 + \frac{1.391}{2} = 1.39\,\text{W}. \tag{6.253}$$

Assuming $r_{T1} = 0.05\,\Omega$, the power loss in the winding resistance of the primary is given by

$$P_{rT1} = \frac{2r_{T1}}{3n_1^2}\sqrt{\frac{2n_1^2 M_{V\,DCmin}^2(1 - n_1 M_{V\,DCmin})}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.05}{3 \times 8^2}\sqrt{\frac{2 \times 8^2 \times 0.0134^2(1 - 8 \times 0.0134)}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 0.063\,\text{W}. \tag{6.254}$$

The power loss in the forward resistance of diode D_1 is

$$P_{RF1} = \frac{2R_F}{3}\sqrt{\frac{2n_1^2 M_{V\,DCmin}^2(1 - n_1 M_{V\,DCmin})}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.016}{3}\sqrt{\frac{2 \times 8^2 \times 0.0134^2(1 - 8 \times 0.0134)}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 1.291\,\text{W}, \tag{6.255}$$

and the power loss in V_F of diode D_1 is

$$P_{VF1} = n_1 M_{V\,DCmin} I_{Omax} V_F = 8 \times 0.0134 \times 20 \times 0.3 = 0.643\,\text{W}, \tag{6.256}$$

resulting the conduction loss in diode D_1

$$P_{D1} = P_{RF1} + P_{VF1} = 1.291 + 0.643 = 1.934\,\text{W}. \tag{6.257}$$

Assuming $r_{T2} = 0.01\,\Omega$, the power loss in the winding resistance of the secondary is

$$P_{rT2} = \frac{2r_{T2}}{3}\sqrt{\frac{2n_1^2 M_{V\,DCmin}^2(1 - n_1 M_{V\,DCmin})}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.01}{3}\sqrt{\frac{2 \times 8^2 \times 0.0134^2(1 - 8 \times 0.0134)}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 0.807\,\text{W}. \tag{6.258}$$

The winding power loss in both primary and secondary is given by

$$P_{rT} = P_{rT1} + P_{rT2} = 0.063 + 0.807 = 0.87\,\text{W}. \tag{6.259}$$

The power loss in the forward resistance R_F of D_2 is

$$P_{RF2} = \frac{2R_F}{3}\sqrt{\frac{2(1 - n_1 M_{V\,DCmin})^3}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.016}{3}\sqrt{\frac{2(1 - 8 \times 0.0134)^3}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 10.76\,\text{W}. \tag{6.260}$$

The power loss in V_F of diode D_2 is

$$P_{VF2} = V_F I_{Omax}(1 - n_1 M_{V\,DCmin}) = 0.3 \times 20 \times (1 - 8 \times 0.0134) = 5.357\,\text{W}. \tag{6.261}$$

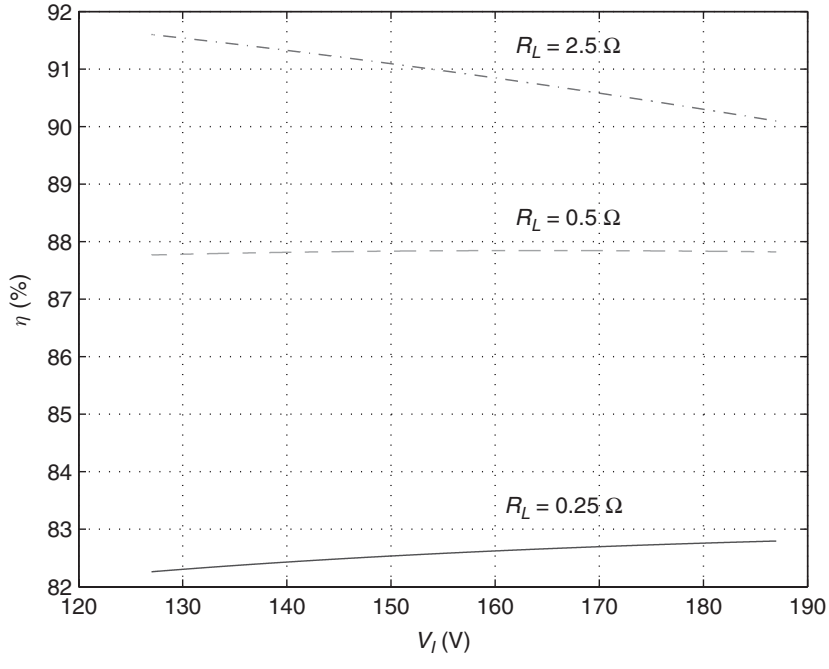


Figure 6.21 Efficiency η as a function of the dc input voltage V_I at various load resistances R_L for the forward converter in DCM.

Hence, the conduction power loss in diode D_2 is

$$P_{D2} = P_{VF2} + P_{RF2} = 5.357 + 10.76 = 16.12\,\text{W}. \tag{6.262}$$

Assuming $r_L = 0.015\,\Omega$, the power loss in the inductor winding resistance is

$$P_{rL} = \frac{2r_L}{3}\sqrt{\frac{2(1 - n_1 M_{V\,DCmin})}{f_s L R_{Lmin}}}P_{Omax}$$

$$= \frac{2 \times 0.015}{3}\sqrt{\frac{2(1 - 8 \times 0.0134)}{10^5 \times 0.56 \times 10^{-6} \times 0.25}} \times 100 = 11.29\,\text{W}. \tag{6.263}$$

The total converter power loss is

$$P_{LS} = P_{rDS} + P_{sw} + P_{D1} + P_{D2} + P_{rL} + P_{rT}$$

$$= 0.694 + 1.316 + 1.934 + 16.12 + 11.29 + 0.87 = 32.379\,\text{W}. \tag{6.264}$$

The efficiency of the forward converter is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{100}{100 + 32.379} = 75.54\,\%. \tag{6.265}$$

Figures 6.21–6.26 show the characteristics of the converter designed. The lowest efficiency η occurs at I_{Omax} and V_{Imax}. The duty cycle D decreases as V_I increases and I_O decreases (or R_L increases).

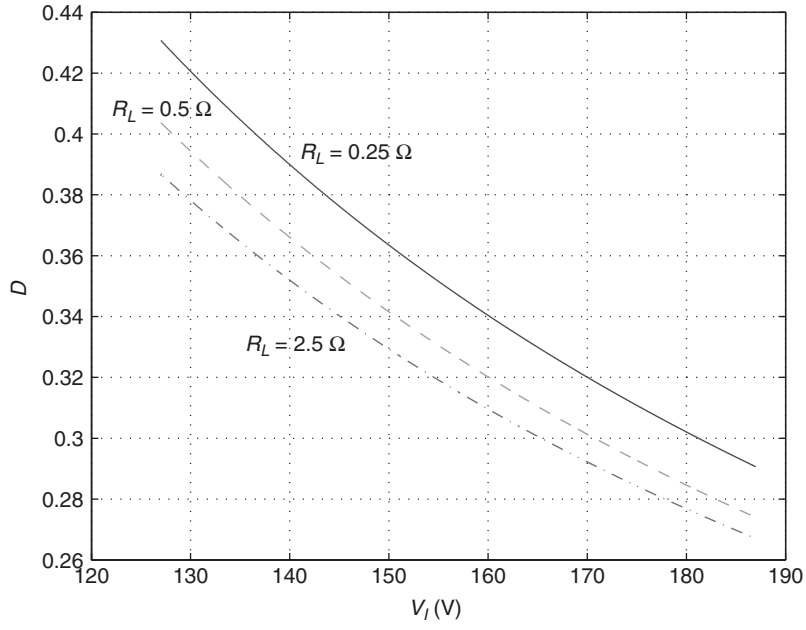


Figure 6.22 Duty cycle D as a function of the dc input voltage V_I at various load resistances R_L for the forward converter in DCM.

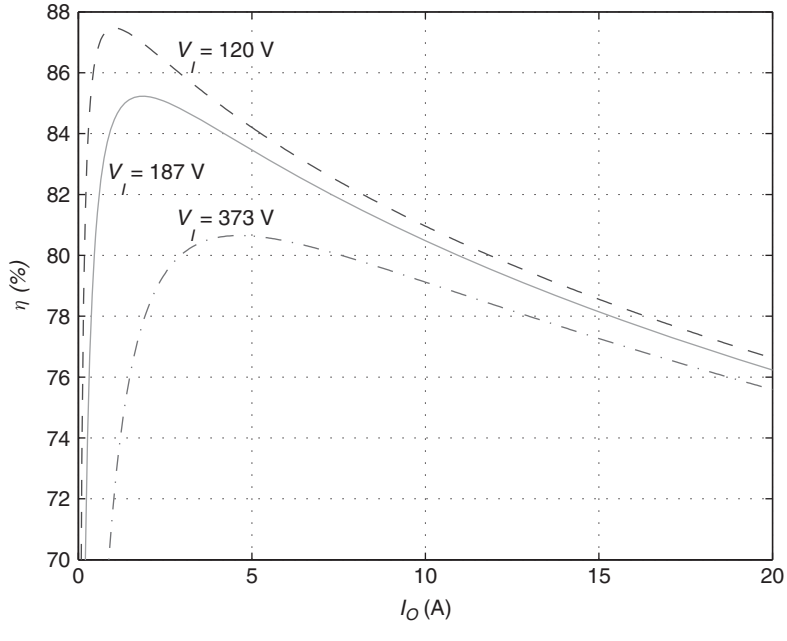


Figure 6.23 Efficiency η as a function of the dc load current I_O at various dc input voltages V_I for the forward converter in DCM.

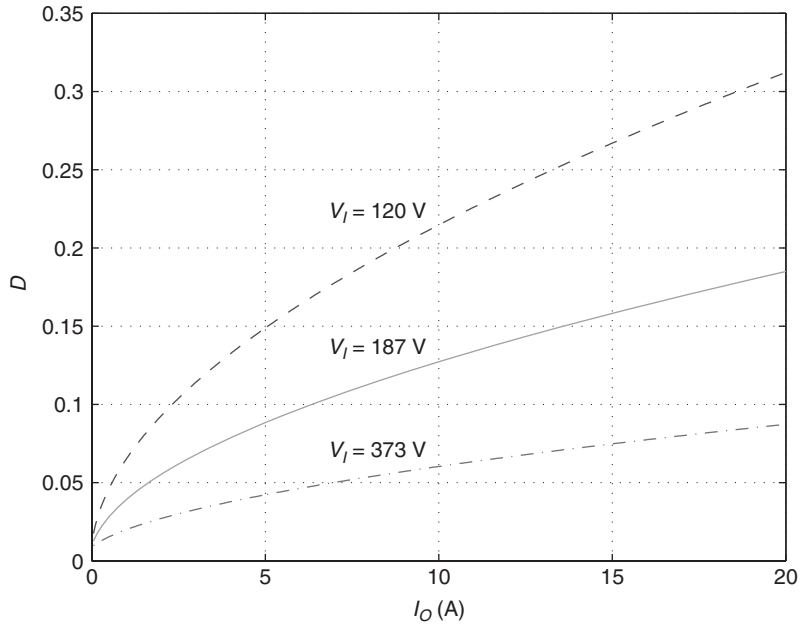


Figure 6.24 Duty cycle D as a function of the dc load current I_O at various dc input voltages V_I for the forward converter in DCM.

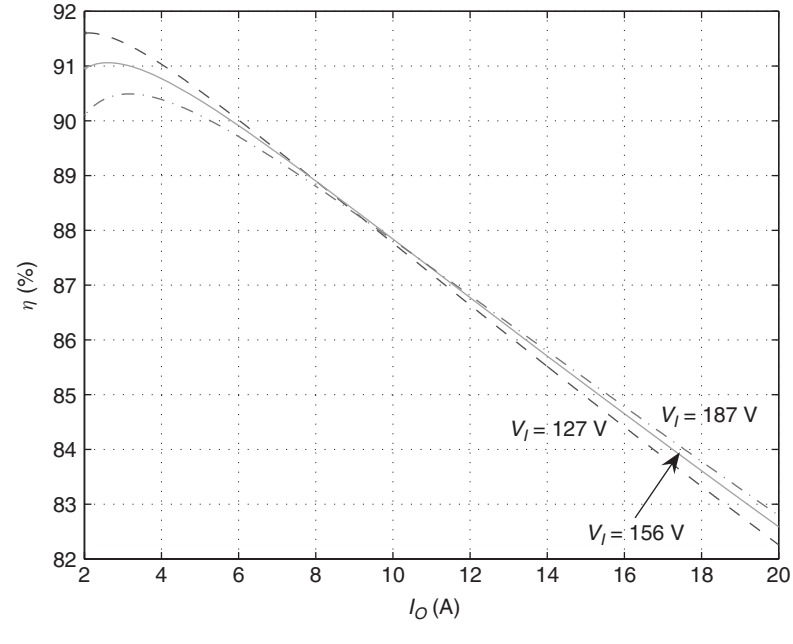


Figure 6.25 Efficiency η as a function of the load resistance R_L at various dc input voltages V_I for the forward converter in DCM.

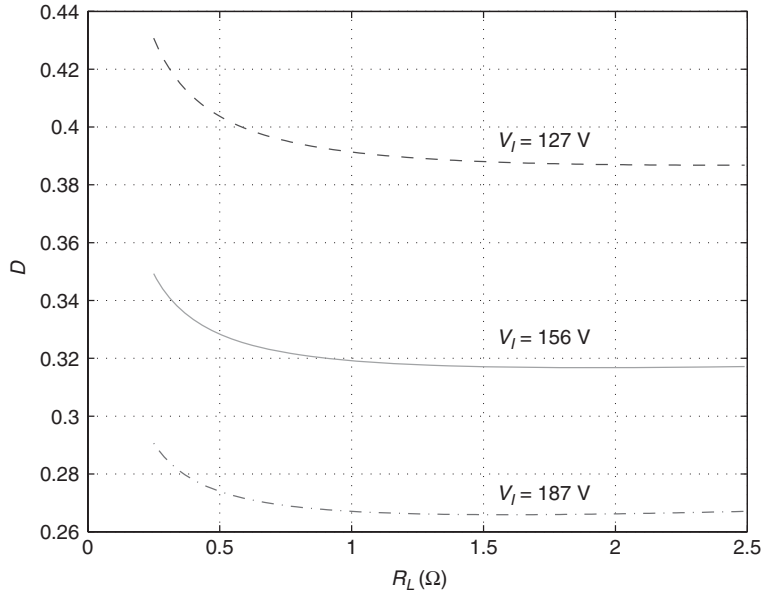


Figure 6.26 Duty cycle D as a function of the load resistance R_L at various dc input voltages V_I for the forward converter in DCM.

6.4 Multiple-output Forward Converter

Figure 6.27 shows a two-output forward converter. In order to obtain the second output, the transformer has an extra secondary winding, which drives an additional rectifier composed of two diodes, an inductor, and a filter capacitor. More outputs can be obtained by adding more secondaries, rectifiers, and low-pass filters. Usually, only one output is controlled and other outputs are not regulated. If the dc input voltage V_I is increased, the duty cycle D is decreased by the feedback network of the controlled output. Nearly the same decrease in D is also required by the unregulated outputs, maintaining the output voltages close the required values. However, the load resistances may change in the opposite direction to that of the regulated output, causing variations of the output voltages. This is especially true for DCM operation, in which the output voltage is heavily dependent on the load resistance. Interactions between multiple outputs are referred to as *cross-regulation*.

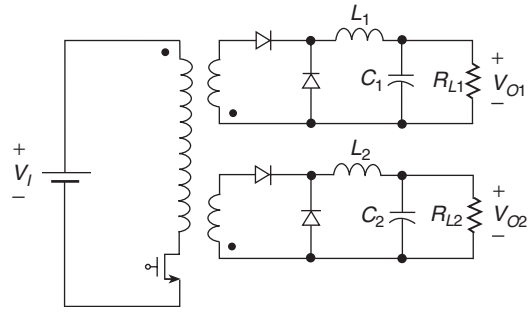


Figure 6.27 Multiple-output forward converter.

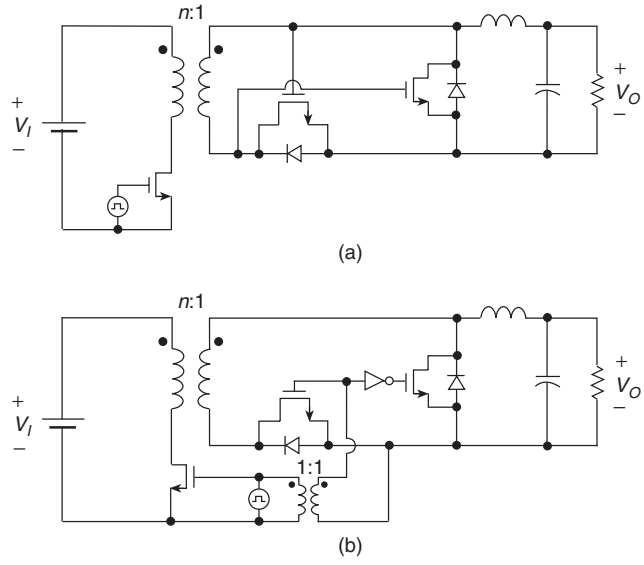


Figure 6.28 Forward converters with synchronous rectifier. (a) With self-driven MOSFETs. (b) With IC driver of all MOSFETs.

6.5 Forward Converter with Synchronous Rectifier

Synchronous rectifiers are attractive in low output voltage applications (e.g., 1.8 or 3.3 V), where Schottky diodes may be replaced by low on-resistance MOSFETs, as shown in Figure 6.28. In the self-driven architecture shown in Figure 6.28(a), the MOSFETs are driven by the transformer output voltage. The transistor gates are connected to the opposite ends of the secondary winding, and the gate of each device is connected to the drain of another device. The rectifier MOSFETs are automatically synchronized to the main switch. The benefits of this topology are simplicity and low parts count. In the circuit of Figure 6.28(b), the MOSFETs are driven by an IC driver, which is normally a part of an IC control circuit. The transformer in the driver and the transformer in the power stage ensure dc isolation between the converter input and the output. Unlike diodes, MOSFETs do not have offset voltages. Low-voltage MOSFETs exhibit very low on-resistances (e.g., 5 mΩ), yielding low conduction loss and high efficiency. Since MOSFETs can conduct current in both directions, the transformer reset circuit is not needed. A converter with a synchronous rectifier may operate only in CCM.

6.6 Forward Converters with Active Clamping

A forward converter with three active clamping and core reset circuits is shown in Figure 6.29 [19]. The clamping circuit of Figure 6.29(a) is connected across the transformer primary. The main transistor Q_1 is driven with the duty cycle D and the clamp transistor is driven with the duty cycle $1 - D$. This circuit is called the high-end n-channel active clamp. The MOSFET Q_2 carries only the transformer magnetizing current, which has a small peak value compared to the reflected load current. Therefore, Q_2 may have a much lower current rating than that of Q_1. A dead time is required between the time Q_1

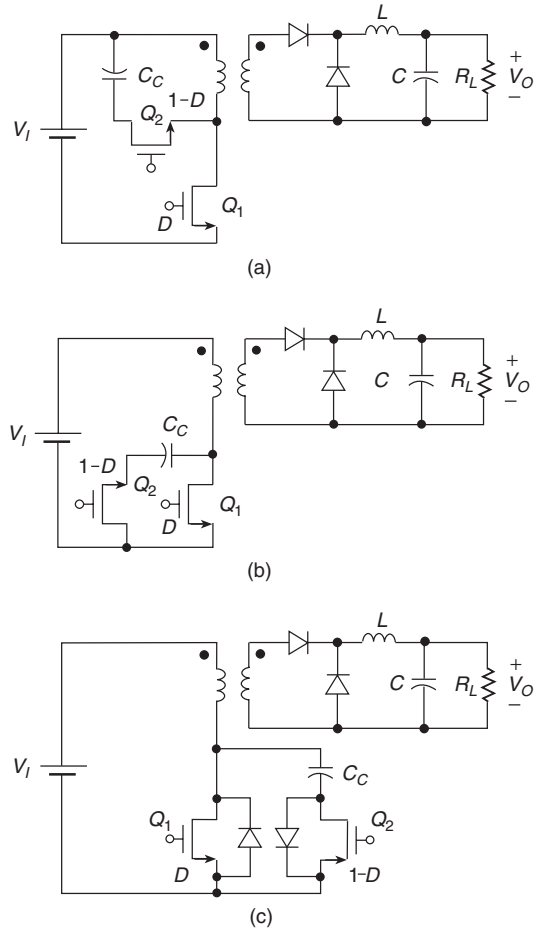


Figure 6.29 Forward converters with active clamping. (a) High-end n-channel active clamping. (b) Low-end n-channel active clamping. (c) Low-end p-channel active clamping.

is turning off and the time Q_2 is turning on. During the dead time, the primary current flows through the body diode of either MOSFET. This is a resonant time interval in which zero-voltage switching occurs. Neglecting the voltage drop across the leakage inductance, the voltage across the clamping capacitor C_c is

$$V_{Cc(H)} = \frac{V_I}{1-D}. \tag{6.266}$$

Therefore, it is also called a boost-type clamp. The voltage across the main switch Q_1 is given by

$$V_{DS(Q_1)} = \frac{V_I^2}{V_I - nV_O}. \tag{6.267}$$

The clamping circuit of Figure 6.29(b) is connected in parallel with the main switch. It is called the low-end n-channel active clamp. Neglecting the voltage drop across the leakage inductance, the voltage across the clamping capacitor C_c is

$$V_{Cc(L)} = \frac{D}{1-D}V_I. \tag{6.268}$$

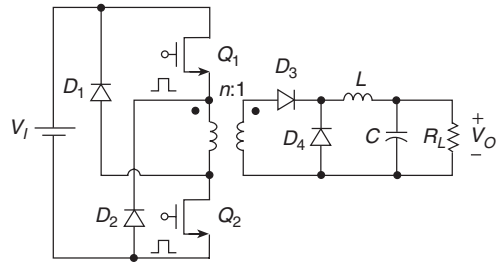


Figure 6.30 Two-transistor forward converter.

Therefore, it is also called a buck-boost-type clamp. The voltage across the main switch Q_1 is given by (6.267). The clamping circuit of Figure 6.29(c) is called the low-end p-channel active clamp. It uses a p-channel MOSFET. There is no need for the transformer reset circuit in all three circuits.

6.7 Two-switch Forward Converter

A two-transistor forward converter is shown Fig 6.30. The two transistors are ON during the time interval $0 < t \leq DT$ and OFF during the reminder of the cycle. During the interval $0 < t \leq DT$, the voltage across the primary winding is V_I, the current through the magnetizing inductance L_m flows through both transistors, and it increases with slope V_I/L_m. After the transistors are turned off, the demagnetization diodes are forced to conduct by the magnetizing current, the voltage across the primary winding is $-V_I$, the current of the magnetizing inductance L_m decreases to zero at time $t = DT + t_m$ with slope $-V_I/L_m$, and the energy stored in the magnetizing inductance L_m is returned to the input voltage source V_I. The magnetizing current is reset to zero before the beginning of the next cycle. When the magnetizing current reaches zero, both demagnetization diodes turn off. Therefore, the duty cycle must be held in the range $0 < D < 0.5$. There is no need for a core reset circuit. The rectifier circuit on the secondary side of the transformer is identical to that of the single-transistor forward converter. The horizontal rectifier diode conducts when both transistors are ON, and the freewheeling diode conducts when both transistors are OFF. The dc voltage transfer function is

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{\eta D}{n}. \tag{6.269}$$

The two-switch forward converter has reduced ringing. The peak voltage across the switches is $V_{SM} = V_I$. However, the circuit requires a floating gate drive for the high saide transistor.

6.8 Summary

- The PWM forward converter can be derived from the buck converter by adding a transformer, a diode, and a transformer core reset circuit. Therefore, it belongs to the family of buck-derived converters.
- The PWM forward converter provides dc isolation between the input and the output.
- The transformer allows the forward converter to obtain much lower and much higher values of the dc voltage transfer function than those of the buck converter.

- The forward converter is a step-down or a step-up converter.
- If the number of turns of the primary and tertiary is the same, the voltage stress on the transistor is twice the dc input voltage and the duty cycle D must be less than 0.5 in the forward converter.
- The typical power level of the forward converter is from 30 to 500 W.
- The transistor is driven with respect to ground in the forward converter.
- The magnetizing inductance of the transformer is not required to store energy.
- The forward converter requires a transformer core reset circuit.
- The maximum duty cycle in the forward converter is less than 100 % to allow for core reset.
- The magnetic core utilization is poor in the forward converter because a dc current flows through the primary.
- The forward converter can operate in two modes: CCM or DCM.
- The dc voltage transfer function of the lossless forward converter is $M_{V\ DC} = D/n_1$.
- The duty cycle D of the lossy converter is greater than that of the lossless converter at the same dc voltage transfer function.
- The peak-to-peak value of the inductor current ripple Δi_L is independent of the dc load current for CCM.
- The peak-to-peak value of the current through the filter capacitor C is equal to the peak-to-peak inductor current ripple Δi_L.
- The peak-to-peak ripple current through the filter capacitor decreases as the inductance L increases.
- If the capacitance of the filter capacitor is sufficiently high, the output ripple voltage is determined only by the ESR of the filter capacitor and is independent of the capacitance of the filter capacitor.
- The minimum value of the inductance L is determined by the CCM/DCM boundary, ripple of the output voltage, or ac losses in the inductor and/or filter capacitor.
- A disadvantage of the forward converter is that the input current is pulsating. However, a nonpulsating input current waveform can be obtained by inserting an input LC filter between the input dc source and the transistor.
- The corner frequency of the output filter $f_o = 1/(2\pi\sqrt{LC})$ is independent of the load resistance.
- For the forward converter operating in CCM and DCM, the minimum efficiency occurs at the maximum load current I_{Omax} (or R_{Lmin}) and a high efficiency occurs at light loads.

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6.10 Review Questions

6.1 Does the forward PWM converter provide dc isolation between the input and the output?

6.2 Does the forward converter require a transformer core reset circuit? Explain its operation.

6.3 What is the range of the duty cycle in the forward converter?

6.4 Is the forward converter a step-down or a step-up converter?

6.5 Is the transformer required to store energy in the forward converter?

6.6 Is the input current of the basic forward converter pulsating?

6.7 How can the forward converter circuit be modified to obtain a nonpulsating input current?

6.8 Is the transistor drive circuit floating with respect to ground in the forward converter?

6.9 How is the dc voltage transfer function $M_{V\ DC}$ related to the duty cycle D of the lossless forward converter for CCM?

6.10 Is the duty cycle D of the lossy forward converter lower or greater than that of the lossless converter at a given value of $M_{V\ DC}$ for CCM?

6.11 Is the corner frequency of the output filter dependent on the load resistance in the forward converter?

6.12 Is it possible to obtain a negative output voltage in the forward converter? If so, draw a circuit of such a converter.

6.13 Is it possible to obtain a multiple-output forward converter? If so, draw the circuit of such a converter.

6.14 Is it possible to control all the outputs in the forward converter?

6.15 What is the typical output power range of the forward converter?

6.16 Is the efficiency high at heavy or light loads for the forward converter?

6.11 Problems

6.1 For the forward PWM converter, find the maximum duty cycle D_{MAX}: (a) for $n_3 = 0.5n_1$; (b) for $n_3 = 2n_1$; (c) for $n_3 = 4n_1$.

6.2 For the forward PWM converter, find the switch peak voltage in terms of the dc input voltage V_I: (a) for $n_3 = 0.5n_1$; (b) for $n_3 = 2n_1$; (c) for $n_3 = 4n_1$.

6.3 For the forward PWM converter, find the peak voltage of the diode D_3 connected in series with the tertiary in terms of the dc input voltage V_I: (a) for $n_3 = 0.5n_1$; (b) for $n_3 = 2n_1$; (c) for $n_3 = 4n_1$.

6.4 A forward PWM converter is supplied by a European single-phase rectified utility line voltage and $V_O = 12$ V. Find the primary-to-secondary transformer turns ratio n_1.

6.5 A forward PWM converter is supplied by a European single-phase rectified utility line voltage, $V_O = 12$ V, and $n_1 = 8$. Find the maximum permissible duty cycle D_{MAX}.

6.6 A forward PWM converter is supplied by a European single-phase rectified utility line voltage, $V_O = 12$ V, and $n_1 = n_3 = 8$. Find the minimum, nominal, and maximum duty cycle.

6.7 A forward PWM converter is supplied by a European single-phase rectified utility line voltage, $V_{Imax} = 342$ V, $V_O = 12$ V, and $n_1 = n_3 = 8$. Find the voltage stresses of the semiconductor devices.

6.8 A forward PWM converter has $V_O = 12$ V, $I_O = 4$ to 40 A, $n_1 = n_3 = 8$, $V_{Imax} = 342$ V, $\eta = 90\,\%$, and $f_s = 75$ kHz. Find the minimum inductance required for CCM operation.

6.9 A forward PWM converter has $V_O = 12$ V, $I_O = 4$ to 40 A, duty cycle $D_{min} = 0.3119$, $L = 20\,\mu$H, $f_s = 75$ kHz, and $V_r/V_O \leq 1\,\%$. Find the filter capacitance and the corner frequency of the output filter.

6.10 A forward PWM converter has $V_O = 12$ V, $I_O = 4$ to 40 A, $L = 20\,\mu$H, $D_{min} = 0.3119$, and $f_s = 75$ kHz. Find the current stresses of the rectifier diodes.

6.11 A forward PWM converter has $V_O = 12$ V, $I_O = 4$ to 40 A, $n_1 = n_3 = 8$, $L = 20\,\mu$H, $V_{Imax} = 342$ V, $D_{min} = 0.3119$, and $f_s = 75$ kHz. Find the magnetizing inductance such that its peak current is less than 12 % of the maximum peak current of the primary of the ideal transformer.

6.12 A forward PWM converter is supplied by a European single-phase rectified utility line voltage, $V_O = 12\,\text{V}$, $I_O = 4$ to $40\,\text{A}$, $n_1 = n_3 = 8$, $L = 20\,\mu\text{H}$, and $f_s = 75\,\text{kHz}$. Find the current stress of the switch.

6.13 For a forward PWM converter supplied by a European single-phase rectified utility line voltage, determine the maximum inductance required for DCM operation, if $V_O = 12\,\text{V}$, $I_O = 0$ to $4\,\text{A}$, $n_1 = n_3 = 8$, and $f_s = 75\,\text{kHz}$.

6.14 Design a PWM forward converter that will meet the following specifications: CCM, V_I is the European single-phase rectified line voltage with $V_{rms} = 220\,\text{V} \pm 10\,\%$, $V_O = 14\,\text{V}$, $I_{Omin} = 2\,\text{A}$, $I_{Omax} = 20\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Assume $r_{DS} = 1\,\Omega$, $V_F = 0.56\,\text{V}$, $R_F = 25\,\text{m}\Omega$, $r_{L(dc)} = 20\,\text{m}\Omega$, $r_{T1} = 100\,\text{m}\Omega$, $r_{T2} = 25\,\text{m}\Omega$, $C_o = 100\,\text{pF}$, $L_m = 5\,\text{mH}$, and $f_s = 100\,\text{kHz}$. Find component values, component stresses, and converter efficiency.

6.15 Design a PWM forward converter with $V_I = 48 \pm 6\,\text{V}$, $V_O = 5\,\text{V}$, $I_O = 2$ to $20\,\text{A}$, $f_s = 50\,\text{kHz}$, $V_r/V_O \leq 1\,\%$, and $\Delta i_{Lm(max)}/I_{1max} \leq 10\,\%$. Find L, L_m, C, r_C, n_1, n_3, D_{min}, D_{max}, D_{MAX}, V_{SMmax}, I_{SMmax}, V_{D1Mmax}, I_{D1Mmax}, V_{D2Mmax}, I_{D2Mmax}, V_{D3Mmax}, I_{D3Mmax}, and η. Assume CCM, $r_{DS} = 0.18\,\Omega$, $V_F = 0.4\,\text{V}$, $R_F = 20\,\text{m}\Omega$, $r_{L(dc)} = 20\,\text{m}\Omega$, $r_{T1} = 50\,\text{m}\Omega$, $r_{T2} = 15\,\text{m}\Omega$, and $C_o = 200\,\text{pF}$.

6.16 A PWM forward converter has $V_I = 24$ to $32\,\text{V}$, $I_O = 2$ to $20\,\text{A}$, $V_O = 18\,\text{V}$, and $f_s = 150\,\text{kHz}$. Find L, C, n_1, n_3, D_{min}, D_{max}, D_{MAX}, V_{SMmax}, I_{SMmax}, I_{D1Mmax}, V_{D1Mmax}, and V_{D3Mmax}.

6.17 Draw a circuit of a multiple-output dc-dc forward converter with $V_{O1} = 3.3\,\text{V}$, $V_{O2} = 12\,\text{V}$, and $V_{O3} = -12\,\text{V}$.

7

Half-bridge PWM DC–DC Converter

7.1 Introduction

The half-bridge PWM dc–dc converter [1]–[23] contains two transistors, a transformer, and a rectifier. Its main advantage is that the voltage stresses of the transistors are low and equal to the maximum dc input voltage of the converter. It can handle the rectified dc voltage of the European 220 Vrms + 10 % utility single-phase line, which is usually in the range from 280 to 340 V. Power transistors with a voltage rating of 400 to 500 V are readily available and may be used in this converter; therefore, the half-bridge converter is used in off-line power supplies. Another advantage is that the core saturation problems are minimized because the dc component of the current through the primary is zero due to the coupling or blocking capacitors in series with the primary. Since the primary is driven in both directions, the core is utilized more effectively. The disadvantages are the requirement of an additional power transistor and of an isolated driver for the upper transistor. Typically, the converter is suitable for medium- and high-power applications from 150 W to 1 kW and is widely used in telecommunications power supplies. It belongs to the family of buck-derived converters. The purpose of this chapter is to present an analysis and design procedure for the half-bridge PWM converter.

7.2 DC Analysis of PWM Half-bridge Converter for CCM

7.2.1 Circuit Description

A PWM half-bridge dc–dc converter circuit is depicted in Figure 7.1(a). The converter consists of a PWM inverter and a PWM rectifier. The inverter consists of two power MOSFETs

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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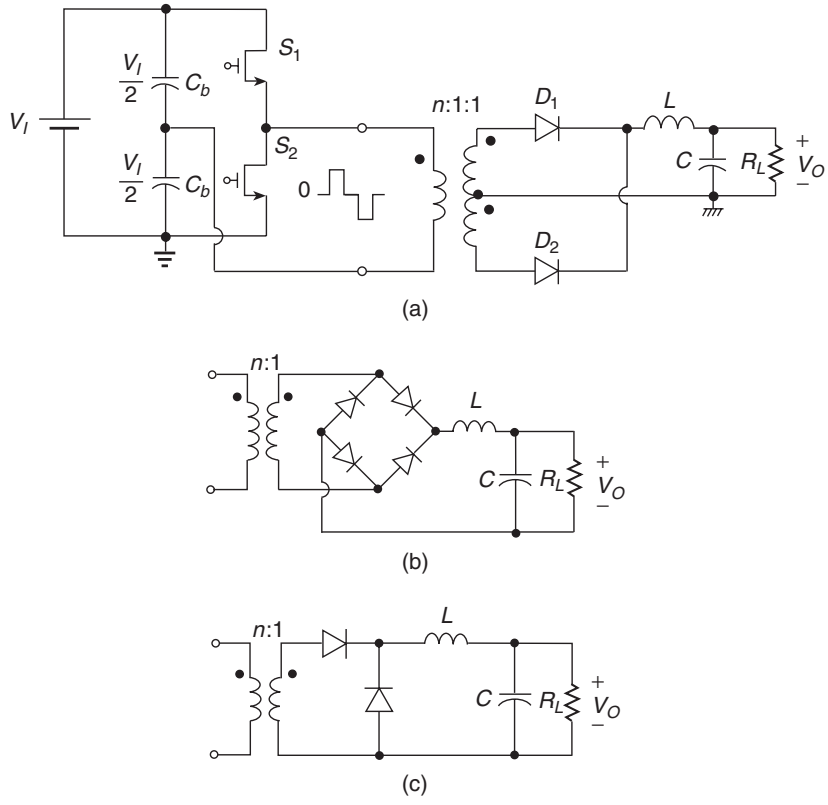


Figure 7.1 Half-bridge converter with two blocking capacitors. (a) With a transformer center-tapped rectifier. (b) With a full-bridge rectifier. (c) With a half-wave rectifier.

used as controllable switches S_1 and S_2, a transformer, and two blocking capacitors C_b. The isolation transformer does not have to store energy. Its magnetizing inductance should be large enough to reduce the current through this inductance and the switches. Because of the blocking capacitors, the dc current through the primary of the transformer is zero, resulting in excellent core utilization. In addition, the core is operated in a bipolar mode because the primary winding is driven in both directions from $V_I/2$ to $-V_I/2$; therefore, the core is utilized more effectively. The core is half the size of that in equivalent transformers in single-transistor converters, in which magnetic cores are operated in unipolar mode. Therefore, the half-bridge converter provides a cost advantage over its single-transistor counterparts.

The transistors are driven by nonoverlapping voltages that are out of phase by 180°. The maximum duty cycle of gate-to-source voltages is slightly less than 50 %. The waveforms of the gate voltages should be nonoverlapping to avoid the situation where both transistors are conducting at the same time. In this case, the dc input voltage V_I is connected to the ground through two MOSFET on-resistances, generating a very large current spike and destroying the transistors. For example, if the dc input voltage is $V_I = 340\,\text{V}$ and the MOSFET on-resistance is $r_{DS} = 1\,\Omega$, then the peak current through the MOSFETs is $I_{pk} = V_I/(2r_{DS}) = 340/2 = 170\,\text{A}$. The phenomenon where both transistors are conducting at the same time is called a *cross-conduction*, and the current through the transistors is called a *shoot-through current*. The switching network of the inverter has a totem pole arrangement, resulting in difficulty in driving the upper transistor because its gate is not referenced to ground. A small

pulse transformer is normally used to drive the upper transistor. A second pulse transformer is usually added to drive the lower transistor. Such a driver provides dc isolation in the control path. DC isolation is required in the power stage and control circuit to accomplish a dc isolation between the input and the output of a dc–dc converter. Pulse transformers also provide protection for control circuits against high-voltage breakdown. The transistor may be broken in such a way that there is a short circuit between the transistor drain and gate, and a high voltage V_I appears at the transistor gate. If the control circuit is directly coupled to the gate, a high voltage is applied across the control circuit output, destroying the control circuit. However, if a control circuit is coupled to the gate through a pulse transformer, the control circuit will not be damaged by a high voltage at the transistor gate.

Assuming that both blocking capacitors C_b are identical, the voltage drop across each of them is $V_I/2$. These are usually large electrolytic capacitors with very large tolerances (e.g., $-20\,\%$ and $+100\%$); therefore, the voltage drops across them may be different from $V_I/2$. To make these voltages closer to each other, large balance resistors R_b of the order of $100\,\text{k}\Omega$ to $1\,\text{M}\Omega$ may be connected in parallel with the blocking capacitors. If the front-end rectifier is a voltage doubler, its filter capacitors can be used as the blocking capacitors C_b. The dc current through the primary of the transformer is zero because of the blocking capacitors C_b. However, this property is lost if resistors are connected in parallel with the blocking capacitors C_b.

The half-bridge converter may employ the following rectifiers: a transformer center-tapped rectifier, shown in Figure 7.1(a); a bridge rectifier, depicted in Figure 7.1(b); or a half-wave rectifier with a freewheeling diode, shown in Figure 7.1(c). Full-wave rectifiers (i.e., center-tapped and bridge rectifiers) are more suitable because the voltage across the primary winding changes in both directions, from $V_I/2$ to $-V_I/2$. The transformer center-tapped rectifier consists of two diodes D_1 and D_2, an inductor L, a filter capacitor C, and a load resistor R_L. It is most suitable for low-voltage applications because only one diode conducts while it carries the entire inductor current. Schottky diodes or low on-resistance power MOSFETs can be used as rectifying devices. The voltage stress of the diodes is high, equal to V_I/n, and makes the center-tapped rectifier unsuitable for high-voltage applications.

In contrast, the bridge rectifier is suitable for high-voltage applications because the voltage stress of the diodes is low, equal to $V_I/(2n)$, which is half of that in the center-taped rectifier. This rectifier is not suitable for low-voltage applications because two diodes conduct at the same time and the total forward voltage across the two diodes becomes comparable with the output voltage. As a result, the efficiency is poor at a low output voltage V_O.

To eliminate the dc current through the primary winding, a nonelectrolytic coupling capacitor C_c (2 to $10\,\mu\text{F}$) may be connected in series with the primary winding, as shown in Figure 7.2. The voltage across C_c is the average voltage across the bottom switch, which is equal to $V_I/2$. For the ac component, the dc input source V_I in the converter of Figure 7.1(a) behaves similarly to a short circuit and the two blocking capacitors are connected in parallel, resulting in the converter circuit shown in Figure 7.2(a), where $C_c = 2C_b$.

7.2.2 Assumptions

Analysis of the half-bridge PWM converter with a transformer center-tapped rectifier, shown in Figure 7.1(a), is based on the following assumptions:

1. The power MOSFETs and the diodes are ideal switches.
2. The capacitances and lead inductances of the transistors and the diodes are zero.

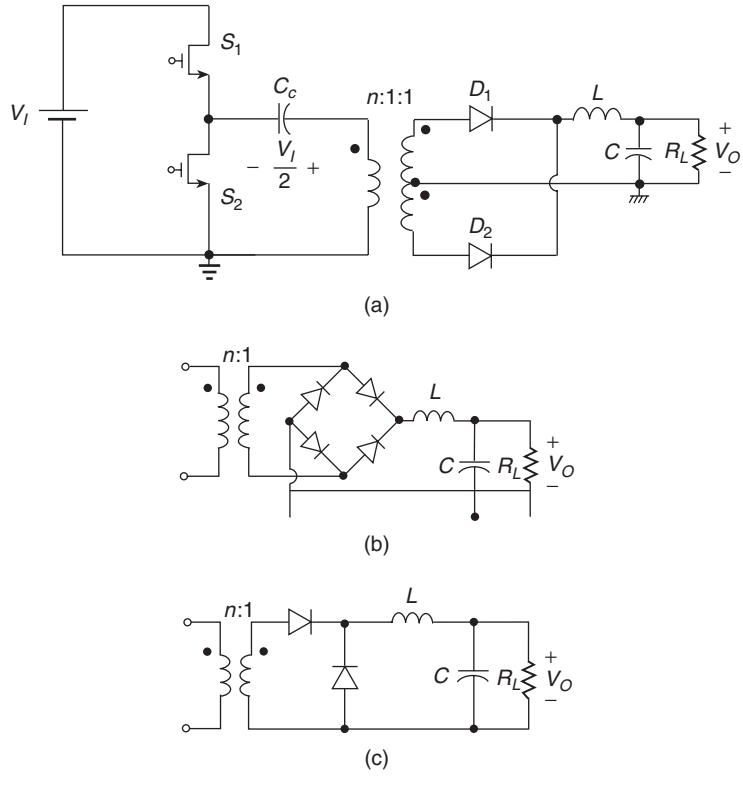


Figure 7.2 Half-bridge converter with a single coupling capacitor C_c. (a) With a transformer center-tapped rectifier. (b) With a bridge rectifier. (c) With a half-wave rectifier.

3. The transformer is modeled by an ideal transformer and its magnetizing inductance L_m. Leakage inductances and stray capacitances are neglected.
4. Passive components are linear, time-invariant, and frequency-independent.
5. The output impedance of the input voltage source V_I is zero for both dc and ac components.

7.2.3 Time Interval $0 < t \leq DT$

During the time interval $0 < t \leq DT$, the switch S_1 and diode D_1 are ON and the switch S_2 and diode D_2 are off. An ideal equivalent circuit for this time interval is shown in Figure 7.3(a). The voltage across the switch S_2 is

$$v_{S2} = V_I. \tag{7.1}$$

The voltage across the primary and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = V_I - \frac{V_I}{2} = \frac{V_I}{2} = L_m \frac{di_{Lm}}{dt}. \tag{7.2}$$

Hence, the current through the magnetizing inductance L_m is

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt + i_{Lm}(0) = \frac{1}{L_m}\int_0^t \left(\frac{V_I}{2}\right) dt + i_{Lm}(0) = \frac{V_I}{2L_m}t + i_{Lm}(0), \tag{7.3}$$

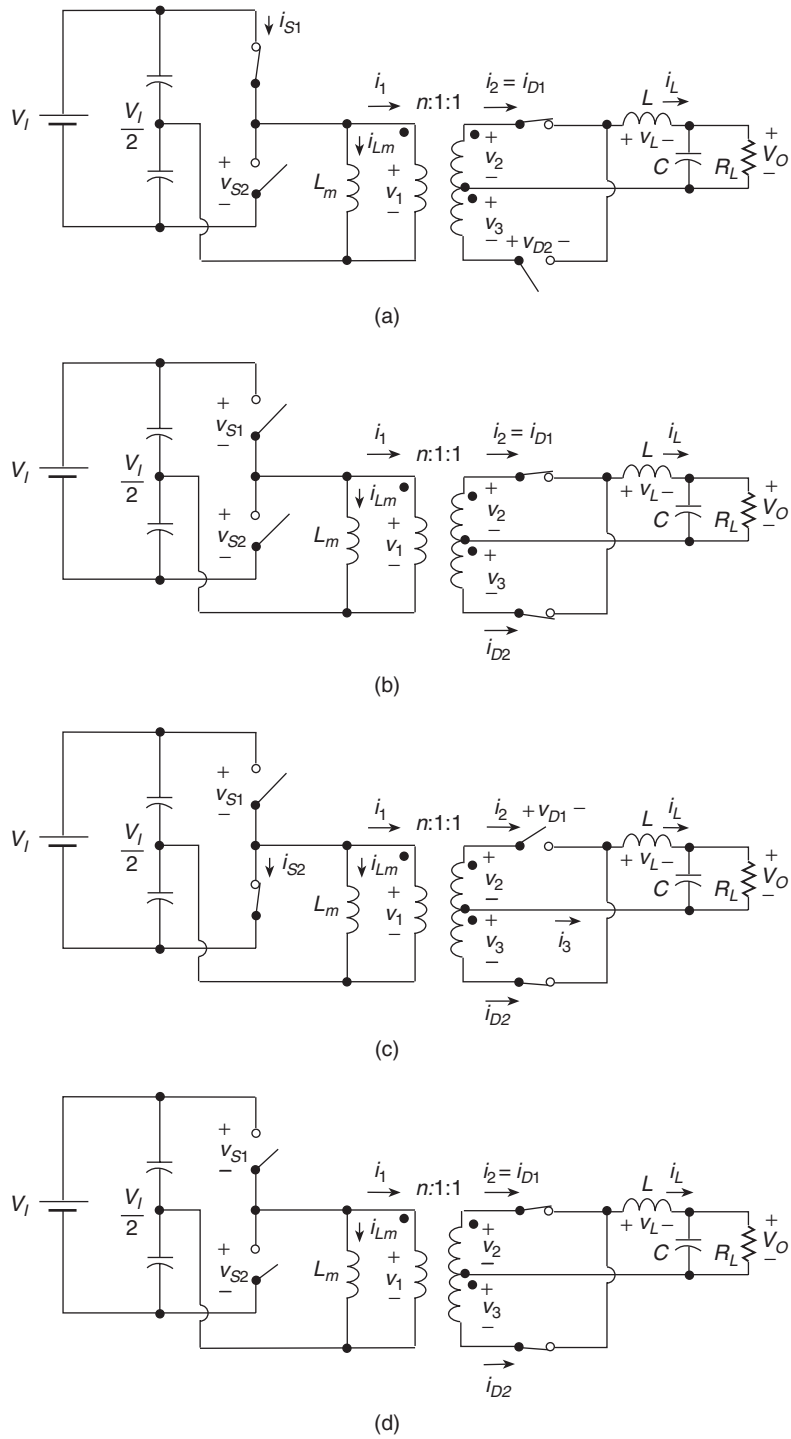


Figure 7.3 Equivalent circuit of the half-bridge converter with a transformer center-tapped rectifier for CCM. (a) For $0 < t \leq DT$. (b) For $DT < t \leq T/2$. (c) For $T/2 < t \leq T/2 + DT$. (d) For $T/2 + DT < t \leq T$.

where $i_{Lm}(0)$ is the initial current through the magnetizing inductance L_m at $t = 0$; this current is negative. The peak-to-peak ripple current through L_m is

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(0) = \frac{V_I DT}{2L_m} = \frac{DV_I}{2f_s L_m}. \tag{7.4}$$

Consequently,

$$i_{Lm}(0) = -\frac{\Delta i_{Lm}}{2} = -\frac{V_I D}{4f_s L}, \tag{7.5}$$

$$i_{Lm}(DT) = \frac{\Delta i_{Lm}}{2} = \frac{V_I D}{4f_s L}, \tag{7.6}$$

and

$$i_{Lm} = \frac{V_I}{2L_m} t - \frac{V_I D}{4f_s L}. \tag{7.7}$$

From (7.4),

$$\Delta i_{Lm(max)} = \frac{D_{min} V_{Imax}}{2f_s L_{m(min)}}, \tag{7.8}$$

from which

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{2f_s \Delta i_{Lm(max)}}. \tag{7.9}$$

Note that $DV_I = D_{min} V_{Imax} = D_{max} V_{Imin}$ is constant if the output voltage V_O is held constant.

The output voltages of the transformer are

$$v_2 = v_3 = \frac{v_1}{n} = \frac{V_I}{2n}. \tag{7.10}$$

The voltage across the diode D_2 is

$$v_{D2} = -v_2 - v_3 = -\frac{V_I}{2n} - \frac{V_I}{2n} = -\frac{V_I}{n}. \tag{7.11}$$

The negative diode voltage keeps the diode reverse biased, as originally assumed. The voltage across the inductor L is given by

$$v_L = \frac{V_I}{2n} - V_O = L\frac{di_L}{dt}. \tag{7.12}$$

Hence, one obtains the current through inductor L,

$$\begin{aligned} i_2 = i_{D1} = i_L &= \frac{1}{L}\int_0^t v_L\, dt + i_L(0) = \frac{1}{L}\int_0^t \left(\frac{V_I}{2n} - V_O\right) dt + i_L(0) \\ &= \frac{\dfrac{V_I}{2n} - V_O}{L} t + i_L(0), \end{aligned} \tag{7.13}$$

where $i_L(0)$ is the initial current in the inductor L at time $t = 0$. The peak inductor current becomes

$$i_L(DT) = \frac{\left(\dfrac{V_I}{2n} - V_O\right) DT}{L} + i_L(0), \tag{7.14}$$

and the peak-to-peak value of the current ripple through the inductor L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{\left(\dfrac{V_I}{2n} - V_O\right) DT}{L} = \frac{\left(\dfrac{V_I}{2n} - V_O\right) D}{f_s L} = \frac{V_O(0.5 - D)}{f_s L}, \tag{7.15}$$

where $V_I = nV_O/D$ as will shortly be shown. The current through the primary of the transformer is

$$i_1 = \frac{i_2}{n} = \frac{\dfrac{V_I}{2n} - V_O}{nL}t + \frac{i_L(0)}{n}, \tag{7.16}$$

and the current through the switch is

$$i_{S1} = i_1 + i_{Lm} = \frac{\dfrac{V_I}{2n} - V_O}{nL}t + \frac{i_L(0)}{n} + \frac{V_I}{2L_m}t + i_{Lm}(0)$$

$$= \frac{\dfrac{V_I}{2n} - V_O}{nL}t + \frac{i_L(0)}{n} + \frac{V_I}{2L_m}t - \frac{V_I D}{4f_s L}. \tag{7.17}$$

Current and voltage waveforms in the half-bridge converter for CCM are depicted in Figure 7.4.

7.2.4 Time Interval $DT < t \leq T/2$

Figure 7.3(b) shows an equivalent circuit of the converter for the time interval $DT < t \leq T/2$, during which both switches are OFF and both diodes are ON. Assuming that the

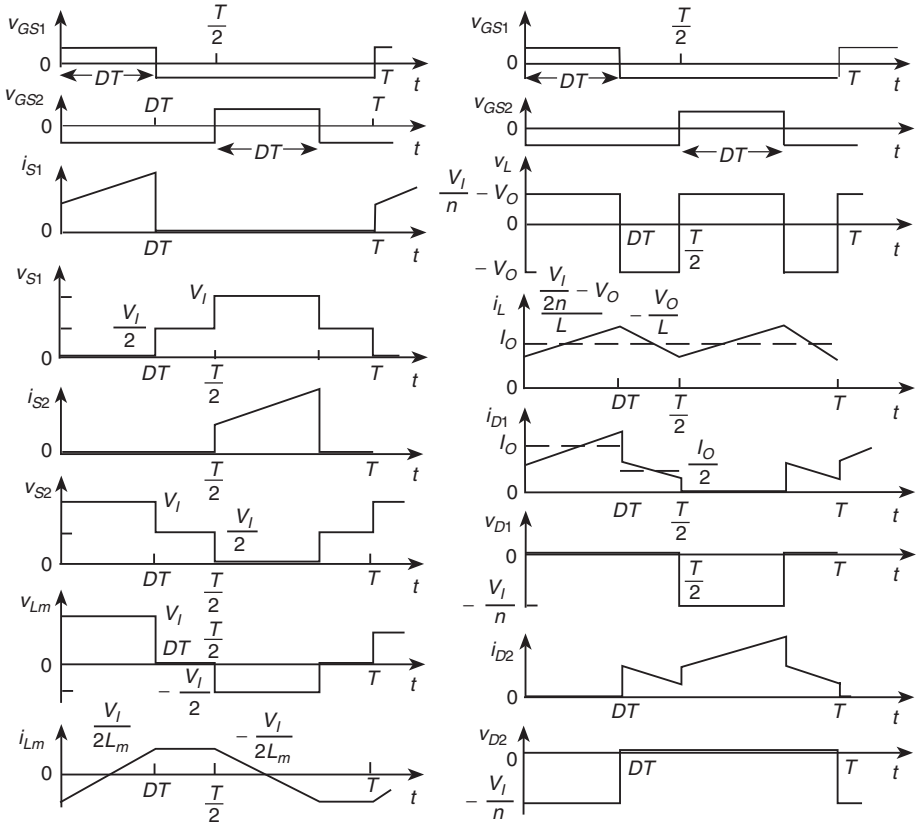


Figure 7.4 Waveforms in the half-bridge converter with a transformer center-tapped rectifier for CCM.

off-resistances of the switches are the same, the voltages across both switches are

$$v_{S1} = v_{S2} = \frac{V_I}{2}. \tag{7.18}$$

As a result, the voltage across the primary winding and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = L_m \frac{di_{Lm}}{dt} = 0, \tag{7.19}$$

resulting in the current through the magnetizing inductance,

$$i_{Lm} = i_{Lm}(DT) = -\frac{V_I D}{4 f_s L}, \tag{7.20}$$

and the current through the primary,

$$i_1 = -i_{Lm} = -i_{Lm}(DT) = \frac{V_I D}{4 f_s L}. \tag{7.21}$$

The currents through both secondary windings are equal in magnitude, but flow in opposite directions, resulting in zero magnetic flux; therefore, the voltages across the transformer secondary windings are

$$v_2 = v_3 = 0. \tag{7.22}$$

Hence, both rectifier diodes are ON . The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{7.23}$$

and the inductor current is

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L \, dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT). \tag{7.24}$$

Assuming that the rectifier circuit is symmetrical, the inductor current is divided equally between the diodes,

$$i_{D1} = i_{D2} = \frac{i_L}{2} = -\frac{V_O}{2L}(t - DT) + \frac{i_L(DT)}{2}. \tag{7.25}$$

7.2.5 Time Interval $T/2 < t \leq T/2 + DT$

Figure 7.3(c) shows an equivalent circuit of the converter for the time interval $T/2 < t \leq T/2 + DT$, during which the switch S_1 and diode D_1 are OFF and the switch S_2 and diode D_2 are ON . The voltage across the switch S_1 is

$$v_{S1} = V_I. \tag{7.26}$$

The voltage across the primary and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = 0 - \frac{V_I}{2} = -\frac{V_I}{2} = L_m \frac{di_{Lm}}{dt}, \tag{7.27}$$

and the current through the magnetizing inductance is

$$\begin{aligned} i_{Lm} = \frac{1}{L_m}\int_{T/2}^{t} v_{Lm} \, dt + i_{Lm}\left(\frac{T}{2}\right) &= -\frac{V_I}{2L_m}\left(t - \frac{T}{2}\right) + i_{Lm}\left(\frac{T}{2}\right) \\ &= -\frac{V_I}{2L_m}\left(t - \frac{T}{2}\right) + \frac{V_I D}{4 f_s L}. \end{aligned} \tag{7.28}$$

The voltages at the transformer secondaries are

$$v_2 = v_3 = \frac{v_1}{n} = -\frac{V_I}{2n}. \tag{7.29}$$

The voltage across the diode D_1 is

$$v_{D1} = v_2 + v_3 = -\frac{V_I}{2n} - \frac{V_I}{2n} = -\frac{V_I}{n}. \tag{7.30}$$

The voltage across the inductor L is

$$v_L = \frac{V_I}{2n} - V_O = L\frac{di_L}{dt}. \tag{7.31}$$

Hence, the current through the bottom transformer winding, the diode D_2, and the inductor L is found to be

$$i_{D2} = -i_3 = i_L = \frac{1}{L}\int_{T/2}^{t} v_L\,dt + i_L\left(\frac{T}{2}\right) = \frac{\frac{V_I}{2n} - V_O}{L}\left(t - \frac{T}{2}\right) + i_L\left(\frac{T}{2}\right). \tag{7.32}$$

Hence, the current through the primary is

$$i_1 = \frac{i_3}{n} = -\frac{i_{D2}}{n} = -\frac{\frac{V_I}{2n} - V_O}{nL}\left(t - \frac{T}{2}\right) - \frac{i_L\left(\frac{T}{2}\right)}{n}. \tag{7.33}$$

The current through the switch S_2 is

$$\begin{aligned} i_{S2} &= -i_1 - i_{Lm} = \frac{\frac{V_I}{2n} - V_O}{nL}\left(t - \frac{T}{2}\right) + \frac{i_L\left(\frac{T}{2}\right)}{n} + \frac{V_I}{2L_m}\left(t - \frac{T}{2}\right) - i_{Lm}\left(\frac{T}{2}\right) \\ &= \frac{\frac{V_I}{2n} - V_O}{nL}\left(t - \frac{T}{2}\right) + \frac{i_L\left(\frac{T}{2}\right)}{n} + \frac{V_I}{2L_m}\left(t - \frac{T}{2}\right) - \frac{V_I D}{4f_s L}. \end{aligned} \tag{7.34}$$

7.2.6 Time Interval $T/2 + DT < t \leq T$

An equivalent circuit of the converter for the time interval $T/2 + DT < t \leq T$ is shown in Figure 7.3(d). Both switches are OFF and both diodes are ON during this time interval. The equivalent circuit for this time interval is the same as that of Figure 7.3(b). Therefore, the analysis of the converter is the same as that given in Section 7.2.4.

7.2.7 Device Stresses

The maximum value of the voltage of each switch is

$$V_{SMmax} = V_{Imax}, \tag{7.35}$$

and the maximum peak current of each switch is

$$I_{SMmax} = \frac{I_{DMmax}}{n} + \frac{\Delta i_{Lm(max)}}{2} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} + \frac{\Delta i_{Lm(max)}}{2}. \tag{7.36}$$

The maximum peak value of the voltage across each diode in the transformer center-tapped rectifier is

$$V_{DMmax} = \frac{V_{Imax}}{n}, \tag{7.37}$$

and in the full-bridge rectifier is

$$V_{DMmax} = \frac{V_{Imax}}{2n}. \tag{7.38}$$

The average value of the inductor current is equal to the dc output current I_O. Hence, one arrives at the peak current of each diode

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2}. \tag{7.39}$$

7.2.8 DC Voltage Transfer Function of Lossless Half-bridge Converter for CCM

Referring to Figure 7.4,

$$\left(\frac{V_I}{2n} - V_O\right) DT = V_O \left(\frac{1}{2} - D\right) T, \tag{7.40}$$

resulting in the dc voltage transfer function of the lossless converter,

$$M_{V\ DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{D}{n}, \quad \text{for } D \leq 0.5. \tag{7.41}$$

The range of $M_{V\,DC}$ is

$$0 \leq M_{V\,DC} \leq \frac{1}{2n}. \tag{7.42}$$

For the lossless converter, the output voltage V_O is independent of the load resistance R_L and depends only on the dc input voltage V_I.

Rearrangement of (7.41) gives $V_I = nV_O/D$. Hence, from (7.15),

$$\Delta i_{Lmax} = \frac{V_O(\frac{1}{2} - D_{min})}{f_s L}. \tag{7.43}$$

The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = \frac{V_I}{n}. \tag{7.44}$$

The dc current transfer function is

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n}{D}. \tag{7.45}$$

As D is increased from 0 to 0.5, $M_{I\,DC}$ decreases from ∞ to $2n$.

From (7.35), (7.36), and (7.41), the switch and the diode utilization in the half-bridge converter is characterized by the output-power capability

$$c_p \equiv \frac{P_O}{V_{SM} I_{SM}} = \frac{V_O I_O}{V_{SM} I_{SM}} = \frac{nV_O}{V_{SM}} = \frac{nV_O}{V_I} = D. \tag{7.46}$$

As D is increased from 0 to 0.5, c_p increases from 0 to 0.5.

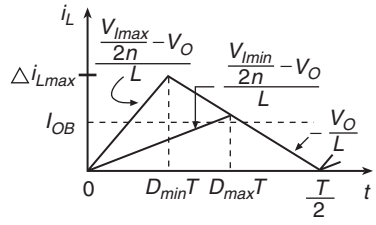


Figure 7.5 Waveforms of the inductor current in the half-bridge converter at CCM/DCM the boundary.

7.2.9 Boundary between CCM and DCM

The waveform of the inductor current at the CCM/DCM boundary is shown in Figure 7.5 and is given by

$$i_L = -\frac{V_O}{L}(t - DT) + i_L(DT), \quad \text{for } DT < t \le \frac{T}{2}, \tag{7.47}$$

from which

$$i_L\left(\frac{T}{2}\right) = -\frac{V_O T\left(\frac{1}{2} - D\right)}{L} + i_L(DT) = 0. \tag{7.48}$$

This gives the maximum peak value of the inductor current at the CCM/DCM boundary,

$$\Delta i_{Lmax} = \frac{V_O T\left(\frac{1}{2} - D_{min}\right)}{L_{min}} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{f_s L_{min}}. \tag{7.49}$$

The dc output current at the CCM/DCM boundary is

$$I_{Omin} = I_{OB} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s L_{min}} = \frac{V_O}{R_{Lmax}}. \tag{7.50}$$

Hence, the load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{0.5 - D}. \tag{7.51}$$

Thus, one obtains the minimum value of the inductance L,

$$L_{min} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s I_{Omin}} = \frac{R_{Lmax}\left(\frac{1}{2} - D_{min}\right)}{2f_s} = \frac{D_{min}\left(\frac{V_{Imax}}{2n} - V_O\right)}{2f_s I_{Omin}}. \tag{7.52}$$

Figures 7.6 and 7.7 respectively show the normalized load current $I_{OB}/(V_O/2f_sL) = (0.5 - D)$ and normalized load resistance $R_{LB}/(2f_sL) = 1/(0.5 - D)$ as function of duty cycle D at the CCM/DCM boundary for the half-bridge converter.

7.2.10 Ripple Voltage in Half-bridge Converter for CCM

The analysis of the ripple voltage for the half-bridge converter is similar to that for the buck converter. It can be shown that the ripple output voltage is equal to the ripple voltage across the ESR if

$$C \ge C_{min} = \max\left\{\frac{D_{max}}{2r_C f_s}, \frac{0.5 - D_{min}}{2r_C f_s}\right\} \tag{7.53}$$

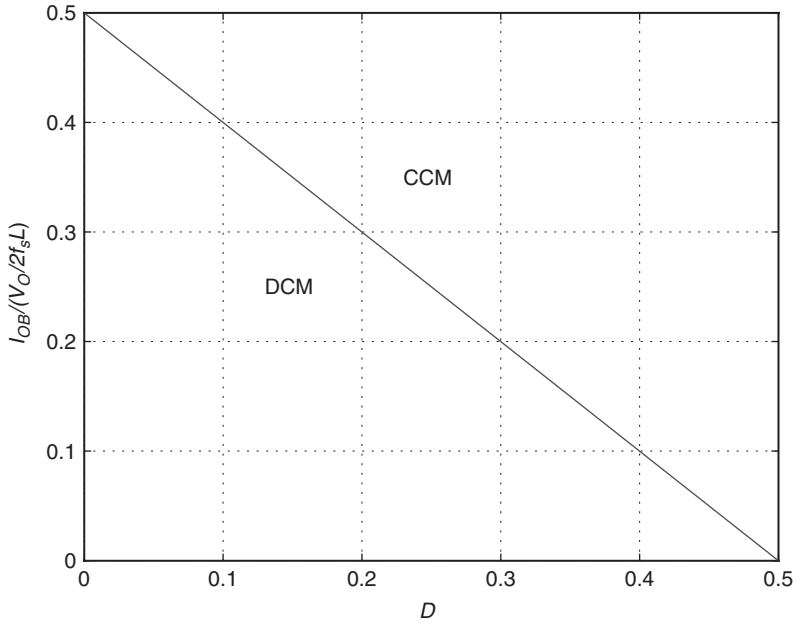


Figure 7.6 Normalized load current $I_{OB}/(V_O/2f_sL) = (0.5 - D)$ as a function of duty cycle D at the CCM/DCM boundary for the half-bridge converter.

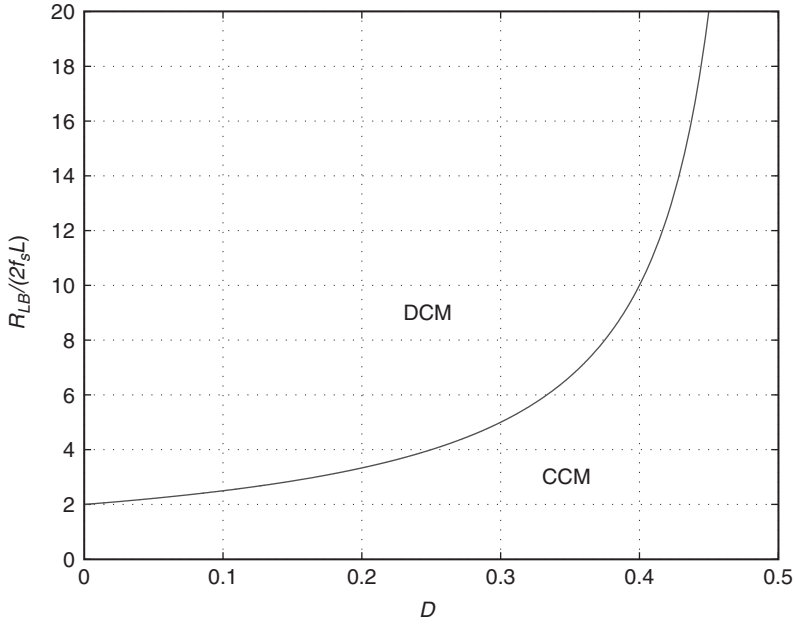


Figure 7.7 Normalized load resistance $R_{LB}/(2f_sL)$ as a function of duty cycle D at the CCM/DCM boundary for the half-bridge converter.

where $D_{max} \leq 0.5$. If condition (7.53) is satisfied, the peak-to-peak ripple output voltage V_r is expressed by

$$V_r = r_C \Delta i_{Lmax} = \frac{r_C V_O (0.5 - D_{min})}{f_s L}. \tag{7.54}$$

Setting $D_{max} = 0.5$ or $D_{min} = 0$, one obtains the worst-case condition for the capacitance at which the ripple is determined by the ESR of the filter capacitor for any value of D,

$$C \geq C_{min} = \frac{1}{4 r_C f_s}. \tag{7.55}$$

If condition (7.53) is not met, the peak-to-peak ripple output voltage V_r depends on the voltage across both the filter capacitance and the ESR. The maximum increase in the capacitor charge during each half of the cycle T is

$$\Delta Q = \frac{\frac{T}{4}\frac{\Delta i_{Lmax}}{2}}{2} = \frac{T \Delta i_{Lmax}}{16} = \frac{\Delta i_{Lmax}}{16 f_s}, \tag{7.56}$$

resulting in the ripple voltage across the capacitance C,

$$V_{Cpp} = \frac{\Delta Q}{C} = \frac{\Delta i_{Lmax}}{16 f_s C} = \frac{V_O (0.5 - D_{min})}{16 f_s^2 LC} = \frac{\pi^2 V_O (0.5 - D_{min}) f_o^2}{4 f_s^2}, \tag{7.57}$$

where $f_o = 1/(2\pi\sqrt{LC})$ is the corner frequency of the output low-pass filter. Hence,

$$C_{min} = \frac{\Delta i_{Lmax}}{16 f_s V_{Cpp}} = \frac{(0.5 - D_{min}) V_O}{16 f_s^2 L V_{Cpp}}. \tag{7.58}$$

The peak-to-peak ripple voltage across the ESR is

$$V_{rcpp} = r_C \Delta i_{Lmax} = \frac{r_C V_O (0.5 - D_{min})}{f_s L}. \tag{7.59}$$

The total ripple output voltage can be approximated by

$$V_{rpp} \approx V_{Cpp} + V_{rcpp} = \frac{V_O (0.5 - D_{min})}{16 f_s^2 LC} + \frac{r_C V_O (0.5 - D_{min})}{f_s L}. \tag{7.60}$$

7.2.11 Power Losses and Efficiency of Half-bridge Converter for CCM

Figure 7.8 depicts an equivalent circuit of the half-bridge converter with parasitic components, where r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The conduction losses will be determined assuming that the ripple of the inductor current is zero. Therefore, the inductor current can be approximated as

$$i_L \approx I_O. \tag{7.61}$$

The current through the switch S_1 can be expressed as

$$i_{S1} = \begin{cases} \dfrac{I_O}{n}, & \text{for } 0 < t \leq DT, \\ 0, & \text{for } DT < t \leq T. \end{cases} \tag{7.62}$$

The rms value of switch S_1 is

$$I_{S1rms} = \sqrt{\frac{1}{T}\int_0^{DT} i_{S1}^2 \, dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{D}}{n}, \tag{7.63}$$

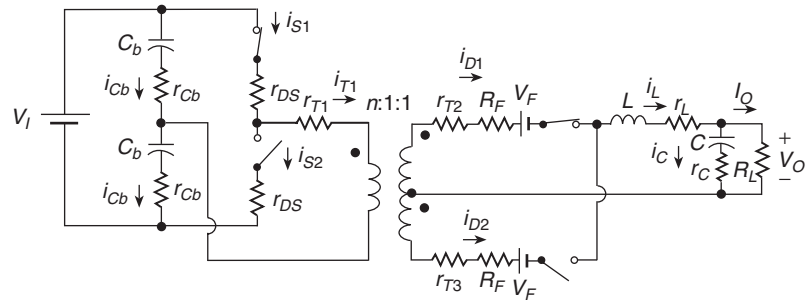


Figure 7.8 Equivalent circuit of the half-bridge converter with parasitic resistances to determine component losses.

and the conduction loss in the upper MOSFET is

$$P_{rDS1} = r_{DS1} I_{S1rms}^2 = \frac{D r_{DS1} I_O^2}{n^2} = \frac{D r_{DS1}}{n^2 R_L} P_O. \tag{7.64}$$

If the on-resistances of both the MOSFETs are identical (i.e., $r_{DS1} = r_{DS2} = r_{DS}$), then the conduction losses in both the MOSFETs are also identical (i.e., $P_{rDS1} = P_{rDS2} = P_{rDS}$).

Assuming that the transistor output capacitance C_o is linear, the switching loss per transistor is

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o n^2 V_O^2}{D^2} = \frac{f_s C_o V_O^2}{M_{V\,DC}^2} = \frac{f_s C_o n^2 R_L P_O}{D^2} = \frac{f_s C_o R_L P_O}{M_{V\,DC}^2}. \tag{7.65}$$

Hence, one obtains the total power dissipation in each MOSFET (excluding the drive power)

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \frac{D r_{DS} I_O^2}{n^2} + \frac{1}{2} f_s C_o V_I^2 = \left(\frac{D r_{DS}}{n^2 R_L} + \frac{f_s C_o n^2 R_L}{2 D^2} \right) P_O$$

$$= \left(\frac{D r_{DS}}{n^2 R_L} + \frac{f_s C_o R_L}{2 M_{V\,DC}^2} \right) P_O. \tag{7.66}$$

The current through the bottom blocking capacitors is

$$i_{Cb} \approx \begin{cases} \dfrac{I_O}{2n}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T/2, \\ -\dfrac{I_O}{2n}, & \text{for } T/2 < t \le T/2 + DT, \\ 0, & \text{for } T/2 + DT < t \le T. \end{cases} \tag{7.67}$$

Hence, the rms value of each blocking capacitor current is

$$I_{Cbrms} = \sqrt{\frac{1}{T} \int_0^T i_{Cb}^2 \, dt} = \sqrt{\frac{1}{T} \left[\int_0^{DT} \left(\frac{I_O}{2n} \right)^2 dt + \int_{T/2}^{T/2+DT} \left(-\frac{I_O}{2n} \right)^2 dt \right]}$$

$$= \sqrt{\frac{2}{T} \int_0^{DT} \left(\frac{I_O}{2n} \right)^2 dt} = \frac{I_O}{n} \sqrt{\frac{D}{2}}. \tag{7.68}$$

The power loss in the ESR r_{Cb} of each blocking capacitor is

$$P_{rCb} = r_{Cb} I_{Cbrms}^2 = \frac{r_{Cb} D I_O^2}{2n^2} = \frac{D r_{Cb}}{2n^2 R_L} P_O. \tag{7.69}$$

The rms value of the current through the primary winding is

$$I_{rT1rms} = \sqrt{\frac{1}{T}\int_0^T (i_{S1}^2 + i_{S2}^2)\,dt} = \sqrt{\frac{1}{T}\left[\int_0^{DT}\left(\frac{I_O}{n}\right)^2 dt + \int_{T/2}^{T/2+DT}\left(\frac{I_O}{n}\right)^2 dt\right]}$$

$$= \sqrt{\frac{2}{T}\int_0^{DT}\left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{2D}}{n}, \tag{7.70}$$

and the conduction loss in the primary winding resistance is

$$P_{rT1} = r_{T1}I_{T1rms}^2 = \frac{2Dr_{T1}I_O^2}{n^2} = \frac{2Dr_{T1}}{n^2R_L}P_O. \tag{7.71}$$

The current through the diode D_1 can be approximated by

$$i_{D1} = \begin{cases} I_O, & \text{for } 0 < t \le DT, \\ \dfrac{I_O}{2}, & \text{for } DT < t \le T/2, \\ 0, & \text{for } T/2 < t \le T/2 + DT, \\ \dfrac{I_O}{2}, & \text{for } T/2 + DT < t \le T, \end{cases} \tag{7.72}$$

leading to its rms value,

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^T i_{D1}^2 dt} = \sqrt{\frac{1}{T}\left[\int_0^{DT} I_O^2\,dt + 2\int_{DT}^{T/2}\left(\frac{I_O}{2}\right)^2 dt\right]} = \frac{I_O\sqrt{2D+1}}{2}, \tag{7.73}$$

and the power loss in R_F,

$$P_{RF1} = R_F I_{D1rms}^2 = \frac{(2D+1)R_F I_O^2}{4} = \frac{(2D+1)R_F}{4R_L}P_O. \tag{7.74}$$

The average value of the diode current is

$$I_{D(AV)} = \frac{1}{T}\int_0^T i_{D1}\,dt = \frac{I_O}{2}, \tag{7.75}$$

which gives the power loss associated with the voltage V_F,

$$P_{VF1} = V_F I_{D(AV)} = \frac{V_F I_O}{2} = \frac{V_F}{2V_O}P_O. \tag{7.76}$$

Thus, the overall diode conduction loss is

$$P_{D1} = P_{RF1} + P_{VF1} = \frac{(2D+1)R_F I_O^2}{4} + \frac{V_F I_O}{2} = \left[\frac{(2D+1)R_F}{4R_L} + \frac{V_F}{2V_O}\right]P_O. \tag{7.77}$$

The power loss in the secondary winding resistance r_{T2} is

$$P_{rT2} = r_{T2}I_{Drms}^2 = \frac{(2D+1)r_{T2}I_O^2}{4} = \frac{(2D+1)r_{T2}}{4R_L}P_O. \tag{7.78}$$

If both secondary winding resistances r_{T2} and r_{T3} are equal, then the conduction losses in both output windings are the same (i.e., $P_{rT2} = P_{rT3} = P_{rT}$).

The rms value of the inductor current is

$$I_{Lrms} \approx I_O, \tag{7.79}$$

and the inductor conduction loss is

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 = \frac{r_L}{R_L}P_O. \tag{7.80}$$

The current through the filter capacitor is

$$i_C \approx i_L - I_O = \begin{cases} \dfrac{\Delta i_L}{DT}t - \dfrac{\Delta i_L}{2}, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L}{\left(\frac{1}{2} - D\right)T}(t - DT) + \dfrac{\Delta i_L}{2}, & \text{for } DT < t \le T/2. \end{cases} \tag{7.81}$$

Hence, using (7.43), one arrives at the rms value of the capacitor current,

$$I_{Crms} = \sqrt{\frac{1}{(T/2)}\int_0^{T/2} i_C^2\, dt} = \frac{\Delta i_L}{\sqrt{12}} = \frac{V_O\left(\frac{1}{2} - D\right)}{\sqrt{12} f_s L}, \tag{7.82}$$

and the power loss in the ESR of the filter capacitor,

$$P_{rC} = r_C I_{Crms}^2 = \frac{r_C(\Delta i_L)^2}{12} = \frac{r_C V_O^2\left(\frac{1}{2} - D\right)^2}{12 f_s^2 L^2} = \frac{r_C R_L\left(\frac{1}{2} - D\right)^2 P_O}{12 f_s^2 L^2}. \tag{7.83}$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= 2P_{rDS1} + 2P_{sw} + P_{rT1} + 2P_{rCb} + 2P_{rT2} + 2P_{D1} + P_{rL} + P_{rC} \\ &= \frac{[2D(r_{DS} + r_{T1}) + Dr_{Cb}]I_O^2}{n^2} + 2f_s C_o V_I^2 + \frac{(2D+1)(R_F + r_{T2})I_O^2}{2} \\ &\quad + V_F I_O + r_L I_O^2 + \frac{r_C(\Delta i_L)^2}{12} \\ &= \left[\frac{2D(r_{DS} + r_{T1}) + Dr_{Cb}}{n^2 R_L} + \frac{2f_s C_o R_L}{M_{V\,DC}^2} + \frac{(2D+1)(R_F + r_{T2})}{2R_L}\right. \\ &\quad \left. + \frac{V_F}{V_O} + \frac{r_L}{R_L} + \frac{r_C R_L(\frac{1}{2} - D)^2}{12 f_s^2 L^2}\right] P_O. \end{aligned} \tag{7.84}$$

Thus, the converter efficiency is

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} \\ &= \frac{1}{1 + \dfrac{D[2(r_{DS} + r_{T1}) + r_{Cb}]}{n^2 R_L} + \dfrac{2f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{(2D+1)(R_F + r_{T2})}{2R_L} + \dfrac{V_F}{V_O}} \\ &\qquad + \frac{r_L}{R_L} + \frac{r_C R_L\left(\frac{1}{2} - D\right)^2}{12 f_s^2 L^2}. \end{aligned} \tag{7.85}$$

7.2.12 DC Voltage Transfer Function of Lossy Converter for CCM

Using (7.62), the dc component of the input current can be found to be

$$I_I = \frac{1}{T}\int_0^{DT} i_{S1}\, dt = \frac{1}{T}\int_0^{DT}\left(\frac{I_O}{n}\right) dt = \frac{DI_O}{n}. \tag{7.86}$$

This produces the dc current transfer function of the half-bridge converter,

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n}{D}. \tag{7.87}$$

This equation is valid for both lossless and lossy converters. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = \frac{n M_{V\,DC}}{D}, \tag{7.88}$$

from which the voltage transfer function of the lossy half-bridge converter is

$$\begin{aligned} M_{V\,DC} &= \frac{\eta}{M_{I\,DC}} = \frac{\eta D}{n} \\ &= \frac{D}{n\left[1 + \dfrac{2D(r_{DS} + r_{T1}) + D r_{Cb}}{n^2 R_L} + \dfrac{2 f_s C_o n^2 R_L}{D^2} + \dfrac{(2D+1)(R_F + r_{T2})}{2R_L} + \dfrac{V_F}{V_O} + \dfrac{r_L}{R_L} + \dfrac{r_C R_L \left(\frac{1}{2} - D\right)^2}{12 f_s^2 L^2}\right]}. \end{aligned} \tag{7.89}$$

Hence, one arrives at the on-duty cycle,

$$D = \frac{n M_{V\,DC}}{\eta} = \frac{n V_O}{\eta V_I}. \tag{7.90}$$

The duty cycle D, at a given dc voltage transfer function, is greater for the lossy converter than for the lossless converter. The switches must be closed for a longer portion of the lossy converter period in order to transfer enough energy to equal the required output energy and the converter losses.

Substitution of (7.90) into (7.85) gives the efficiency of the half-bridge converter

$$\eta = \frac{N_\eta}{D_\eta}, \tag{7.91}$$

where

$$\begin{aligned} N_\eta = 1 &- \frac{n M_{V\,DC}[2(r_{DS} + r_{T1}) + r_{Cb}]}{n^2 R_L} - \frac{n M_{V\,DC}(R_F + r_{T2})}{R_L} + \frac{r_C R_L n M_{V\,DC}}{12 f_s^2 L^2} \\ &+ \left\{\left[\frac{n M_{V\,DC}[2(r_{DS} + r_{T1}) + r_{Cb}]}{n^2 R_L} + \frac{n M_{V\,DC}(R_F + r_{T2})}{R_L} - \frac{r_C R_L n M_{V\,DC}}{12 f_s^2 L^2} - 1\right]^2 \right. \\ &\left. - \frac{r_C R_L n^2 M_{V\,DC}^2}{3 f_s^2 L^2}\left[1 + \frac{r_L}{R_L} + \frac{R_F + r_{T2}}{2R_L} + \frac{V_F}{V_O} + \frac{2 f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{48 f_s^2 L^2}\right]\right\}^{\frac{1}{2}} \end{aligned} \tag{7.92}$$

and

$$D_\eta = 2\left(1 + \frac{r_L}{R_L} + \frac{R_F + r_{T2}}{2R_L} + \frac{V_F}{V_O} + \frac{2 f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{48 f_s^2 L^2}\right). \tag{7.93}$$

7.2.13 Design of Half-bridge Converter for CCM

Design a PWM half-bridge converter operating in CCM to meet the following specifications: $V_{Inom} = \sqrt{2} \times 110 = 156\,\text{V}$, $V_{Imin} = \sqrt{2} \times 90 = 127\,\text{V}$, $V_{Imax} = \sqrt{2} \times 132 = 187\,\text{V}$, $V_O = 5\,\text{V}$, $I_{Omin} = 4\,\text{A}$, $I_{Omax} = 40\,\text{A}$, and $V_r/V_O \leq 1\,\%$.

Solution. A half-bridge converter with a transformer center-tapped rectifier is selected for the design because the output voltage is low. The maximum and minimum values of the

dc output power are

$$P_{Omax} = V_O I_{Omax} = 5 \times 40 = 200\,\text{W} \tag{7.94}$$

and

$$P_{Omin} = V_O I_{Omin} = 5 \times 4 = 20\,\text{W}. \tag{7.95}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{5}{40} = 0.125\,\Omega \tag{7.96}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{5}{4} = 1.25\,\Omega. \tag{7.97}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{5}{187} = 0.02674 = \frac{1}{37.4} \tag{7.98}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{5}{156} = 0.03205 = \frac{1}{31.2} \tag{7.99}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{5}{127} = 0.03937 = \frac{1}{25.4}. \tag{7.100}$$

Assume the converter efficiency is $\eta = 75\,\%$ and the maximum duty cycle $D_{max} \approx 0.4$. Hence, the transformer turns ratio is

$$n = \frac{\eta D_{max}}{M_{V\,DCmax}} = \frac{0.75 \times 0.4}{0.03937} = 7.62. \tag{7.101}$$

Pick $n = 7$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{nM_{V\,DCmin}}{\eta} = \frac{7 \times 0.02674}{0.75} = 0.2496, \tag{7.102}$$

$$D_{nom} = \frac{nM_{V\,DCnom}}{\eta} = \frac{7 \times 0.03205}{0.75} = 0.299, \tag{7.103}$$

and

$$D_{max} = \frac{nM_{V\,DCmax}}{\eta} = \frac{7 \times 0.03937}{0.75} = 0.3675. \tag{7.104}$$

Assume the switching frequency $f_s = 100\,\text{kHz}$. The minimum inductance required to maintain the converter in CCM is

$$L_{min} = \frac{R_{Lmax}\left(\frac{1}{2} - D_{min}\right)}{2f_s} = \frac{1.25 \times \left(\frac{1}{2} - 0.2496\right)}{2 \times 10^5} = 1.565\,\mu\text{H}. \tag{7.105}$$

Let $L = 20\,\mu\text{H}$. An inductance L much larger than L_{min} was selected in order to reduce the ripple current through the inductor and thus the filter capacitance. The maximum ripple of the inductor current is

$$\Delta i_{Lmax} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{f_s L} = \frac{5 \times \left(\frac{1}{2} - 0.2496\right)}{10^5 \times 20 \times 10^{-6}} = 0.626\,\text{A}. \tag{7.106}$$

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{5}{100} = 50\,\text{mV}. \tag{7.107}$$

If the filter capacitance is large enough, $V_r = r_{Cmax}\Delta i_{Lmax}$ and the maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{50 \times 10^{-3}}{0.626} = 79.87\,\text{m}\Omega. \tag{7.108}$$

Pick $r_C = 50\,\text{m}\Omega$. The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is

$$C_{min} = \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{\frac{1}{2} - D_{min}}{2f_s r_C}\right\} = \max\left\{\frac{0.3675}{2f_s r_C}, \frac{\frac{1}{2} - 0.2496}{2f_s r_C}\right\} = \frac{D_{max}}{2f_s r_C}$$

$$= \frac{0.3675}{2 \times 10^5 \times 50 \times 10^{-3}} = 36.75\ \mu\text{F}. \tag{7.109}$$

Pick $C = 47\,\mu\text{F}/50\,\text{m}\Omega/16\,\text{V}$.

The voltage and current stresses of the diodes are

$$V_{DMmax} = \frac{V_{Imax}}{n} = \frac{187}{7} = 26.7\,\text{V} \tag{7.110}$$

and

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = 40 + \frac{0.626}{2} = 40.313\,\text{A}. \tag{7.111}$$

The maximum peak value of the current through the ideal transformer primary is

$$I_{1max} = \frac{I_{DMmax}}{n} = \frac{40.313}{7} = 5.759\,\text{A}. \tag{7.112}$$

The maximum peak-to-peak current through the magnetizing inductance should be limited to, say, 10 % of I_{1max}, which gives

$$\Delta i_{Lm(max)} = 0.1 I_{1max} = 0.1 \times 5.759 = \frac{0.1 I_{DMmax}}{n} = 0.576\,\text{A}. \tag{7.113}$$

From (7.9), the minimum magnetizing inductance is

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{2f_s \Delta i_{Lm(max)}} = \frac{0.2496 \times 187}{2 \times 10^5 \times 0.576} = 405.2\,\mu\text{H}. \tag{7.114}$$

The voltage and current stresses of the power MOSFETs are

$$V_{SMmax} = V_{Imax} = 187\,\text{V} \tag{7.115}$$

and

$$I_{SMmax} = \frac{I_{DMmax}}{n} + \frac{\Delta i_{Lm(max)}}{2} = \frac{40.313}{7} + \frac{0.576}{2} = 6.047\,\text{A}. \tag{7.116}$$

International Rectifier IRF640 power MOSFETs are chosen, which have $V_{DSS} = 200\,\text{V}$, $I_{SM} = 18\,\text{A}$, $r_{DS} = 180\,\text{m}\Omega$, $C_o = 100\,\text{pF}$, and $Q_g = 43\,\text{nF}$. MBR2545CT Schottky barrier diodes are also chosen, which have $I_{D(AV)max} = 30\,\text{A}$, $I_{FSM} = 300\,\text{A}$, $V_{DM} = 45\,\text{V}$, $V_F = 0.27\,\text{V}$, and $R_F = 13.25\,\text{m}\Omega$.

The conduction power loss in each MOSFET is

$$P_{rDS1} = \frac{D_{max} r_{DS} I_{Omax}^2}{n^2} = \frac{0.3675 \times 0.18 \times 40^2}{7^2} = 2.16\,\text{W}, \tag{7.117}$$

and the switching loss per transistor is

$$P_{sw} = f_s C_o V_{Imax}^2 = 10^5 \times 100 \times 10^{-12} \times 187^2 = 0.35\,\text{W}. \tag{7.118}$$

Assuming that the winding resistance of the primary is $r_{T1} = 20\,\text{m}\Omega$ and the winding resistances of the transformer on the secondary side are $r_{T2} = r_{T3} = 5\,\text{m}\Omega$, the conduction

power loss is

$$P_{rT1} = \frac{2D_{max} r_{T1} I_{Omax}^2}{n^2} = \frac{2 \times 0.3675 \times 0.02 \times 40^2}{7^2} = 0.48\,\text{W} \tag{7.119}$$

and

$$P_{rT2} = P_{rT3} = \frac{(2D_{max} + 1) r_{T2} I_{Omax}^2}{4}$$

$$= \frac{(2 \times 0.3675 + 1) \times 0.005 \times 40^2}{4} = 3.47\,\text{W}. \tag{7.120}$$

Assuming that $r_{Cb} = 50\,\text{m}\Omega$, the power loss in the ESR of each blocking capacitor is

$$P_{rCb} = \frac{r_{Cb} D_{max} I_{Omax}^2}{2n^2} = \frac{0.05 \times 0.3675 \times 40^2}{2 \times 7^2} = 0.3\,\text{W}. \tag{7.121}$$

The diode loss due to R_F is

$$P_{RF1} = \frac{(2D_{max} + 1) R_F I_{Omax}^2}{4}$$

$$= \frac{(2 \times 0.3675 + 1) \times 0.01325 \times 40^2}{4} = 9.196\,\text{W}, \tag{7.122}$$

the diode loss due to V_F is

$$P_{VF1} = \frac{V_F I_{Omax}}{2} = \frac{0.27 \times 40}{2} = 5.4\,\text{W}, \tag{7.123}$$

and the conduction loss in each diode is

$$P_{D1} = P_{RF1} + P_{VF1} = 9.196 + 5.4 = 14.596\,\text{W}. \tag{7.124}$$

Assuming that the ESR of the inductor is $r_L = 10\,\text{m}\Omega$,

$$P_{rL} = r_L I_{Omax}^2 = 0.01 \times 40^2 = 16\,\text{W}, \tag{7.125}$$

and the power loss in the capacitor ESR is

$$P_{rC} = \frac{r_C \Delta i_L^2}{12} = \frac{0.05 \times 0.626^2}{12} = 1.6\,\text{mW}. \tag{7.126}$$

Neglecting the MOSFET gate-drive power, the total power loss is

$$P_{LS} = 2P_{rDS} + 2P_{sw} + 2P_{rCb} + P_{rT1} + 2P_{rT2} + 2P_{D1} + P_{rL} + P_{rC}$$

$$= 2 \times 2.16 + 2 \times 0.35 + 2 \times 0.3 + 0.48 + 2 \times 3.47 + 2 \times 14.596 + 16 + 0.002$$

$$= 58.234\,\text{W}, \tag{7.127}$$

and the efficiency of the converter is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{200}{200 + 58.234} = 77.45\,\%. \tag{7.128}$$

If the peak-to-peak gate-to-source voltage is $V_{GSpp} = 14\,\text{V}$, the gate-drive power per transistor is

$$P_G = f_s Q_g V_{GSpp} = 100 \times 10^3 \times 43 \times 10^{-9} \times 14 = 60.2\,\text{mW}. \tag{7.129}$$

Figures 7.9 and 7.10 depict the efficiency η and the duty cycle D versus the dc input voltage V_I at fixed load resistances R_L. Plots of the efficiency η and the duty cycle D versus the dc load current I_O at various dc input voltages V_I are shown in Figures 7.11 and 7.12. Figures 7.13 and 7.14 illustrate the efficiency η and the duty cycle D as functions of the dc load resistance R_L at fixed dc input voltages V_I. The efficiency η decreases as I_O increases (or R_L decreases). The minimum efficiency η_{min} occurs at I_{Omax} and V_{Imin}. The duty cycle D increases as V_I decreases and I_O increases (or R_L decreases).

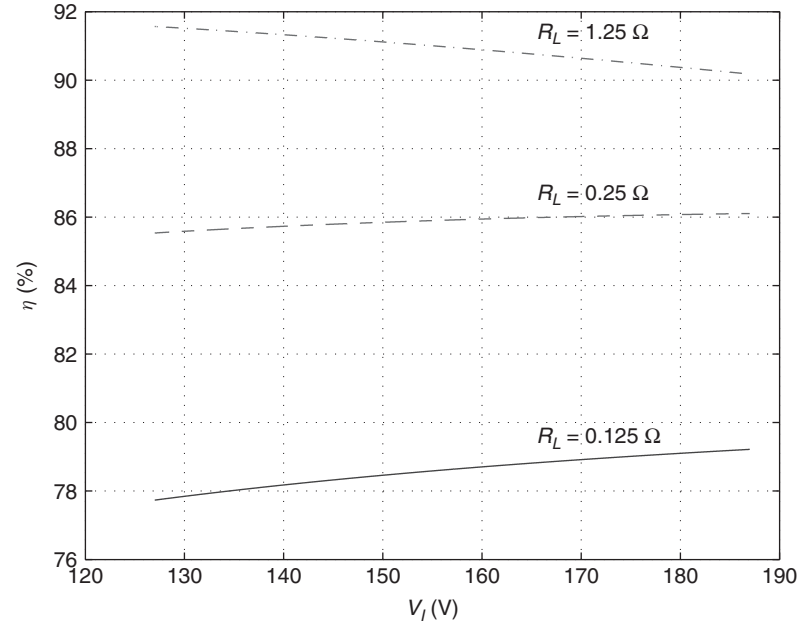


Figure 7.9 Efficiency η as a function of dc input voltage V_I at fixed load resistances R_L for the half-bridge converter in CCM.

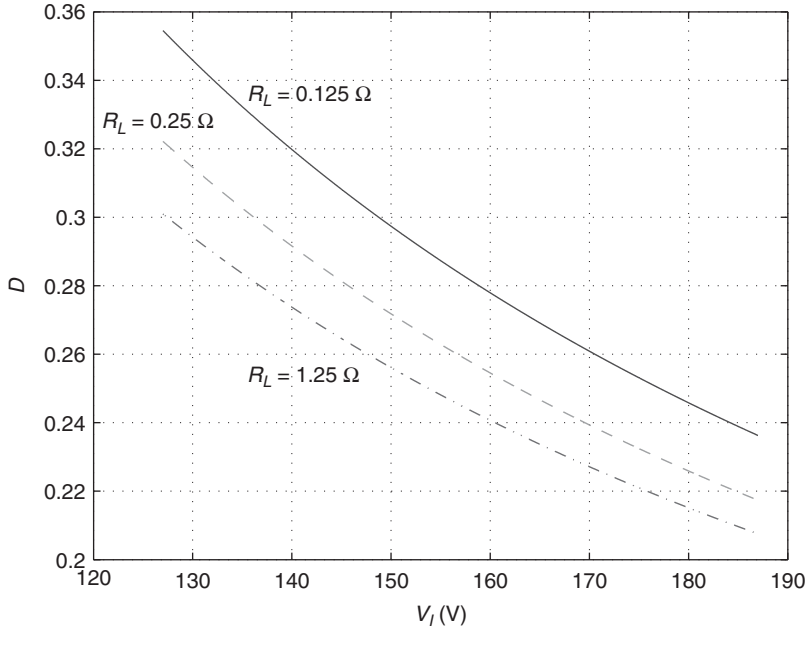


Figure 7.10 Duty cycle D as a function of dc input voltage V_I at fixed load resistances for the half-bridge converter in CCM.

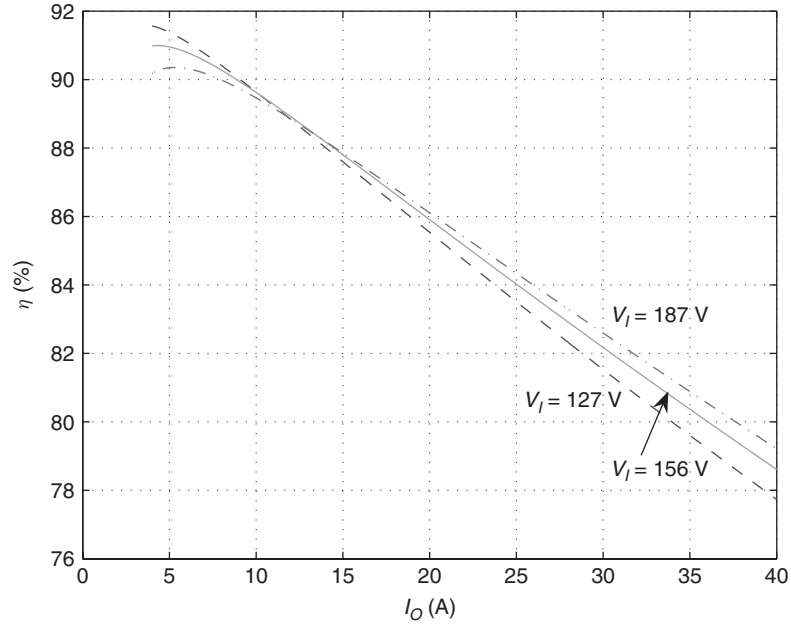


Figure 7.11 Efficiency η as a function of dc load current I_O at fixed dc input voltages V_I for the half-bridge converter in CCM.

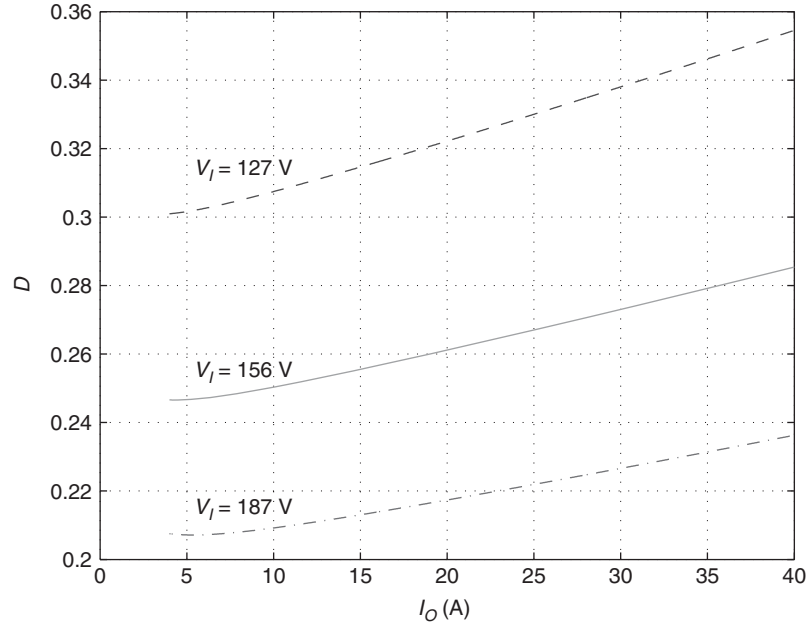


Figure 7.12 Duty cycle D as a function of dc load current I_O at fixed dc input voltages V_I for the half-bridge converter in CCM.

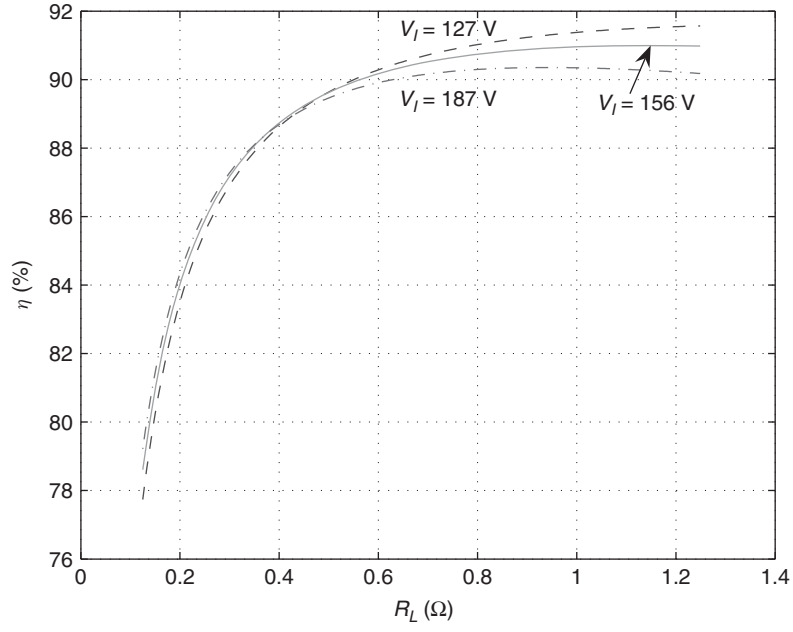


Figure 7.13 Efficiency η as a function of load resistance R_L at fixed dc input voltages V_I for the half-bridge converter in CCM.

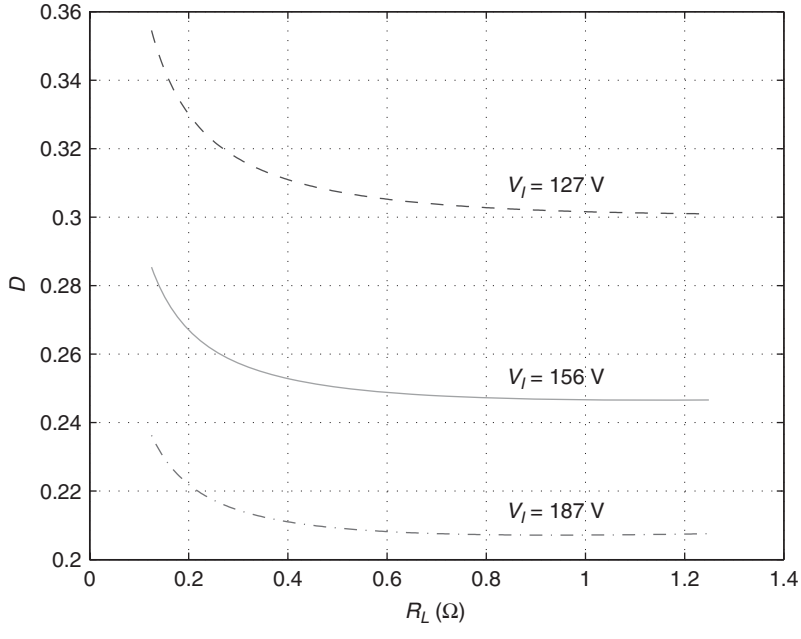


Figure 7.14 Duty cycle D as a function of load resistance R_L at fixed dc input voltages V_I for the half-bridge converter in CCM.

7.3 DC Analysis of PWM Half-bridge Converter for DCM

7.3.1 Time Interval 0 < t ≤ DT

During this time interval, the switch S_1 and the diode D_1 are ON and the switch S_2 and the diode D_2 are off. The equivalent circuit is shown in Figure 7.15(a). The switch voltage v_{S1} and the diode current i_{D2} are zero. The voltage across the switch S_2 is

$$v_{S2} = V_I. \tag{7.130}$$

The voltage across the primary and the magnetizing inductance is

$$v_1 = v_{Lm} = V_I - \frac{V_I}{2} = \frac{V_I}{2} = L_m \frac{di_{Lm}}{dt}, \tag{7.131}$$

resulting in the current through the magnetizing inductance,

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\, dt + i_{Lm}(0) = \frac{V_I}{2L_m}t + i_{Lm}(0). \tag{7.132}$$

Hence,

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(0) = \frac{V_I D}{2f_s L_m}, \tag{7.133}$$

$$i_{Lm}(0) = -\frac{\Delta i_{Lm}}{2} = -\frac{V_I D}{4f_s L_m}, \tag{7.134}$$

$$i_{Lm}(DT) = \frac{\Delta i_{Lm}}{2} = \frac{V_I D}{4f_s L_m}, \tag{7.135}$$

and

$$i_{Lm} = \frac{V_I}{2L_m}t - \frac{V_I D}{4f_s L_m}. \tag{7.136}$$

The voltages at the output of the transformer are

$$v_2 = v_3 = \frac{v_1}{n} = \frac{V_I}{2n}, \tag{7.137}$$

which gives the voltage across the diode D_2,

$$v_{D2} = -v_2 - v_3 = -\frac{V_I}{2n} - \frac{V_I}{2n} = -\frac{V_I}{n}. \tag{7.138}$$

The voltage across the inductor L is

$$v_L = \frac{V_I}{2n} - V_O = L\frac{di_L}{dt}, \quad i_L(0) = 0, \tag{7.139}$$

and the inductor and switch current is

$$i_2 = i_{D1} = i_L = \frac{1}{L}\int_0^t v_L\, dt = \frac{1}{L}\int_0^t \left(\frac{V_I}{2n} - V_O\right) dt = \frac{\dfrac{V_I}{2n} - V_O}{L}t. \tag{7.140}$$

Hence, the peak inductor current is

$$\Delta i_L = i_L(DT) = I_{DM1} = \frac{\left(\dfrac{V_I}{2n} - V_O\right)DT}{L} = \frac{\left(\dfrac{V_I}{2n} - V_O\right)D}{f_s L}. \tag{7.141}$$

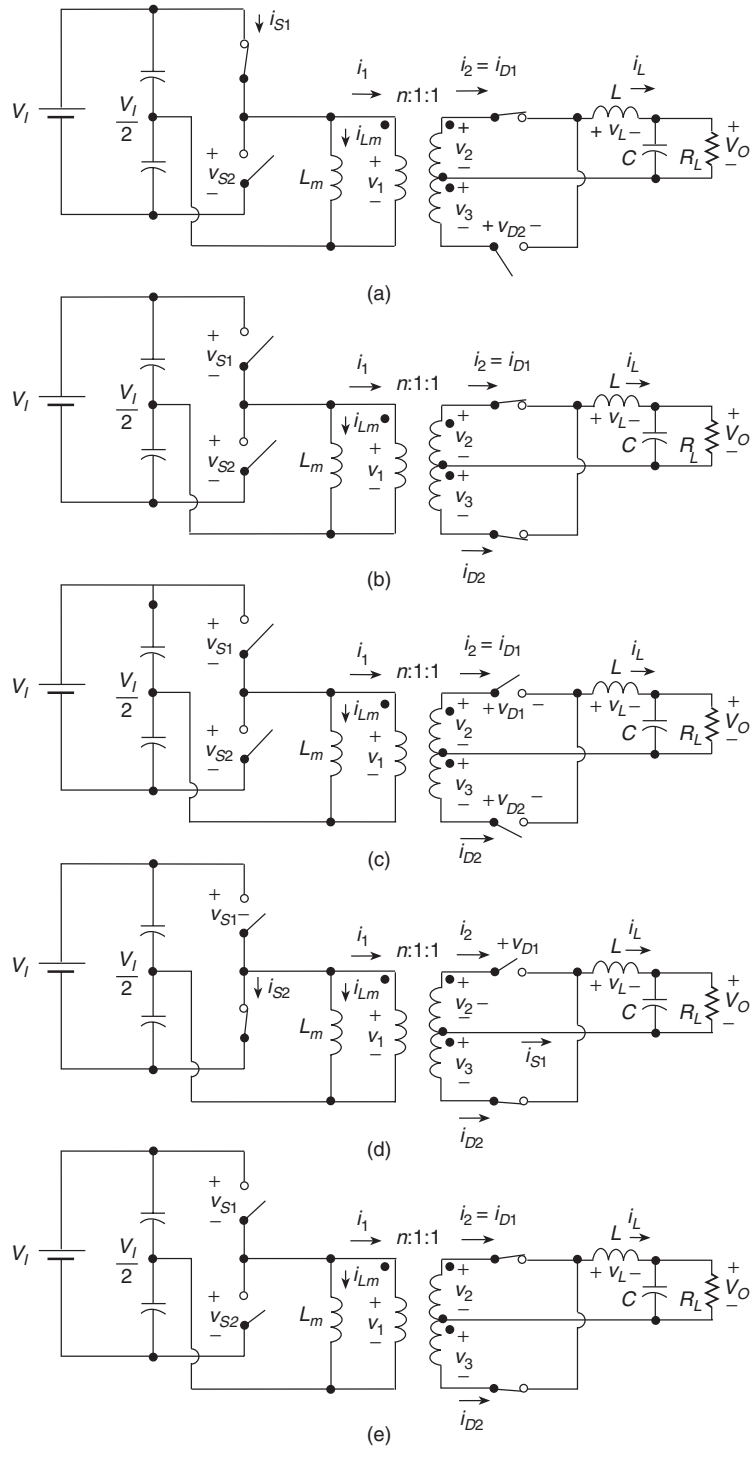


Figure 7.15 Equivalent circuit of the half-bridge converter with a transformer center-tapped rectifier for DCM. (a) For $0 < t \le DT$. (b) For $DT < t \le (D + D_1)T$. (c) For $(D + D_1)T < t \le T/2$. (d) For $T/2 < t \le T/2 + DT$. (e) For $T/2 + DT < t \le T/2 + (D + D_1)T$.

The primary current is

$$i_1 = \frac{i_2}{n} = \frac{\dfrac{V_I}{2n} - V_O}{nL} t, \tag{7.142}$$

and the current through the upper switch is

$$i_{S1} = i_1 + i_{Lm} = \frac{\dfrac{V_I}{2n} - V_O}{nL} t + \frac{V_I}{2L_m} t + i_{Lm}(0) = \frac{\dfrac{V_I}{2n} - V_O}{nL} t + \frac{V_I}{2L_m} t - \frac{V_I D}{4 f_s L_m}. \tag{7.143}$$

The waveforms in the half-bridge converter for DCM are depicted in Figure 7.16.

7.3.2 Time Interval $DT < t \le (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 7.15(b). Both switches are OFF and both diodes are ON . The voltages across the switches are

$$v_{S1} = v_{S2} = \frac{V_I}{2}, \tag{7.144}$$

resulting in the transformer voltages

$$v_1 = v_2 = v_3 = 0, \tag{7.145}$$

the voltage across the primary and the magnetizing inductance

$$v_1 = v_{Lm} = L_m \frac{di_{Lm}}{dt} = 0, \tag{7.146}$$

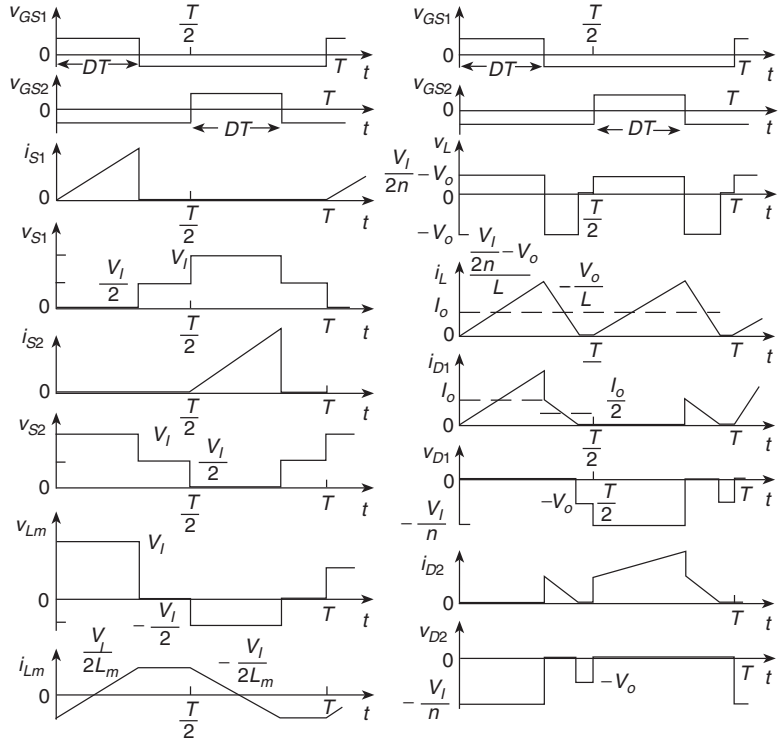


Figure 7.16 Waveforms in the half-bridge converter with a transformer center-tapped rectifier for DCM.

the current through the magnetizing inductance

$$i_{Lm} = i_{Lm}(DT) = \frac{V_I DT}{2L_m} + i_{Lm}(0) = \frac{V_I D}{2f_s L_m} - \frac{V_I D}{4f_s L_m} = \frac{V_I D}{4f_s L_m}, \tag{7.147}$$

and the current through the primary of the ideal transformer

$$i_1 = -i_{Lm} = -i_{Lm}(DT) = -\frac{V_I D}{4f_s L_m}. \tag{7.148}$$

The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{7.149}$$

and the inductor current is obtained using (7.141),

$$\begin{aligned} i_L &= \frac{1}{L}\int_{DT}^{t} v_L\, dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t} (-V_O)\, dt + i_L(DT) \\ &= -\frac{V_O}{L}(t - DT) + i_L(DT) = -\frac{V_O}{L}(t - DT) + \frac{\left(\frac{V_I}{2n} - V_O\right) DT}{L}. \end{aligned} \tag{7.150}$$

Therefore, the peak inductor current is found to be

$$\Delta i_L = i_L(DT) - i_L[(D + D_1)T] = \frac{V_O D_1 T}{L}. \tag{7.151}$$

The currents through the diodes are

$$i_{D1} = i_{D2} = \frac{i_L}{2} = -\frac{V_O}{2L}(t - DT) + i_L(DT). \tag{7.152}$$

This time interval ends when the diode currents i_{D1} and i_{D2} reach zero.

7.3.3 Time Interval $(D + D_1)T < t \leq T/2$

During this time interval, both the switches S_1 and S_2 and both diodes D_1 and D_2 are off. The equivalent circuit is shown in Figure 7.15(c). The inductor current i_L, the inductor voltage v_L, the switch currents i_{S1}, i_{S2}, and the diode currents i_{D1}, i_{D2} are zero. The voltages across the switches are

$$v_{S1} = v_{S2} = \frac{V_I}{2}, \tag{7.153}$$

the voltages across the transformer windings are

$$v_1 = v_2 = v_3 = 0, \tag{7.154}$$

and the voltages across the diodes are

$$v_{D1} = v_{D2} = -V_O. \tag{7.155}$$

The voltage across the primary and the magnetizing inductance is

$$v_1 = v_{Lm} = L_m \frac{di_{Lm}}{dt} = 0, \tag{7.156}$$

the current through the magnetizing inductance is

$$i_{Lm} = i_{Lm}(DT) = \frac{V_I DT}{2L_m} + i_{Lm}(0) = \frac{V_I D}{2f_s L_m} - \frac{V_I D}{4f_s L_m} = \frac{V_I D}{4f_s L_m}, \tag{7.157}$$

and the current through the primary of the ideal transformer is

$$i_1 = -i_{Lm} = -i_{Lm}(DT) = -\frac{V_I D}{4 f_s L_m}. \tag{7.158}$$

This time interval ends when the switch S_1 is turned on by the driver. The second half of the period is similar to the first.

7.3.4 DC Voltage Transfer Function for DCM

Referring to Figure 7.16 and using the volt-second balance,

$$\left(\frac{V_I}{2n} - V_O\right) DT = V_O D_1 T, \tag{7.159}$$

which yields

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{2n(D + D_1)}. \tag{7.160}$$

From (7.141) and (7.160), the peak-to-peak inductor current is

$$\Delta i_L = \frac{\left(\frac{V_I}{2n} - V_O\right) DT}{L} = I_{DM} = \frac{V_O D}{f_s L}\left(\frac{1}{2nM_{V\,DC}} - 1\right). \tag{7.161}$$

Using (7.160) and (7.161),

$$I_O = \frac{1}{(T/2)} \int_0^{(D+D_1)T} i_L\, dt = (D + D_1)\Delta i_L = \frac{D V_O (D + D_1)}{f_s L}\left(\frac{1}{2nM_{V\,DC}} - 1\right). \tag{7.162}$$

From (7.160), $D + D_1 = D/(2nM_{V\ DC})$. Substituting this into (7.162), one obtains

$$I_O = \frac{V_O D^2 (1 - 2nM_{V\,DC})}{4 f_s L n^2 M_{V\,DC}^2} = \frac{V_O}{R_L}, \tag{7.163}$$

which gives

$$\begin{aligned} D &= \sqrt{\frac{(2nM_{V\,DC})^2 f_s L I_O}{(1 - 2nM_{V\,DC}) V_O}} \\ &= \sqrt{\frac{(2nM_{V\,DC})^2 f_s L}{(1 - 2nM_{V\,DC}) R_L}}, \quad \text{for } D \le \frac{1}{2} - \frac{2 f_s L}{R_L} = \frac{1}{2} - \frac{2 f_s L I_O}{V_O}. \end{aligned} \tag{7.164}$$

At the CCM/DCM boundary, the dc voltage transfer function is the same as that in CCM and is given by

$$M_{V\,DCB} = \frac{D_B}{n}. \tag{7.165}$$

Substitution of this into (7.164) yields the duty cycle D_B at the boundary,

$$D_B = \frac{1}{2} - \frac{2 f_s L}{R_L} = \frac{1}{2} - \frac{2 f_s L I_O}{V_O}. \tag{7.166}$$

Figures 7.17 and 7.18 respectively show plots of D versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of $nM_{V\,DC}$ for both CCM and DCM for the lossless half-bridge converter.

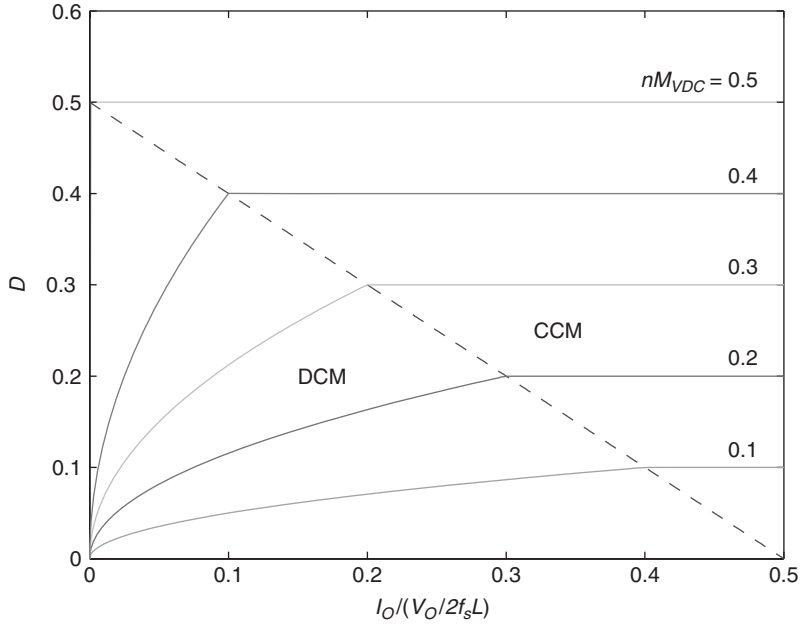


Figure 7.17 Duty cycle D versus normalized load current $I_O/(V_O/2f_sL)$ at fixed values of $nM_{V\ DC}$ for CCM and DCM for the lossless half-bridge converter.

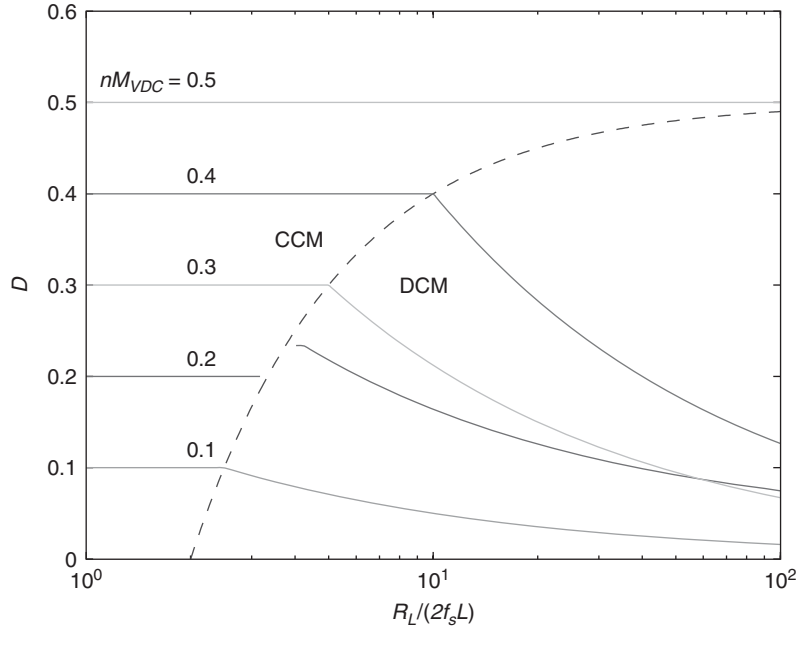


Figure 7.18 Duty cycle D versus normalized load resistance $R_L/(2f_sL)$ at fixed values of $nM_{V\ DC}$ for CCM and DCM for the lossless half-bridge converter.

Rearrangement of (7.164) leads to

$$\frac{f_s L}{D^2 R_L}(2nM_{V\,DC})^2 + 2nM_{V\,DC} - 1 = 0, \tag{7.167}$$

which yields

$$M_{V\ DC} = \frac{V_O}{V_I} = \frac{1}{n\left(1+\sqrt{1+\dfrac{4f_sL}{D^2R_L}}\right)}$$

$$= \frac{1}{n\left(1+\sqrt{1+\dfrac{4f_sLI_O}{D^2V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \tag{7.168}$$

Notice that $nM_{V\,DC}$ depends strongly on D, R_L, L, and f_s for DCM. Figures 7.19 and 7.20 respectively display $nM_{V\,DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of D for both CCM and DCM for the lossless half-bridge converter.

From (7.160) and (7.168),

$$D_1 = D\left(\frac{1}{2nM_{V\,DC}} - 1\right) = \frac{D}{2}\left(\sqrt{1+\frac{4f_sL}{D^2R_L}} - 1\right)$$

$$= \frac{D}{2}\left(\sqrt{1+\frac{4f_sLI_O}{D^2V_O}} - 1\right), \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \tag{7.169}$$

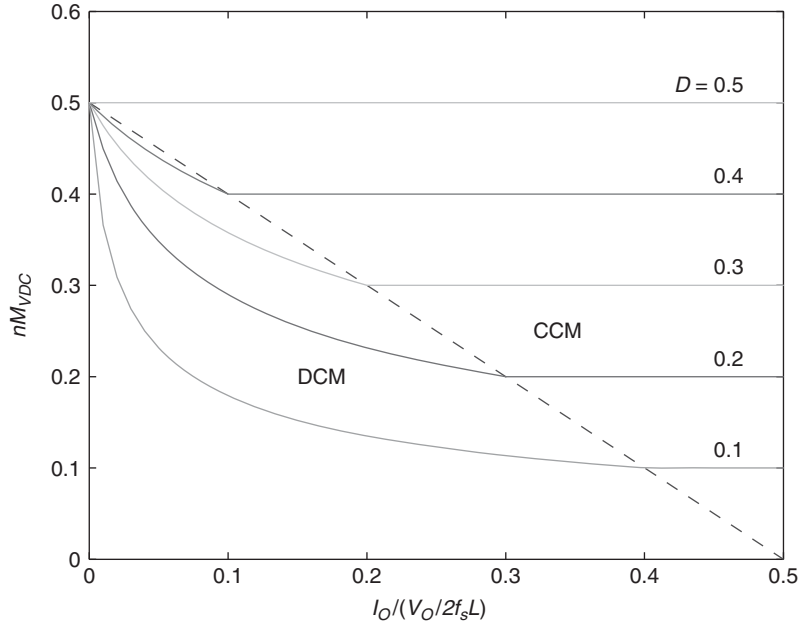


Figure 7.19 DC voltage transfer function $nM_{V\ DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ at fixed values of D for CCM and DCM for the lossless half-bridge converter.

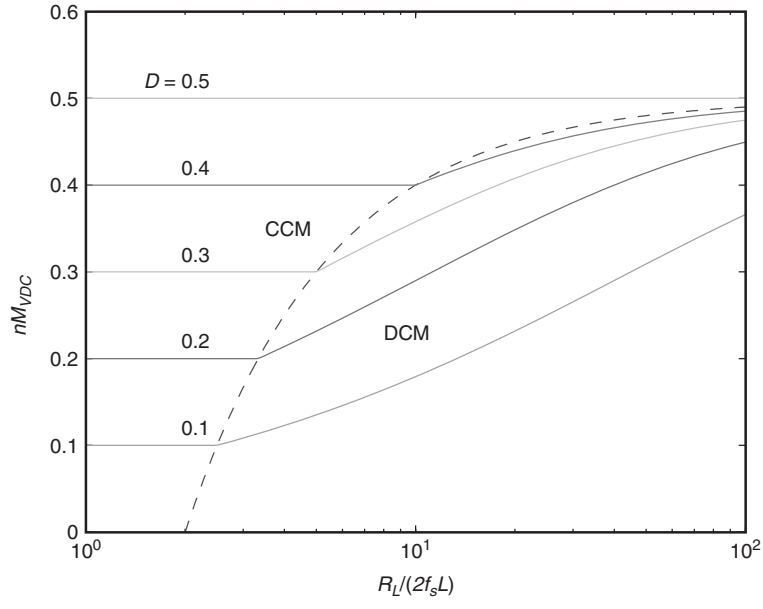


Figure 7.20 DC voltage transfer function $nM_{V\ DC}$ versus normalized load resistance $R_L/(2f_sL)$ at fixed values of D for CCM and DCM for the lossless half-bridge converter.

The dc input current is

$$I_I = \frac{1}{T}\int_0^{DT} i_I\, dt = \frac{1}{T}\int_0^{DT} \frac{\frac{V_I}{2n} - V_O}{nL} t\, dt = \frac{D^2\left(\frac{V_I}{2n} - V_O\right)}{2nf_sL}. \tag{7.170}$$

Hence, the dc input power is

$$P_I = V_I I_I = \frac{D^2 V_I\left(\frac{V_I}{2n} - V_O\right)}{2nf_sL}. \tag{7.171}$$

The output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{7.172}$$

Thus, the converter efficiency is

$$\eta = \frac{(2nM_{V\,DC})^2 f_sL}{D^2R_L(1 - 2nM_{V\,DC})}. \tag{7.173}$$

Hence, one obtains the duty cycle for the lossy half-bridge converter in DCM

$$\begin{aligned} D &= \sqrt{\frac{(2nM_{V\,DC})^2 f_sL}{\eta R_L(1 - 2nM_{V\,DC})}} \\ &= \sqrt{\frac{(2nM_{V\,DC})^2 f_sLI_O}{\eta V_O(1 - 2nM_{V\,DC})}}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}, \end{aligned} \tag{7.174}$$

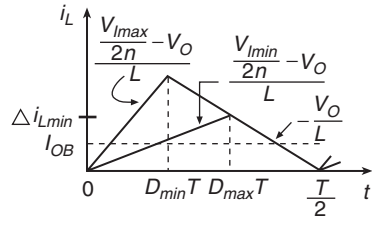


Figure 7.21 Waveforms of the inductor current at the boundary between CCM and DCM in the half-bridge converter for V_{Imin} and V_{Imax}.

and the voltage transfer function for the lossy half-bridge converter in DCM,

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{1}{n\left(1+\sqrt{1+\dfrac{4f_sL}{\eta D^2 R_L}}\right)}$$

$$= \frac{1}{n\left(1+\sqrt{1+\dfrac{4f_sLI_O}{\eta D^2 V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \quad (7.175)$$

7.3.5 Maximum Inductance for DCM

Figure 7.21 shows the waveforms of the inductor current at the CCM/DCM boundary for V_{Imin} and V_{Imax}. The minimum peak value of the inductor current at the boundary occurs for $V_I = V_{Imin}$, which corresponds to $D = D_{Bmax}$, and is described by

$$\Delta i_{Lmin} = \frac{V_O\left(\frac{1}{2} - D_{Bmax}\right)}{f_s L_{max}}. \quad (7.176)$$

The dc output current at the boundary is equal to the maximum output current given by

$$I_{Omax} = I_{OB} = \frac{\Delta i_{Lmin}}{2} = \frac{V_O\left(\frac{1}{2} - D_{Bmax}\right)}{2f_s L_{max}} = \frac{V_O}{R_{Lmin}}, \quad (7.177)$$

which yields

$$L_{max} = \frac{R_{Lmin}\left(\frac{1}{2} - D_{Bmax}\right)}{2f_s} = \frac{V_O(\frac{1}{2} - D_{Bmax})}{2f_s I_{Omax}}. \quad (7.178)$$

7.4 Summary

- The PWM half-bridge converter is a step-down or a step-up converter.
- The dc voltage transfer function of the lossless converter is $M_{V\,DC} = D/n$.
- The voltage transfer function of the half-bridge converter is proportional to the duty cycle as in the buck converter; therefore, the converter belongs to the family of buck-derived converters.
- The maximum value of the duty cycle in the half-bridge converter is theoretically 50 %. However, there must be a mandatory dead time when neither transistor conducts to avoid

cross-conduction. This implies that the duty cycle of the gate-to-source voltages should be slightly lower than 50 %.

- The transformer is not required to store energy in the half-bridge converter.
- The transformer core utilization is excellent in the half-bridge converter because the dc current through the primary winding is zero and the primary is driven in both directions.
- The voltage stress of the switches is low, equal to V_{Imax}; therefore, the converter is used in off-line power supplies.
- The voltage stresses of the diodes are V_{Imax}/n for the transformer center-tapped rectifier and the half-wave rectifier, and $V_{Imax}/(2n)$ for the bridge rectifier.
- The frequency of the waveforms in the output filter is twice the frequency of the MOSFET drivers.
- The duty cycle D of the lossy converter is greater than that of the lossless converter at the same value of the dc voltage transfer function.
- The peak-to-peak value of the inductor current ripple Δi_L is independent of the dc load current for CCM.
- The peak-to-peak value of the current through the filter capacitor C is relatively low; it is equal to the peak-to-peak inductor current ripple Δi_L.
- If the capacitance of the filter capacitor is sufficiently large, the output ripple voltage is determined only by the filter capacitor ESR and is independent of the filter capacitance.
- The minimum value of the inductor is determined by the CCM/DCM boundary, ripple voltage, or ac losses in the inductor and/or the filter capacitor.
- The input current is pulsating. However, an input LC filter can be added at the converter input to obtain a nonpulsating input current waveform.
- The corner frequency of the output filter $f_o = 1/(2\pi\sqrt{LC})$ is independent of the load resistance.
- It is relatively difficult to drive the upper transistor because the gate is not referenced to ground. Therefore, a transformer or an optocoupler is required to drive the circuit.

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7.6 Review Questions

7.1 Give an expression for the dc voltage transfer function of the lossless half-bridge converter.

7.2 What is the maximum value of the duty cycle of the half-bridge converter?

7.3 What happens when the duty cycle is too large in the half-bridge converter?

7.4 What is cross-conduction? How would you prevent it?

7.5 Is the transformer required to store energy in the half-bridge converter?

7.6 What is the dc component of the current through the primary of the transformer in the half-bridge converter?

7.7 What is the total dc magnetic flux caused by the dc components of the diode currents in the center-tapped, bridge, and half-wave rectifiers?

7.8 Is the input current of the basic half-bridge converter pulsating?

7.9 What are the voltage stresses of the switches in the half-bridge converter?

7.10 What are the voltage stresses of the diodes in the center-tapped, bridge, and half-wave rectifiers?

7.11 How can the circuit be changed to obtain a nonpulsating input current in the half-bridge converter?

7.12 Is the upper transistor driven with respect to ground in the half-bridge converter?

7.13 How is the dc voltage transfer function $M_{V\,DC}$ related to the duty cycle D of the lossless half-bridge converter in CCM?

7.14 Is the duty cycle D of the lossy half-bridge converter less than or greater than that for the lossless converter at a given value of $M_{V\,DC}$ in CCM?

7.15 Is the corner frequency of the output filter dependent on the load resistance?

7.17 How can the circuit of the half-bridge converter be modified to eliminate one blocking capacitor?

7.18 What are the best applications for a half-bridge converter with a transformer center-tapped rectifier?

7.19 What are the best applications for a half-bridge converter with a bridge rectifier?

7.20 Why is dead time required in the gate-to-drive voltages of the half-bridge converter?

7.21 Is transformer core utilization good in the half-bridge converter?

7.22 Is the half-bridge converter a good candidate for applications in off-line power supplies?

7.23 Sketch the voltage waveform across the primary winding in the half-bridge converter.

7.7 Problems

7.1 Derive an expression for the voltage stress of the diodes in the half-bridge PWM converter with a bridge rectifier.

7.2 The input voltage of a half-bridge PWM converter operating in CCM is the European single-phase rectified line voltage 220 Vrms $\pm$ 10 % and $V_O = 12$ V. Find the transformer turns ratio n, the minimum duty cycle D_{min}, and the maximum duty cycle D_{max}.

7.3 A half-bridge converter operating in CCM has $V_{Imax} = 342$ V and $n = 9$. Find the voltage stresses of the switches and the diodes.

7.4 A half-bridge converter has $V_{Imin} = 280$ V, $V_{Imax} = 342$ V, $V_O = 12$ V, $I_O = 1$ to 20 A, $f_s = 50$ kHz and $D_{min} = 0.3424$. Find the minimum inductance required to maintain the converter operation in CCM.

7.5 A half-bridge converter has $V_{Imin} = 280$ V, $V_{Imax} = 342$ V, $V_O = 12$ V, $I_O = 1$ to 20 A, $L = 25\,\mu$H, $n = 9$, $D_{min} = 0.3424$, $D_{max} = 0.4193$, $f_s = 50$ kHz, and $V_r/V_O < 2\,\%$. Find the minimum filter capacitance and the corner frequency of the output filter.

7.6 A half-bridge converter has $V_{Imin} = 280$ V, $V_{Imax} = 342$ V, $V_O = 12$ V, $I_O = 1$ to 20 A, $L = 25\,\mu$H, $n = 9$, $\Delta i_{Lmax} = 1.513$, and $f_s = 50$ kHz. Determine the minimum magnetizing inductance at which its peak-to-peak current is less than 10 % of the maximum peak current of the ideal transformer primary.

7.7 A half-bridge converter has $V_{Imin} = 280$ V, $V_{Imax} = 342$ V, $V_O = 12$ V, $I_O = 0$ to 20 A, $f_s = 50$ kHz, $n = 9$, and $D_{min} = 0.3424$. Find the maximum inductance required to maintain operation of the converter in DCM.

7.8 Design a half-bridge converter operating in CCM to met the following specifications: V_I is the single-phase rectified European line voltage with $V_{rms} = 220$ V $\pm$ 10 %,

$V_O = 5\,\text{V}$, $I_{Omin} = 2\,\text{A}$, $I_{Omax} = 20\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Assume $r_{DS} = 1\,\Omega$, $r_{T1} = 150\,\text{m}\Omega$, $r_{T2} = r_{T3} = 40\,\text{m}\Omega$, $r_L = 9\,\text{m}\Omega$, $r_C = 35\,\text{m}\Omega$, $r_{Cb} = 350\,\text{m}\Omega$, $R_F = 10\,\text{m}\Omega$, $V_F = 0.3\,\text{V}$, and $C_o = 80\,\text{pF}$. Assume initially that the converter efficiency is $\eta = 85\,\%$.

7.9 Design a half-bridge converter whose V_I is the single-phase rectified voltage $220\,\text{Vrms} \pm 10\,\%$, $V_O = 5\,\text{V}$, $I_O = 1$ to $10\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Find L, C, L_m, r_C, n, I_{SMmax}, V_{SMmax}, I_{DMmax}, and V_{SMmax}.

8

Full-bridge PWM DC–DC Converter

8.1 Introduction

The full-bridge PWM converter [1]–[22] contains two switching legs. Therefore, it draws two current pulses from the input voltage source per cycle of the transistor switching frequency and is capable of delivering more output power than the half-bridge converter. The voltage stresses of the switches are low and equal to the dc input voltage V_I. For this reason, the full-bridge converter is used in off-line high-power supplies. This topology of the converter offers the highest power levels, from 500 W to 5 kW. The core is excited in both directions and is relatively small. Applications of the full-bridge converter include telecommunications and aerospace power supplies. The converter belongs to the family of buck-derived converters. This chapter describes, analyzes, and gives a design example of the full-bridge converter.

8.2 DC Analysis of PWM Full-bridge Converter for CCM

8.2.1 Circuit Description

A PWM full-bridge dc–dc converter circuit is depicted in Figure 8.1(a). It is composed of a PWM inverter and a PWM rectifier. The inverter consists of a transformer and four power MOSFETs used as controllable switches S_1, S_2, S_3, and S_4. The transistors in each switching leg are driven by nonoverlapping voltages that are out of phase by 180°. The maximum duty cycle of the gate-to-source voltages is slightly less than 50 %. The waveforms of the gate-to-source voltages should be nonoverlapping to avoid cross-conduction. The switching part

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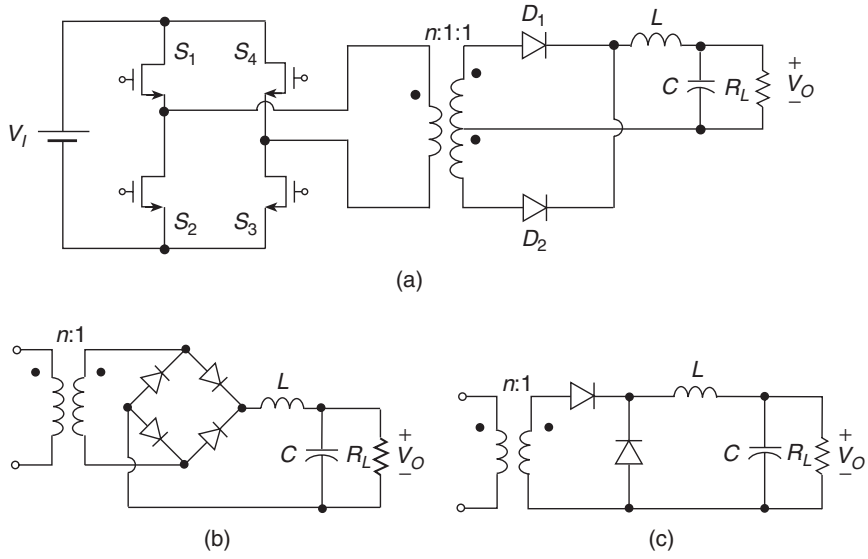


Figure 8.1 Full-bridge converter. (a) With a transformer center-tapped rectifier. (b) With a full-bridge rectifier. (c) With a half-wave rectifier.

of the converter has a totem pole arrangement. Therefore, it is not easy to drive the upper transistors because their gates are not driven with respect to ground. Pulse transformers can be used to drive the upper transistors. The lower transistors can also be driven by pulse transformers. Pulse transformers driving transistors S_1 and S_3 may be connected to one output of a control circuit. Similarly, pulse transformers driving transistors S_2 and S_4 may be connected to the second output of a control circuit. The two outputs of a control circuit provide nonoverlapping voltages out of phase by 180°. The isolation transformer is not required to store energy. Its magnetizing inductance L_m should be large enough to reduce the current through this inductance. On the other hand, if the magnetizing inductance is too large, it requires a large number of turns and is physically large. Ideally, the dc component of the current through the magnetizing inductance is zero. A coupling capacitor may be added in series with the primary winding to achieve zero dc component of the current through the magnetizing inductance and thus remove an imbalance of the magnetic core. The full-bridge converter is well suited to high-power applications, usually from 0.5 kW to several kilowatts. It offers the highest power levels among all converters. In very high-power applications, insulated gate bipolar transistors thyristors, or MOSFET-controlled thyristors are used as switching devices. In addition, two or more power switching devices may be connected in parallel to increase current capability of every switch and output power levels.

Three topologies can be used for the full-bridge converter: with a transformer center-tapped rectifier, with a full-bridge rectifier, or with a half-wave rectifier. The transformer center-tapped rectifier consists of two diodes D_1 and D_2, an inductor L, a filter capacitor C, and a load resistor R_L. An insulated gate bipolar transistors or MOSFET-controlled thyristors can also be used. This rectifier is most suitable for low output voltage applications because only one diode conducts, when two switches are ON. Schottky diodes or low on-resistance power MOSFETs can be used as rectifying devices. The voltage stress of the diodes is $2V_I/n$, which is higher than that in the bridge rectifier. Therefore, the transformer center-tapped rectifier is not suitable for high-voltage applications.

The bridge rectifier is suited for high output voltage applications because the voltage stress of the diodes is V_I/n, which is half of the transformer center-tapped rectifier. This rectifier is not suitable for low-voltage applications because two diodes conduct when two switches are ON, and the total forward voltage across the two diodes may become comparable with the output voltage, resulting in low efficiency.

8.2.2 Assumptions

The analysis of the full-bridge PWM converter with a transformer center-tapped rectifier shown in Figure 8.1(a) is based upon the following assumptions:

1. The power MOSFETs and the diodes are ideal switches.
2. The transistor and diode capacitances and lead inductances are zero.
3. The transformer is modeled by an ideal transformer and its magnetizing inductance L_m. Leakage inductances and stray capacitances are neglected.
4. Passive components are linear, time-invariant, and frequency-independent.
5. The output impedance of the input voltage source V_I is zero for both dc and ac components.

8.2.3 Time Interval $0 < t \leq DT$

During the time interval $0 < t \leq DT$, the switches S_1 and S_3 as well as the diode D_1 are ON, whereas the switches S_2 and S_4 as well as the diode D_2 are OFF. An ideal equivalent circuit for this time interval is shown in Figure 8.2(a). The voltages across the switches S_2 and S_4 are

$$v_{S2} = v_{S4} = V_I. \tag{8.1}$$

The voltage across the primary winding and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = V_I = L_m \frac{di_{Lm}}{dt}. \tag{8.2}$$

Hence, the current through the magnetizing inductance L_m is

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt + i_{Lm}(0) = \frac{1}{L_m}\int_0^t V_I\,dt + i_{Lm}(0) = \frac{V_I}{L_m}t + i_{Lm}(0), \tag{8.3}$$

where $i_{Lm}(0)$ is the initial current through the magnetizing inductance L_m at $t = 0$. This current is negative. The peak-to-peak ripple current of the magnetizing inductance is

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(0) = \frac{V_I DT}{L_m} = \frac{V_I D}{f_s L_m}, \tag{8.4}$$

the current through the magnetizing inductance at $t = 0$ is

$$i_{Lm}(0) = -\frac{\Delta i_{Lm}}{2} = -\frac{V_I D}{2 f_s L_m}, \tag{8.5}$$

and the current through the magnetizing inductance at $t = DT$ is

$$i_{Lm}(DT) = \frac{\Delta i_{Lm}}{2} = \frac{V_I D}{2 f_s L_m}. \tag{8.6}$$

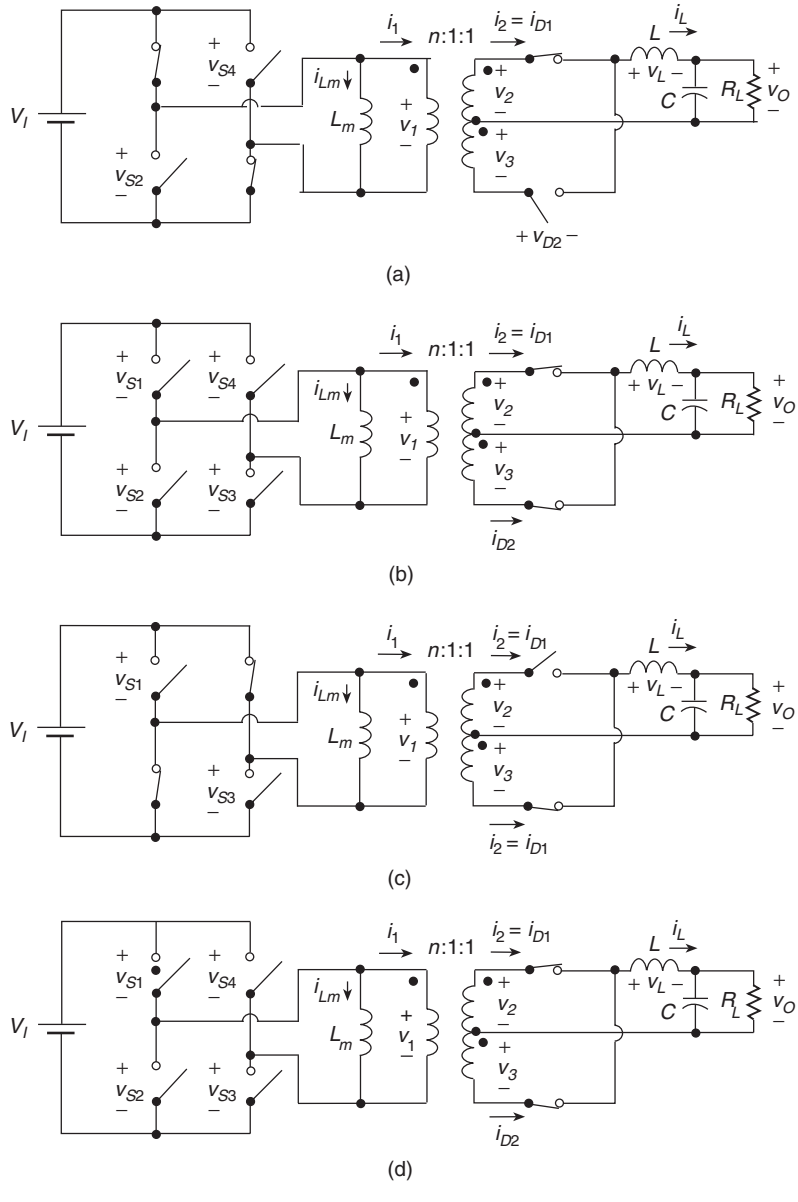


Figure 8.2 Equivalent circuit of the full-bridge converter with a transformer center-tapped rectifier for CCM. (a) For $0 < t \le DT$. (b) For $DT < t \le T/2$. (c) For $T/2 < t \le T/2 + DT$. (d) For $T/2 + DT < t \le T$.

The maximum value of the peak-to-peak ripple current of the magnetizing inductance is

$$\Delta i_{Lm(max)} = \frac{D_{min} V_{Imax}}{f_s L_{m(min)}}, \tag{8.7}$$

which gives the minimum magnetizing inductance

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{f_s \Delta i_{Lm(max)}}. \tag{8.8}$$

The voltages across the transformer secondary windings are

$$v_2 = v_3 = \frac{v_1}{n} = \frac{V_I}{n}. \tag{8.9}$$

The voltage across the diode D_2 is

$$v_{D2} = -v_2 - v_3 = -\frac{V_I}{n} - \frac{V_I}{n} = -\frac{2V_I}{n}. \tag{8.10}$$

Since $v_{D2} < 0$, the diode D_2 is OFF. The voltage across the inductor L is given by

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}, \tag{8.11}$$

resulting in the current through the inductor L

$$\begin{aligned} i_2 = i_{D1} = i_L &= \frac{1}{L}\int_0^t v_L\,dt + i_L(0) = \frac{1}{L}\int_0^t \left(\frac{V_I}{n} - V_O\right)dt + i_L(0) \\ &= \frac{\dfrac{V_I}{n} - V_O}{L}t + i_L(0), \end{aligned} \tag{8.12}$$

where $i_L(0)$ is the initial current in the inductor L at time $t = 0$. The peak inductor current becomes

$$i_L(DT) = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} + i_L(0), \tag{8.13}$$

and the peak-to-peak value of the ripple current through the inductor L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} = \frac{V_O(0.5 - D)}{f_s L}, \tag{8.14}$$

where $V_I = nV_O/(2D)$ as will shortly be shown. The maximum value of the peak-to-peak ripple current through the inductor L is

$$\Delta i_{Lmax} = \frac{V_O(0.5 - D_{min})}{f_s L}. \tag{8.15}$$

The current through the primary winding of the ideal transformer is

$$i_1 = \frac{i_2}{n} = \frac{i_L}{n} = \frac{\dfrac{V_I}{n} - V_O}{nL}t + \frac{i_L(0)}{n}, \tag{8.16}$$

and the current through the switch is

$$i_{S1} = i_{S3} = i_1 + i_{Lm} = \frac{\dfrac{V_I}{n} - V_O}{nL}t + \frac{i_L(0)}{n} + \frac{V_I}{L_m}t + i_{Lm}(0). \tag{8.17}$$

Figure 8.3 shows current and voltage waveforms in the full-bridge converter with a transformer center-tapped rectifier for CCM.

8.2.4 Time Interval $DT < t \leq T/2$

Figure 8.2(b) shows an equivalent circuit of the converter for the time interval $DT < t \leq T/2$, during which all four switches are OFF and both diodes are ON. Assuming that the

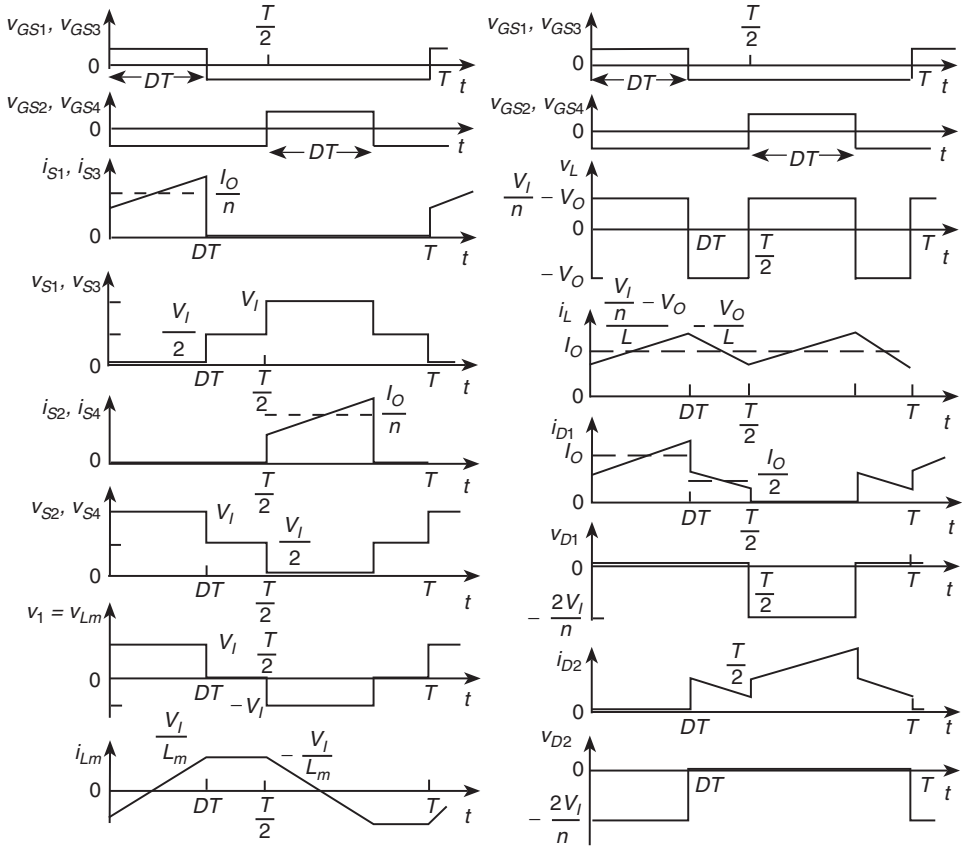


Figure 8.3 Waveforms of the full-bridge converter with a transformer center-tapped rectifier for CCM.

off-resistances of the switches are same, the voltages across all the switches are

$$v_{S1} = v_{S2} = v_{S3} = v_{S4} = \frac{V_I}{2}. \tag{8.18}$$

Therefore, the voltage across the primary winding and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = L_m \frac{di_{Lm}}{dt} = 0, \tag{8.19}$$

which gives the current through the magnetizing inductance,

$$i_{Lm} = i_{Lm}(DT) = \frac{V_I D}{2 f_s L_m}, \tag{8.20}$$

and the current through the primary winding of the ideal transformer,

$$i_1 = -i_{Lm} = -i_{Lm}(DT) = -\frac{V_I D}{2 f_s L_m}. \tag{8.21}$$

The voltages at the transformer outputs are

$$v_2 = v_3 = 0. \tag{8.22}$$

The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{8.23}$$

and the inductor current is

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L\,dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT). \tag{8.24}$$

Assuming that the rectifier circuit is symmetrical, the inductor current is divided equally between the diodes,

$$i_{D1} = i_{D2} = \frac{i_L}{2} = -\frac{V_O}{2L}(t - DT) + \frac{i_L(DT)}{2}. \tag{8.25}$$

8.2.5 Time Interval $T/2 < t \leq T/2 + DT$

Figure 8.2(c) shows an equivalent circuit of the converter for the time interval $T/2 < t \leq T/2 + DT$, during which the switches S_1 and S_3 as well as diode D_1 are OFF, and the switches S_2 and S_4 as well as as well as diode D_2 are ON. The voltages across the switches S_1 and S_3 are

$$v_{S1} = v_{S3} = V_I, \tag{8.26}$$

and the voltage across the primary winding and the magnetizing inductance L_m is

$$v_1 = v_{Lm} = -V_I = L_m\frac{di_{Lm}}{dt}. \tag{8.27}$$

The current through the magnetizing inductance is

$$\begin{aligned} i_{Lm} &= \frac{1}{L_m}\int_{T/2}^{t} v_{Lm}\,dt + i_{Lm}\left(\frac{T}{2}\right) \\ &= -\frac{V_I}{L_m}\left(t - \frac{T}{2}\right) + i_{Lm}\left(\frac{T}{2}\right) \\ &= -\frac{V_I}{L_m}\left(t - \frac{T}{2}\right) + \frac{V_I D}{2f_s L_m}, \end{aligned} \tag{8.28}$$

and the voltages at the output of the transformer are

$$v_2 = v_3 = \frac{v_1}{n} = -\frac{V_I}{n}. \tag{8.29}$$

The voltage across the diode D_1 is

$$v_{D1} = v_2 + v_3 = -\frac{2V_I}{n}. \tag{8.30}$$

The voltage across the inductor is expressed by

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}. \tag{8.31}$$

Hence, the current through the bottom transformer winding, the diode D_2, and the inductor L is

$$i_3 = -i_{D2} = i_L = \frac{1}{L}\int_{T/2}^{t} v_L\,dt + i_L\left(\frac{T}{2}\right) = \frac{\dfrac{V_I}{n} - V_O}{L}\left(t - \frac{T}{2}\right) + i_L\left(\frac{T}{2}\right). \tag{8.32}$$

Hence, the current through the primary winding is

$$i_1 = \frac{i_3}{n} = -\frac{i_{D2}}{n} = -\frac{\dfrac{V_I}{n} - V_O}{nL}\left(t - \frac{T}{2}\right) - \frac{i_L\left(\dfrac{T}{2}\right)}{n}. \tag{8.33}$$

The current through the switch S_2 is

$$i_{S2} = -i_1 - i_{Lm} = \frac{\frac{V_I}{n} - V_O}{nL}\left(t - \frac{T}{2}\right) + \frac{i_L\left(\frac{T}{2}\right)}{n} + \frac{V_I}{L_m}\left(t - \frac{T}{2}\right) - i_{Lm}\left(\frac{T}{2}\right)$$

$$= \frac{\frac{V_I}{n} - V_O}{nL}\left(t - \frac{T}{2}\right) + \frac{i_L\left(\frac{T}{2}\right)}{n} + \frac{V_I}{L_m}\left(t - \frac{T}{2}\right) - \frac{V_I D}{2 f_s L_m}. \tag{8.34}$$

8.2.6 Time Interval $T/2 + DT < t \leq T$

An equivalent circuit of the converter for the time interval $T/2 + DT < t \leq T$ is shown in Figure 8.2(d). All switches are OFF and both diodes are ON during this time interval. The equivalent circuit of Figure 8.2(d) is the same as that of Figure 8.2(b). Consequently, the analysis of the converter is the same as in Section 8.2.4.

8.2.7 Device Stresses

The maximum peak value of the voltage across each switch is

$$V_{SMmax} = V_{Imax}, \tag{8.35}$$

and the maximum peak value of the current through each switch is

$$I_{SMmax} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} + \frac{\Delta i_{Lm(max)}}{2}. \tag{8.36}$$

The maximum peak value of the voltage across each diode of the transformer center-tapped rectifier is

$$V_{DMmax} = \frac{2V_{Imax}}{n}, \tag{8.37}$$

and the maximum peak value of the voltage across each diode of the full-bridge rectifier is

$$V_{DMmax} = \frac{V_{Imax}}{n}. \tag{8.38}$$

The average value of the inductor current is equal to the dc output current I_O. Hence, the maximum peak value of each diode is given by

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2}. \tag{8.39}$$

8.2.8 DC Voltage Transfer Function of Lossless Full-wave Converter for CCM

Referring to Figure 8.3,

$$\left(\frac{V_I}{n} - V_O\right) DT = V_O\left(\frac{1}{2} - D\right) T, \tag{8.40}$$

resulting in the dc voltage transfer function of the lossless converter,

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2D}{n}, \qquad \text{for } D \le 0.5. \tag{8.41}$$

The range of $M_{V\,DC}$ is

$$0 \le M_{V\,DC} \le \frac{1}{n}. \tag{8.42}$$

For the lossless converter, the output voltage V_O is independent of the load resistance R_L and depends only on the dc input voltage V_I. The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = \frac{2V_I}{n}. \tag{8.43}$$

The dc current transfer function is

$$M_{IDC} \equiv \frac{I_O}{I_I} = \frac{n}{2D}. \tag{8.44}$$

As D is increased from 0 to 0.5, M_{IDC} decreases from ∞ to n.

From (8.41), one obtains $V_I = nV_O/(2D)$. Substitution of V_I into (8.14) gives

$$\Delta i_L = \frac{V_O(\frac{1}{2} - D)}{f_s L}. \tag{8.45}$$

From (8.35), (8.36), and (8.41), $I_O/I_{SM} \approx n$ and $V_O/V_{SM} = V_O/V_I = 2D/n$. Hence, the switch utilization in the full-bridge converter, characterized by the output-power capability, is given by

$$c_p \equiv \frac{P_O}{V_{SM}I_{SM}} = \frac{V_O I_O}{V_{SM}I_{SM}} \approx \frac{nV_O}{V_{SM}} = \frac{nV_O}{V_I} = 2D. \tag{8.46}$$

As D is increased from 0 to 0.5, c_p increases from 0 to 1.

8.2.9 Boundary between CCM and DCM

The waveform of the inductor current at the CCM/DCM boundary is shown in Figure 8.4 and is given by

$$i_L = -\frac{V_O}{L}(t - DT) + i_L(DT), \qquad \text{for } DT < t \le \frac{T}{2}, \tag{8.47}$$

which leads to

$$i_L\left(\frac{T}{2}\right) = -\frac{V_O T\left(\frac{1}{2} - D\right)}{L} + i_L(DT) = 0. \tag{8.48}$$

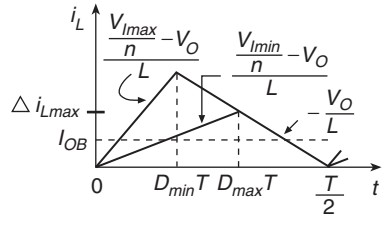


Figure 8.4 Waveforms of the inductor current in the full-bridge converter at the CCM/DCM boundary.

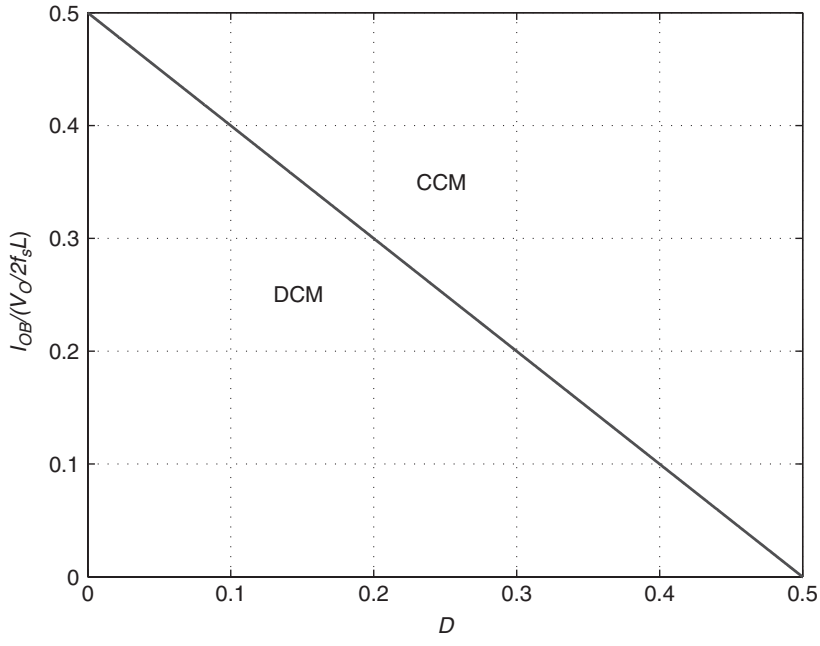


Figure 8.5 Normalized load current $I_{OB}/(V_O/2f_sL)$ as a function of duty cycle D at the CCM/DCM boundary for the full-bridge converter.

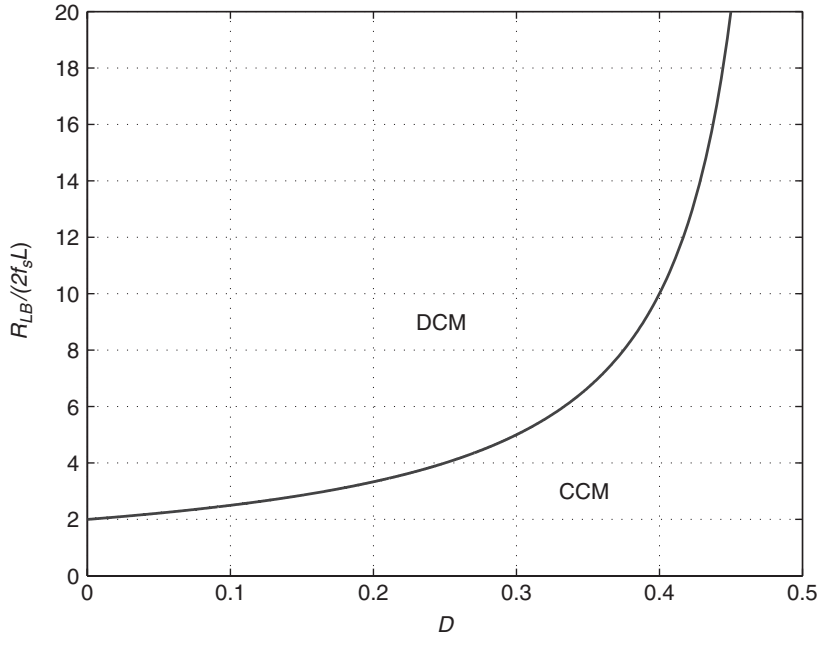


Figure 8.6 Normalized load resistance $R_{LB}/(2f_sL)$ as a function of duty cycle D at the CCM/DCM boundary for the full-bridge converter.

Hence, one obtains the maximum peak value of the inductor current at the CCM/DCM boundary,

$$\Delta i_{Lmax} = i_{Lmax}(DT) = \frac{V_O T\left(\frac{1}{2} - D_{min}\right)}{L_{min}} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{f_s L_{min}}. \tag{8.49}$$

The dc output current at the boundary is

$$I_{OB} = I_{Omin} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s L_{min}} = \frac{V_O}{R_{Lmax}}. \tag{8.50}$$

Hence, the load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{0.5 - D}. \tag{8.51}$$

The minimum value of the inductance L required to maintain the converter operation in CCM is then expressed by

$$L_{min} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s I_{Omin}} = \frac{R_{Lmax}\left(\frac{1}{2} - D_{min}\right)}{2f_s} = \frac{D_{min}\left(\frac{V_{Imax}}{n} - V_O\right)}{2f_s I_{Omin}}. \tag{8.52}$$

Figure 8.5 and 8.6 respectively show the normalized load current $I_{OB}/(V_O/2f_sL) = 0.5 - D$ and load resistance $R_{LB}/(2f_sL) = 1/(0.5 - D)$ at the CCM/DCM boundary as functions of the duty cycle D.

8.2.10 Ripple Voltage in Full-bridge Converter for CCM

An analysis similar to that of the buck converter reveals that the peak-to-peak output ripple voltage is equal to the peak-to-peak ripple voltage across the ESR if

$$C \geq C_{min} = \max\left\{\frac{D_{max}}{2r_C f_s}, \frac{0.5 - D_{min}}{2r_C f_s}\right\}, \tag{8.53}$$

where $D_{max} \leq 0.5$. This condition is satisfied at any duty cycle $D \leq 0.5$ if

$$C \geq C_{min} = \frac{1}{4r_C f_s}. \tag{8.54}$$

If condition (8.53) is met, the peak-to-peak output ripple voltage V_r is independent of the filter capacitance C and is determined by the ripple voltage across the ESR. Thus,

$$V_r = r_C \Delta i_{Lmax} = \frac{r_C V_O(0.5 - D_{min})}{f_s L}. \tag{8.55}$$

If condition (8.53) is not met, the peak-to-peak output ripple voltage is determined by both the voltage across the capacitance and the ESR. The maximum change in charge stored in the capacitor is

$$\Delta Q = \frac{1}{2} \times \frac{T}{4} \times \frac{\Delta i_{Lmax}}{2} = \frac{T \Delta i_{Lmax}}{16} = \frac{\Delta i_{Lmax}}{16 f_s}. \tag{8.56}$$

Hence,

$$V_{Cpp} = \frac{\Delta Q}{C} = \frac{\Delta i_{Lmax}}{16 f_s C_{min}} = \frac{V_O(0.5 - D_{min})}{16 f_s^2 L C_{min}} = \frac{(0.5 - D_{min}) f_o^2}{16 f_s^2}, \tag{8.57}$$

which gives

$$C_{min} = \frac{\Delta i_{Lmax}}{16 f_s V_{Cpp}} = \frac{V_O(0.5 - D_{min})}{16 f_s^2 L V_{Cpp}}. \tag{8.58}$$

The ripple voltage across the ESR is

$$V_{rcpp} = r_C \, \Delta i_{Lmax} = \frac{r_C V_O(0.5 - D_{min})}{f_s L}. \tag{8.59}$$

The output ripple voltage is approximately equal to

$$V_r \approx V_{Cpp} + V_{rcpp} = \frac{V_O(0.5 - D_{min})}{16 f_s^2 LC} + \frac{r_C V_O(0.5 - D_{min})}{f_s L}. \tag{8.60}$$

8.2.11 Power Losses and Efficiency of Full-bridge Converter for CCM

Figure 8.7 depicts an equivalent circuit of the full-bridge converter with parasitic resistances, where r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The conduction losses will be determined by assuming that the ripple of the inductor current is zero. Therefore, the inductor current can be approximated as

$$i_L \approx I_O. \tag{8.61}$$

Assume that the peak value of the magnetizing current i_{Lm} is much lower than the peak value of the switch current. The current through the switches S_1 and S_3 can be expressed by

$$i_{S1} = i_{S3} = \begin{cases} \dfrac{I_O}{n}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T/2. \end{cases} \tag{8.62}$$

The rms value of switches S_1 and S_3 is

$$I_{S1rms} = I_{S3rms} = \sqrt{\frac{1}{T}\int_0^T i_{S1}^2 \, dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{D}}{n}. \tag{8.63}$$

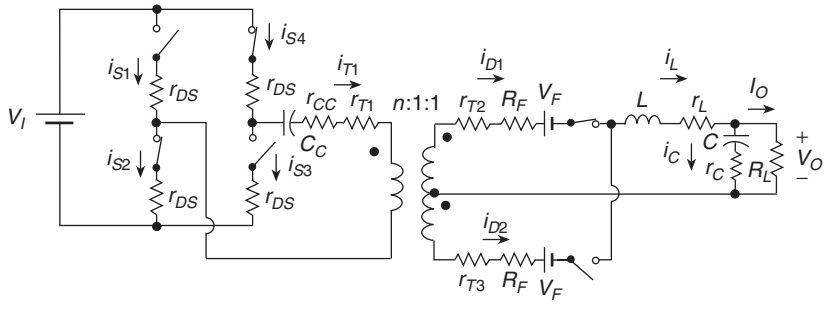


Figure 8.7 Equivalent circuit of the full-bridge converter with parasitic resistances to determine component losses.

Similarly, the current through the switches S_2 and S_4 can be approximated by

$$i_{S2} = i_{S4} = \begin{cases} 0, & \text{for } 0 < t \le T/2, \\ \dfrac{I_O}{n}, & \text{for } T/2 < t \le T/2 + DT, \\ 0, & \text{for } T/2 + DT < t \le T. \end{cases} \tag{8.64}$$

The rms value of switches S_2 and S_4 is

$$I_{S2rms} = I_{S4rms} = \sqrt{\frac{1}{T}\int_0^T i_{S2}^2\, dt} = \sqrt{\frac{1}{T}\int_{T/2}^{T/2+DT} \left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{D}}{n}. \tag{8.65}$$

The conduction loss in each MOSFET is

$$P_{rDS1} = r_{DS} I_{S1rms}^2 = \frac{D r_{DS} I_O^2}{n^2} = \frac{D r_{DS}}{n^2 R_L} P_O. \tag{8.66}$$

Assuming that the transistor output capacitance C_o is linear, the switching loss per transistor is

$$P_{sw} = f_s C_o V_I^2 = \frac{f_s C_o n^2 V_O^2}{4D^2} = \frac{f_s C_o V_O^2}{M_{V\,DC}^2} = \frac{f_s C_o n^2 R_L}{4D^2} P_O = \frac{f_s C_o R_L}{M_{V\,DC}^2} P_O. \tag{8.67}$$

The total power dissipation in each MOSFET (excluding the MOSFET drive power) is given by

$$\begin{aligned} P_{FET} = P_{rDS} + \frac{P_{sw}}{2} &= \frac{D r_{DS} I_O^2}{n^2} + \frac{f_s C V_I^2}{2} = \left(\frac{D r_{DS}}{n^2 R_L} + \frac{f_s C_o n^2 R_L}{8D^2}\right) P_O \\ &= \left(\frac{D r_{DS}}{n^2 R_L} + \frac{f_s C_o R_L}{2M_{V\,DC}^2}\right) P_O. \end{aligned} \tag{8.68}$$

The current through the primary winding resistance r_{T1} is

$$i_{rT1} = \begin{cases} \dfrac{I_O}{n}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T/2, \\ \dfrac{I_O}{n}, & \text{for } T/2 < t \le T/2 + DT, \\ 0, & \text{for } T/2 + DT < t \le T. \end{cases} \tag{8.69}$$

Hence, the rms value of the current through the primary winding resistance is

$$\begin{aligned} I_{rT1rms} &= \sqrt{\frac{1}{T}\int_0^T i_{rT1}^2\, dt} = \sqrt{\frac{1}{T}\left[\int_0^{DT} \left(\frac{I_O}{n}\right)^2 dt + \int_{T/2}^{T/2+DT} \left(\frac{I_O}{n}\right)^2 dt\right]} \\ &= \sqrt{\frac{2}{T}\int_0^{DT} \left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{2D}}{n}. \end{aligned} \tag{8.70}$$

Thus, the conduction loss in the primary winding resistance r_{T1} is

$$P_{rT1} = r_{T1} I_{rT1rms}^2 = \frac{2D r_{T1} I_O^2}{n^2} = \frac{2D r_{T1}}{n^2 R_L} P_O. \tag{8.71}$$

The current of the diode D_1 can be approximated by

$$i_{D1} = \begin{cases} I_O, & \text{for } 0 < t \le DT, \\ \dfrac{I_O}{2}, & \text{for } DT < t \le T/2, \\ 0, & \text{for } T/2 < t \le T/2 + DT, \\ \dfrac{I_O}{2}, & \text{for } T/2 + DT < t \le T, \end{cases} \tag{8.72}$$

leading to its rms value,

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^T i_{D1}^2\, dt} = \sqrt{\frac{1}{T}\left[\int_0^{DT} I_O^2\, dt + 2\int_{DT}^{T/2}\left(\frac{I_O}{2}\right)^2 dt\right]} = \frac{I_O\sqrt{2D+1}}{2}, \tag{8.73}$$

and the power loss in R_F in each diode,

$$P_{RF1} = R_F I_{D1rms}^2 = \frac{(2D+1)R_F I_O^2}{4} = \frac{(2D+1)R_F}{4R_L}P_O. \tag{8.74}$$

The average value of the diode current is

$$I_D = \frac{1}{T}\int_0^T i_{D1}\, dt = \frac{I_O}{2}, \tag{8.75}$$

which gives the power loss associated with the voltage V_F in each diode,

$$P_{VF1} = V_F I_D = \frac{V_F I_O}{2} = \frac{V_F}{2V_O}P_O. \tag{8.76}$$

Thus, the overall conduction loss in each diode is

$$P_{D1} = P_{RF1} + P_{VF1} = \frac{(2D+1)R_F I_O^2}{4} + \frac{V_F I_O}{2} = \left[\frac{(2D+1)R_F}{4R_L} + \frac{V_F}{2V_O}\right]P_O. \tag{8.77}$$

Ideally, the current through the diode D_2 is equal to the current through the diode D_1. Assuming that the diode D_2 is the same as the diode D_1, the power loss in the diode D_2 is the same as that in the diode D_1.

The current through the upper secondary winding is equal to that through the diode D_1. Consequently, the power loss in the upper secondary winding resistance r_{T2} is

$$P_{rT2} = r_{T2} I_{D1rms}^2 = \frac{(2D+1)r_{T2} I_O^2}{4} = \frac{(2D+1)r_{T2}}{4R_L}P_O. \tag{8.78}$$

The power loss in the lower secondary winding resistance is $P_{rT3} = P_{rT2}$.

The rms value of the inductor current is approximately equal to

$$I_{Lrms} \approx I_O, \tag{8.79}$$

which gives the inductor conduction loss,

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 = \frac{r_L}{R_L}P_O. \tag{8.80}$$

The current through the filter capacitor is

$$i_C \approx i_L - I_O = \begin{cases} \dfrac{\Delta i_L}{DT}t - \dfrac{\Delta i_L}{2}, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L}{\left(\frac{1}{2} - D\right)T}(t - DT) + \dfrac{\Delta i_L}{2}, & \text{for } DT < t \le T/2. \end{cases} \tag{8.81}$$

Hence, using (8.45), one obtains the rms value of the capacitor current,

$$I_{Crms} = \sqrt{\frac{1}{(T/2)}\int_0^{T/2} i_C^2\, dt} = \frac{\Delta i_L}{\sqrt{12}} = \frac{V_O(\frac{1}{2} - D)}{\sqrt{12} f_s L}, \tag{8.82}$$

and the power loss in the filter capacitor,

$$P_{rC} = r_C I_{Crms}^2 = \frac{r_C(\Delta i_L)^2}{12} = \frac{r_C V_O^2(\frac{1}{2} - D)^2}{12 f_s^2 L^2} = \frac{r_C R_L(\frac{1}{2} - D)^2}{12 f_s^2 L^2} P_O. \tag{8.83}$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= 4P_{rDS1} + 4P_{sw} + P_{rT1} + 2P_{rT2} + 2P_{D1} + P_{rL} + P_{rC} \\ &= \frac{DI_O^2(4r_{DS} + 2r_{T1})}{n^2} + 4f_s C_o V_I^2 + \frac{(2D+1)(R_F + r_{T2})I_O^2}{2} + V_F I_O + r_L I_O^2 + \frac{r_C(\Delta i_L)^2}{12} \\ &= \left[\frac{D(4r_{DS} + 2r_{T1})}{n^2 R_L} + \frac{4f_s C_o R_L}{M_{V\,DC}^2} + \frac{(2D+1)(R_F + r_{T2})}{2R_L}\right. \\ &\quad \left. + \frac{V_F}{V_O} + \frac{r_L}{R_L} + \frac{r_C R_L(\frac{1}{2} - D)^2}{12 f_s^2 L^2}\right] P_O. \end{aligned} \tag{8.84}$$

Thus, the converter efficiency is

$$\begin{aligned} \eta &= \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}} \\ &= \frac{1}{1 + \dfrac{D(4r_{DS} + 2r_{T1})}{n^2 R_L} + \dfrac{4f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{(2D+1)(R_F + r_{T2})}{2R_L} + \dfrac{V_F}{V_O} + \dfrac{r_L}{R_L} + \dfrac{r_C R_L(\frac{1}{2} - D)^2}{12 f_s^2 L^2}}. \end{aligned} \tag{8.85}$$

8.2.12 DC Voltage Transfer Function of Lossy Converter for CCM

Neglecting the magnetizing current i_{Lm}, the input current of the converter can be approximated by

$$i_I \approx i_{S1} + i_{S4} = \begin{cases} \dfrac{I_O}{n}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T/2, \\ \dfrac{I_O}{n}, & \text{for } T/2 < t \le T/2 + DT, \\ 0, & \text{for } T/2 + DT < t \le T. \end{cases} \tag{8.86}$$

Hence, the dc component of the input current is

$$I_I = \frac{1}{(T/2)}\int_0^{DT} i_{S1}\, dt = \frac{2}{T}\int_0^{DT}\left(\frac{I_O}{n}\right) dt = \frac{2DI_O}{n}, \tag{8.87}$$

leading to the dc current transfer function of the full-bridge converter,

$$M_{IDC} \equiv \frac{I_O}{I_I} = \frac{n}{2D}. \tag{8.88}$$

This equation is valid for both lossless and lossy converters. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{IDC} = \frac{n M_{V\,DC}}{2D}, \tag{8.89}$$

from which the voltage transfer function of the lossy full-bridge converter is

$$M_{V\,DC} = \frac{\eta}{M_{IDC}} = \frac{2D\eta}{n}$$

$$= \frac{2D}{n\left[1 + \frac{D(4r_{DS} + 2r_{T1})}{n^2 R_L} + \frac{4 f_s C_o n^2 R_L}{D^2} + \frac{(2D+1)(R_F + r_{T2})}{2R_L} + \frac{V_F}{V_O} + \frac{r_L}{R_L} + \frac{r_C R_L (\frac{1}{2} - D)^2}{12 f_s^2 L^2}\right]}. \tag{8.90}$$

From (8.90), the on-duty cycle is

$$D = \frac{n M_{V\,DC}}{2\eta} = \frac{n V_O}{2\eta V_I}. \tag{8.91}$$

The duty cycle D at a given dc voltage transfer function is greater for the lossy converter than for the lossless converter.

Substitution of (8.91) into (8.85) yields the efficiency of the full-bridge converter

$$\eta = \frac{N_\eta}{D_\eta}, \tag{8.92}$$

where

$$N_\eta = 1 - \frac{n M_{V\,DC}}{2R_L}\left(\frac{4r_{DS} + 2r_{T1}}{n^2} + R_F + r_{T2}\right) + \frac{r_C R_L n M_{V\,DC}}{24 f_s^2 L^2}$$

$$+ \left\{\left[\frac{n M_{V\,DC}}{2R_L}(R_F + r_{T2} + \frac{4r_{DS} + 2r_{T1}}{n^2}) - \frac{r_C R_L n M_{V\,DC}}{24 f_s^2 L^2} - 1\right]^2\right.$$

$$\left. - \frac{r_C R_L n^2 M_{V\,DC}^2}{12 f_s^2 L^2}\left[1 + \frac{r_L}{R_L} + \frac{R_F + r_{T2}}{2R_L} + \frac{V_F}{V_O} + \frac{4 f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{48 f_s^2 L^2}\right]\right\}^{\frac{1}{2}} \tag{8.93}$$

and

$$D_\eta = 2\left(1 + \frac{r_L}{R_L} + \frac{V_F}{V_O} + \frac{R_F + r_{T2}}{2R_L} + \frac{4 f_s C_o R_L}{M_{V\,DC}^2} + \frac{r_C R_L}{48 f_s^2 L^2}\right). \tag{8.94}$$

8.2.13 Design of Full-bridge Converter for CCM

Design a PWM full-bridge converter operating in CCM to meet the following specifications: $V_{Inom} = \sqrt{2} \times 220 = 311\,\text{V}$, $V_{Imin} = \sqrt{2} \times 200 = 283\,\text{V}$, $V_{Imax} = \sqrt{2} \times 240 = 340\,\text{V}$, $V_O = 48\,\text{V}$, $I_{Omin} = 2.5\,\text{A}$, $I_{Omax} = 25\,\text{A}$, and $V_r/V_O \leq 1\,\%$.

Solution. A full-bridge converter with a transformer center-tapped rectifier is selected for the design because the output voltage is low. The maximum and minimum values of the dc output power are

$$P_{Omax} = V_O I_{Omax} = 48 \times 25 = 1200\,\text{W} \tag{8.95}$$

and

$$P_{Omin} = V_O I_{Omin} = 48 \times 2.5 = 120\,\text{W}. \tag{8.96}$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{48}{25} = 1.92\,\Omega \tag{8.97}$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{48}{2.5} = 19.2\,\Omega. \tag{8.98}$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{48}{340} = 0.1412 = \frac{1}{7.083}, \tag{8.99}$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{48}{311} = 0.1543 = \frac{1}{6.479}, \tag{8.100}$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{48}{283} = 0.1696 = \frac{1}{5.896}. \tag{8.101}$$

Let us assume the converter efficiency is $\eta = 85\,\%$ and the maximum duty cycle $D_{max} \approx 0.4 < 0.5$. Hence, the transformer turns ratio is

$$n = \frac{2\eta D_{max}}{M_{V\,DCmax}} = \frac{2 \times 0.85 \times 0.4}{0.1696} = 4.01. \tag{8.102}$$

Let $n = 4$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{nM_{V\,DCmin}}{2\eta} = \frac{4 \times 0.1412}{2 \times 0.85} = 0.3322, \tag{8.103}$$

$$D_{nom} = \frac{nM_{V\,DCnom}}{2\eta} = \frac{4 \times 0.1543}{2 \times 0.85} = 0.3631, \tag{8.104}$$

and

$$D_{max} = \frac{nM_{V\,DCmax}}{2\eta} = \frac{4 \times 0.1696}{2 \times 0.85} = 0.3991. \tag{8.105}$$

Assume the switching frequency is $f_s = 50\,\text{kHz}$. The minimum inductance required to maintain the converter operation in CCM is

$$L_{min} = \frac{R_{Lmax}(\frac{1}{2} - D_{min})}{2f_s} = \frac{19.2 \times (\frac{1}{2} - 0.3322)}{2 \times 50 \times 10^3} = 32.2\,\mu\text{H}. \tag{8.106}$$

Pick $L = 40\,\mu\text{H}$.

The maximum ripple of the inductor current is

$$\Delta i_{Lmax} = \frac{V_O(\frac{1}{2} - D_{min})}{f_s L} = \frac{48 \times (\frac{1}{2} - 0.3322)}{50 \times 10^3 \times 40 \times 10^{-6}} = 4.027\,\text{A}. \tag{8.107}$$

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{48}{100} = 480\,\text{mV}. \tag{8.108}$$

If the filter capacitance is large enough, $V_r = r_{Cmax}\Delta i_{Lmax}$. Hence, the maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{480 \times 10^{-3}}{4.027} = 119.195\,\text{m}\Omega. \tag{8.109}$$

Pick a capacitor with $r_C = 100\,\text{m}\Omega$. The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is

$$C_{min} = \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{\frac{1}{2} - D_{min}}{2f_s r_C}\right\} = \max\left\{\frac{0.3991}{2f_s r_C}, \frac{\frac{1}{2} - 0.3322}{2f_s r_C}\right\} = \frac{D_{max}}{2f_s r_C}$$

$$= \frac{0.3991}{2 \times 50 \times 10^3 \times 0.1} = 39.91\,\mu\text{F}. \tag{8.110}$$

Pick $C = 50\,\mu\text{F}/100\,\text{V}/100\,\text{m}\Omega$.

The corner frequency is

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{40 \times 10^{-6} \times 100 \times 10^{-6}}} = 3.559\,\text{kHz}. \tag{8.111}$$

Since $i_1 = i_{D1}/n$, the maximum peak current through the ideal transformer primary winding is

$$I_{1max} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} = \frac{25}{4} + \frac{4.027}{2 \times 4} = 6.25 + 0.503 = 6.753\,\text{A}. \tag{8.112}$$

Let us assume that the maximum peak-to-peak value of the magnetizing current is less than 10 % of I_{1max}. Thus, the maximum peak of the magnetizing inductance current is

$$\Delta i_{Lm(max)} = 0.1 I_{1max} = 0.1 \times 6.753 = 0.6753\,\text{A}. \tag{8.113}$$

Hence, the minimum magnetizing inductance is

$$L_{m(min)} = \frac{D_{min} V_{Imax}}{f_s\,\Delta i_{Lm(max)}} = \frac{0.3322 \times 340}{50 \times 10^3 \times 0.6753} = 3.345\,\text{mH}. \tag{8.114}$$

Pick $L_m = 3.5\,\text{mH}$.

The voltage and current stresses of the power MOSFETs are

$$V_{SMmax} = V_{Imax} = 340\,\text{V} \tag{8.115}$$

and

$$I_{SMmax} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} + \frac{\Delta i_{Lm(max)}}{2} = \frac{25}{4} + \frac{4.027}{2 \times 4} + \frac{0.6753}{2}$$

$$= 6.25 + 0.503 + 0.338 = 7.091\,\text{A}. \tag{8.116}$$

The voltage stress of the diodes in the transformer center-tapped rectifier is

$$V_{DMmax} = \frac{2V_{Imax}}{n} = \frac{2 \times 340}{4} = 170\,\text{V}, \tag{8.117}$$

and the current stress of the diodes is

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = 25 + \frac{4.027}{2} = 27.014\,\text{A}. \tag{8.118}$$

MTM15N40 power MOSFETs are selected, which have $V_{DSS} = 400\,\text{V}$, $I_{SM} = 15\,\text{A}$ of continuous current, $r_{DS} = 300\,\text{m}\Omega$, $Q_g = 110\,\text{nC}$, and $C_o = 100\,\text{pF}$. MR866 fast recovery diodes are also selected, which have $I_{D(AV)}\text{max} = 40\,\text{A}$, $I_{FSM} = 350\,\text{A}$, $V_{DM} = 600\,\text{V}$, $V_F = 0.7\,\text{V}$, and $R_F = 12.5\,\text{m}\Omega$.

The power losses and the efficiency will be calculated at the maximum load current $I_{Omax} = 25\,\text{A}$ and the minimum dc input voltage $V_{Imin} = 283\,\text{V}$. The conduction power loss in each MOSFET is

$$P_{rDS1} = \frac{D_{max} r_{DS} I_{Omax}^2}{n^2} = \frac{0.3991 \times 0.3 \times 25^2}{4^2} = 4.68\,\text{W}. \tag{8.119}$$

The switching loss per transistor is

$$P_{sw} = f_s C_o V_{Imin}^2 = 50 \times 10^3 \times 100 \times 10^{-12} \times 283^2 = 0.4\,\text{W}. \tag{8.120}$$

Hence, the total power loss in each transistor is

$$P_{MOS} = P_{rDS1} + \frac{P_{sw}}{2} = 4.68 + \frac{0.4}{2} = 4.88\,\text{W}. \tag{8.121}$$

Assuming that the winding resistance of the primary winding is $r_{T1} = 25\,\text{m}\Omega$ and the winding resistances of the transformer on the secondary side are $r_{T2} = r_{T3} = 10\,\text{m}\Omega$, the conduction power losses in these resistances are

$$P_{rT1} = \frac{2D_{max} r_{T1} I_{Omax}^2}{n^2} = \frac{2 \times 0.3991 \times 0.025 \times 25^2}{4^2} = 0.78\,\text{W} \tag{8.122}$$

and

$$P_{rT2} = P_{rT3} = \frac{(2D_{max} + 1) r_{T2} I_{Omax}^2}{4} = \frac{(2 \times 0.3991 + 1) \times 0.01 \times 25^2}{4} = 2.81\,\text{W}. \tag{8.123}$$

The diode loss due to R_F is

$$P_{RF1} = \frac{(2D_{max} + 1) R_F I_{Omax}^2}{4} = \frac{(2 \times 0.3991 + 1) \times 0.0125 \times 25^2}{4} = 3.512\,\text{W}. \tag{8.124}$$

The diode loss due to V_F is

$$P_{VF1} = \frac{V_F I_{Omax}}{2} = \frac{0.7 \times 25}{2} = 8.75\,\text{W}, \tag{8.125}$$

and the conduction loss in each diode is

$$P_{D1} = P_{RF1} + P_{VF1} = 3.512 + 8.75 = 12.262\,\text{W}. \tag{8.126}$$

Assuming that the dc inductor ESR is $r_{L(dc)} = 10\,\text{m}\Omega$, the conduction power loss in the inductor is

$$P_{rL} = r_L I_{Omax}^2 = 0.01 \times 25^2 = 6.25\,\text{W}, \tag{8.127}$$

and the power loss in the capacitor ESR is

$$P_{rC} = \frac{r_C (\Delta i_{Lmax})^2}{12} = \frac{0.1 \times 4.027^2}{12} = 0.135\,\text{W}. \tag{8.128}$$

The total power loss is

$$\begin{aligned} P_{LS} &= 4P_{rDS} + 4P_{sw} + P_{rT1} + 2P_{rT2} + 2P_{D1} + P_{rL} + P_{rC} \\ &= 4 \times 4.68 + 4 \times 0.4 + 0.78 + 2 \times 2.81 + 2 \times 12.262 + 6.25 + 0.135 \\ &= 57.63\,\text{W} \end{aligned} \tag{8.129}$$

and the efficiency of the converter is

$$\eta = \frac{P_{Omax}}{P_{Omax} + P_{LS}} = \frac{1200}{1200 + 57.63} = 95.42\,\%. \tag{8.130}$$

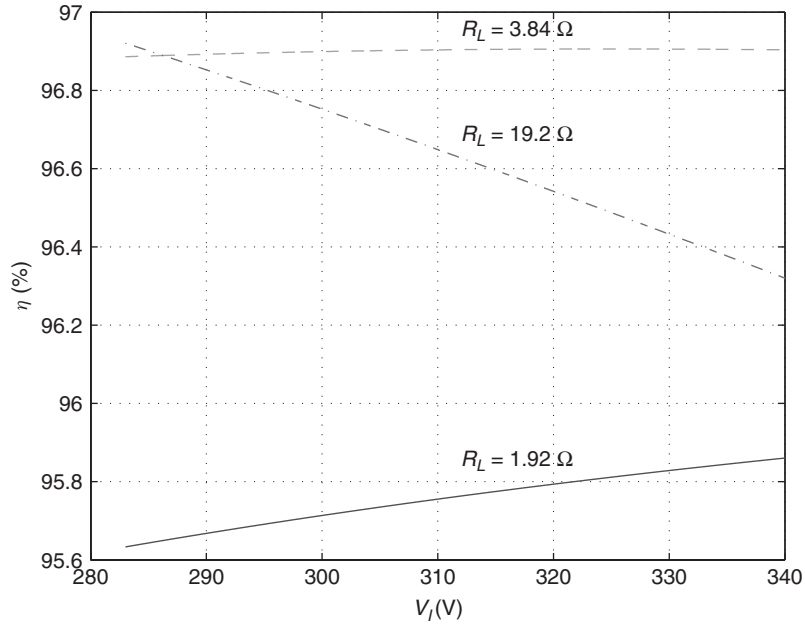


Figure 8.8 Efficiency η as a function of the dc input voltage V_I at fixed load resistances R_L for the full-bridge converter in CCM.

The peak-to-peak gate-to-source voltage is $V_{GSpp} = 14\,\text{V}$. Hence, one arrives at the gate-drive power per transistor

$$P_G = f_s V_{GSpp} Q_g = 50 \times 10^3 \times 14 \times 110 \times 10^{-9} = 77\,\text{mW}. \tag{8.131}$$

Figure 8.8–8.13 show the plots of the efficiency η and the duty cycle D as functions of V_I, I_O and R_L for the designed full-bridge converter for CCM. The efficiency η was computed from (8.92)–(8.94) and the duty cycle D was calculated from (8.91). The efficiency η first increases and then decreases as I_O increases. The duty cycle D decreases as V_I increases.

8.3 DC Analysis of PWM Full-bridge Converter for DCM

8.3.1 Time Interval $0 < t \leq DT$

During this time interval, the switches S_1 and S_3 and diode D_1 are ON and the switches S_2 and S_4 and the diode D_2 are OFF. The equivalent circuit is shown in Figure 8.14(a). The voltages across the switches S_2 and S_4 are

$$v_{S2} = v_{S4} = V_I, \tag{8.132}$$

the voltage across the primary winding is

$$v_1 = V_I, \tag{8.133}$$

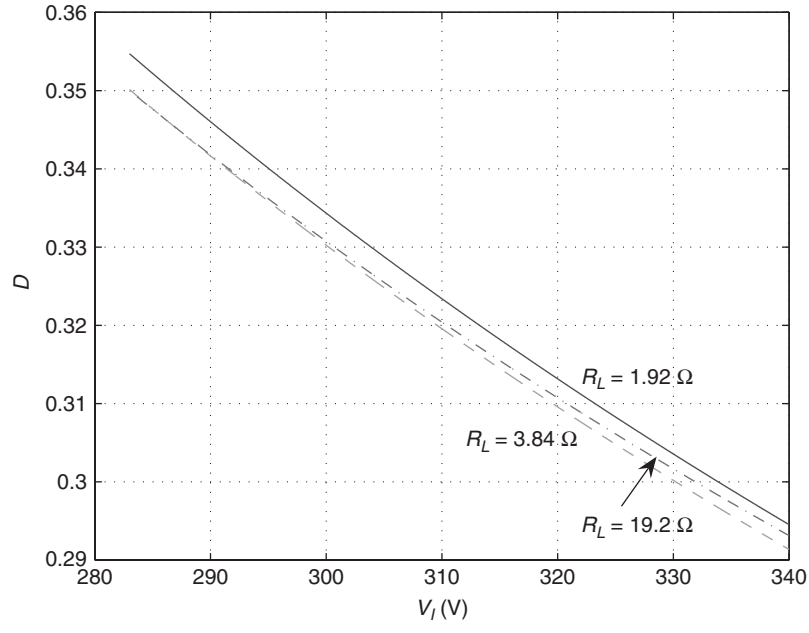


Figure 8.9 Duty cycle D as a function of the dc input voltage V_I at fixed load resistances R_L for the full-bridge converter in CCM.

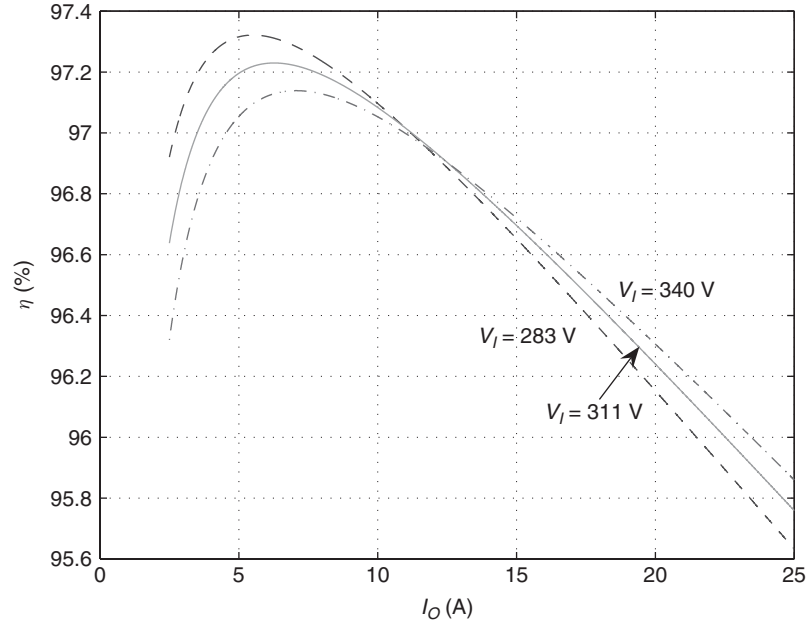


Figure 8.10 Efficiency η as a function of the dc load current I_O at fixed input voltages V_I for the full-bridge converter in CCM.

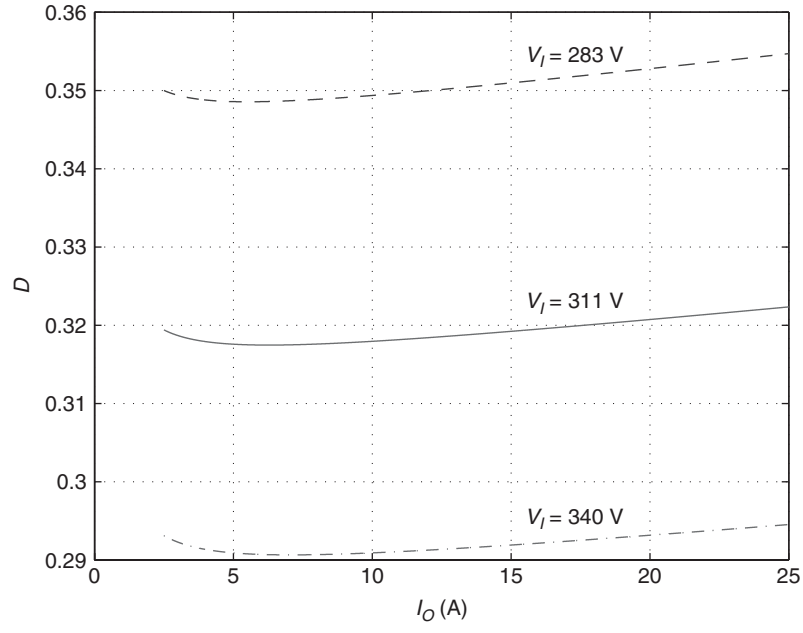


Figure 8.11 Duty cycle D as a function of the dc load current I_O at fixed input voltages V_I for the full-bridge converter in CCM.

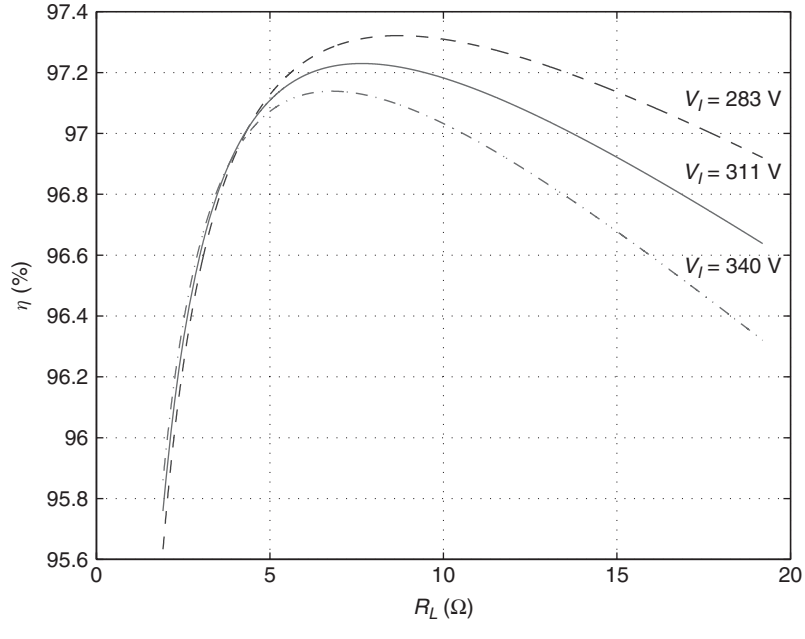


Figure 8.12 Efficiency η as a function of the load resistance I_O at fixed input voltages V_I for the full-bridge converter in CCM.

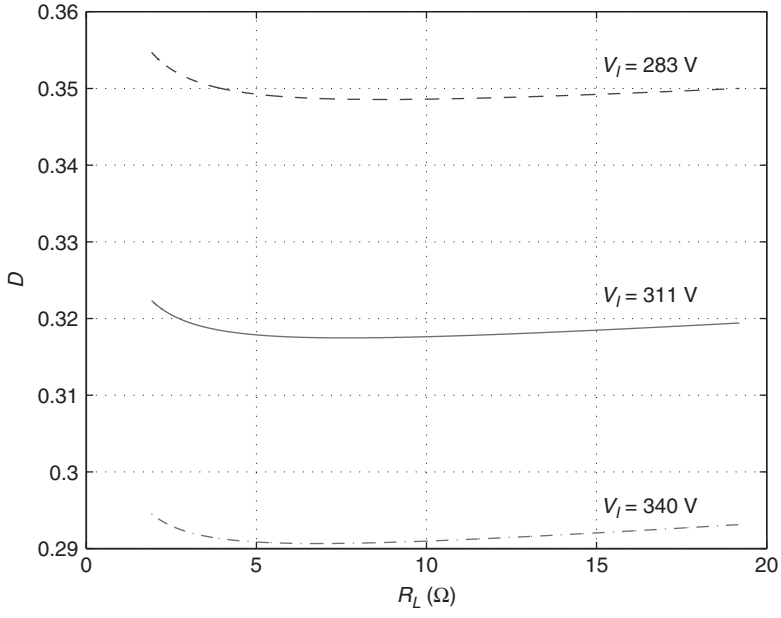


Figure 8.13 Duty cycle D as a function of the load resistance I_O at fixed input voltages V_I for the full-bridge converter in CCM.

the voltages across the transformer secondary are

$$v_2 = v_3 = \frac{v_1}{n} = \frac{V_I}{n}, \tag{8.134}$$

and the voltage across the diode D_2 is

$$v_{D2} = -(v_2 + v_3) = -\frac{2V_I}{n}. \tag{8.135}$$

The voltage across the inductor L is

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}, \qquad i_L(0) = 0, \tag{8.136}$$

and the inductor and switch current is

$$i_2 = i_{D1} = i_L = \frac{1}{L}\int_0^t v_L\,dt = \frac{1}{L}\int_0^t \left(\frac{V_I}{n} - V_O\right) dt = \frac{\dfrac{V_I}{n} - V_O}{L}t. \tag{8.137}$$

Hence, the peak inductor current is

$$\Delta i_L = i_L(DT) = I_{DM} = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} = \frac{\left(\dfrac{V_I}{n} - V_O\right)D}{f_s L}. \tag{8.138}$$

The voltage across the magnetizing inductance is

$$v_{Lm} = V_I = L_m\frac{di_{Lm}}{dt}, \qquad i_{Lm}(0) < 0, \tag{8.139}$$

which yields the current through the magnetizing inductance

$$i_{Lm} = \frac{1}{L_m}\int_0^t v_{Lm}\,dt = \frac{V_I}{L_m}t + i_{Lm}(0) \tag{8.140}$$

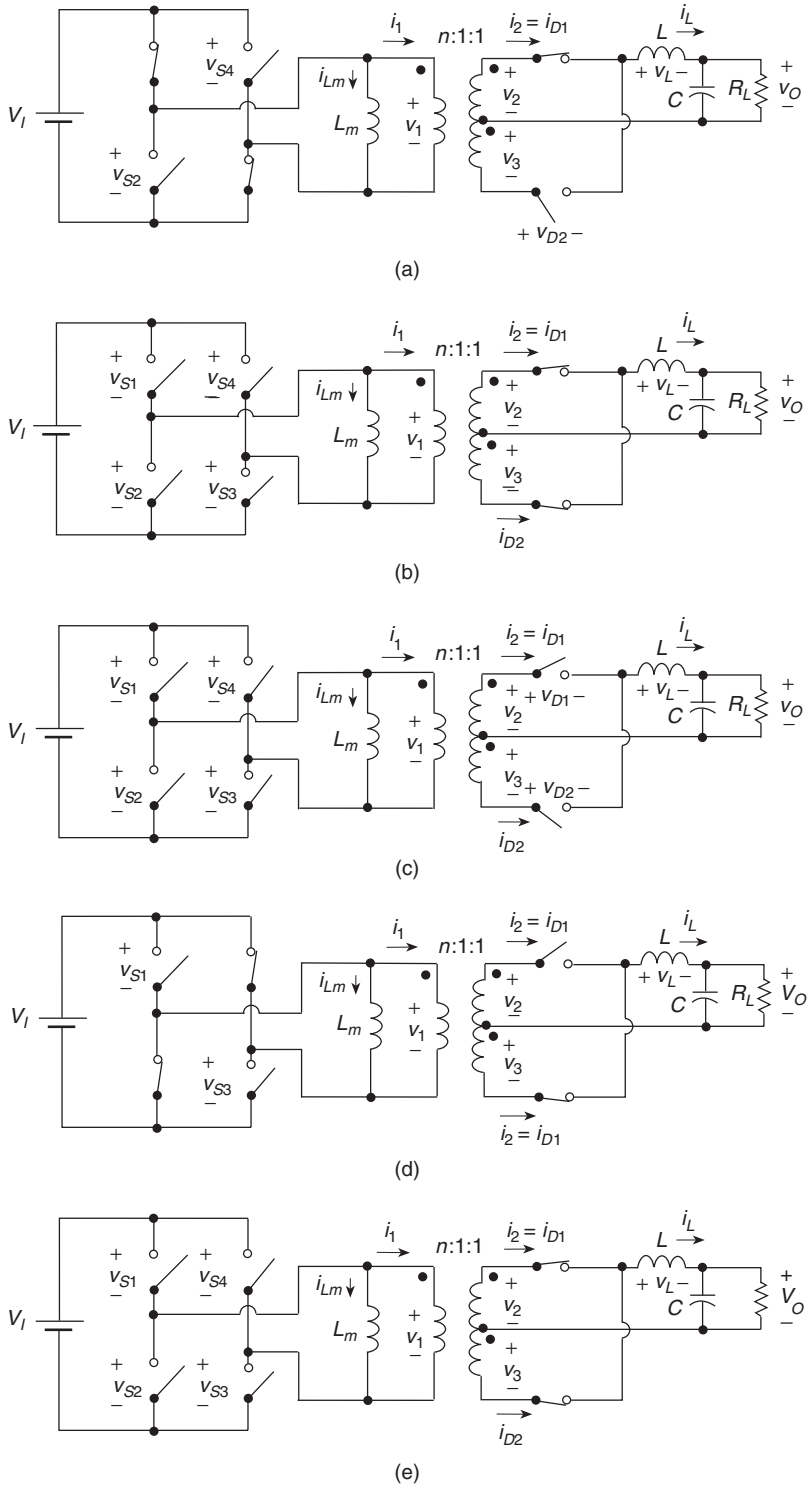


Figure 8.14 Equivalent circuit of the full-bridge converter with a transformer center-tapped rectifier for DCM. (a) For $0 < t \leq DT$. (b) For $DT < t \leq (D + D_1T)T$. (c) For $(D + D_1)T < t \leq T/2$. (d) For $T/2 < t \leq T/2 + DT$. (e) For $T/2 + DT < t \leq (D + D_1)T$.

and

$$i_{Lm}(DT) = \frac{V_I DT}{L_m} + i_{Lm}(0) = \frac{V_I D}{f_s L_m} + i_{Lm}(0). \tag{8.141}$$

Hence,

$$\Delta i_{Lm} = i_{Lm}(DT) - i_{Lm}(0) = \frac{V_I D}{f_s L_m}, \tag{8.142}$$

$$i_{Lm}(0) = -\frac{\Delta i_{Lm}}{2} = -\frac{V_I D}{2 f_s L_m}, \tag{8.143}$$

and

$$i_{Lm}(DT) = \frac{\Delta i_{Lm}}{2} = \frac{V_I D}{2 f_s L_m}. \tag{8.144}$$

The current through the primary winding of the ideal transformer is

$$i_1 = \frac{i_2}{n} = \frac{\dfrac{V_I}{n} - V_O}{nL} t, \tag{8.145}$$

and the current through switches S_1 and S_3 is

$$i_{S1} = i_{S3} = i_1 + i_{Lm} = \frac{\dfrac{V_I}{n} - V_O}{nL} t + \frac{V_I}{L_m} t + i_{Lm}(0) = \frac{\dfrac{V_I}{n} - V_O}{nL} t + \frac{V_I}{L_m} t - \frac{V_I D}{2 f_s L}. \tag{8.146}$$

8.3.2 Time Interval $DT < t \leq (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 8.14(b). During this time interval, all switches are OFF and both diodes are ON. The voltages across the switches are

$$v_{S1} = v_{S2} = v_{S3} = v_{S4} = \frac{V_I}{2}, \tag{8.147}$$

and the voltages across the primary and secondary windings are

$$v_1 = v_2 = v_3 = 0. \tag{8.148}$$

The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{8.149}$$

and the inductor and diode current is obtained using (8.138),

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L\, dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t} (-V_O)\, dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT)$$

$$= -\frac{V_O}{L}(t - DT) + \frac{\left(\dfrac{V_I}{n} - V_O\right) DT}{L}. \tag{8.150}$$

The peak inductor current is found to be

$$\Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\, dt = \frac{1}{L}\int_{(D+D_1)T}^{DT} (-V_O)\, dt = \frac{V_O D_1 T}{L}. \tag{8.151}$$

The currents of the diodes are

$$i_{D1} = i_{D2} = \frac{i_L}{2} = \frac{1}{L}\int_{DT}^{t} (-V_O)\, dt + i_L(DT) = -\frac{V_O}{2L}(t - DT) + \frac{i_L(DT)}{2}. \tag{8.152}$$

The voltage across the magnetizing inductance is

$$v_{Lm} = 0, \tag{8.153}$$

the current through the magnetizing inductance is

$$i_{Lm} = i_{Lm}(DT) = \frac{V_I D}{2 f_s L_m}, \tag{8.154}$$

and the current through the primary winding of the ideal transformer is

$$i_1 = -i_{Lm} = -\frac{V_I D}{2 f_s L_m}. \tag{8.155}$$

This time interval ends when the diode currents reach zero.

8.3.3 Time Interval $(D + D_1)T < t \leq T/2$

During this time interval, all switches and both diodes are OFF. The equivalent circuit is shown in Figure 8.14(c). The voltages across the switches are

$$v_{S1} = v_{S2} = v_{S3} = v_{S4} = \frac{V_I}{2}, \tag{8.156}$$

the voltages across the primary and secondary windings are

$$v_1 = v_2 = v_3 = 0, \tag{8.157}$$

and the voltages across the diodes are

$$v_{D1} = v_{D2} = -V_O. \tag{8.158}$$

The inductor current i_L, the inductor voltage v_L, the switch currents, and the diode currents are zero.

The voltage across the magnetizing inductance is

$$v_{Lm} = 0, \tag{8.159}$$

the current through the magnetizing inductance is

$$i_{Lm} = i_{Lm}(DT) = \frac{V_I D}{2 f_s L_m}, \tag{8.160}$$

and the current through the primary winding of the ideal transformer is

$$i_1 = -i_{Lm} = -\frac{V_I D}{2 f_s L_m}. \tag{8.161}$$

This time interval ends when the switches S_2 and S_4 are turned on by the driver.

8.3.4 DC Voltage Transfer Function for DCM

Referring to Figure 8.15 and using the volt-second balance,

$$\left(\frac{V_I}{n} - V_O\right) DT = V_O D_1 T, \tag{8.162}$$

which leads to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{n(D + D_1)}. \tag{8.163}$$

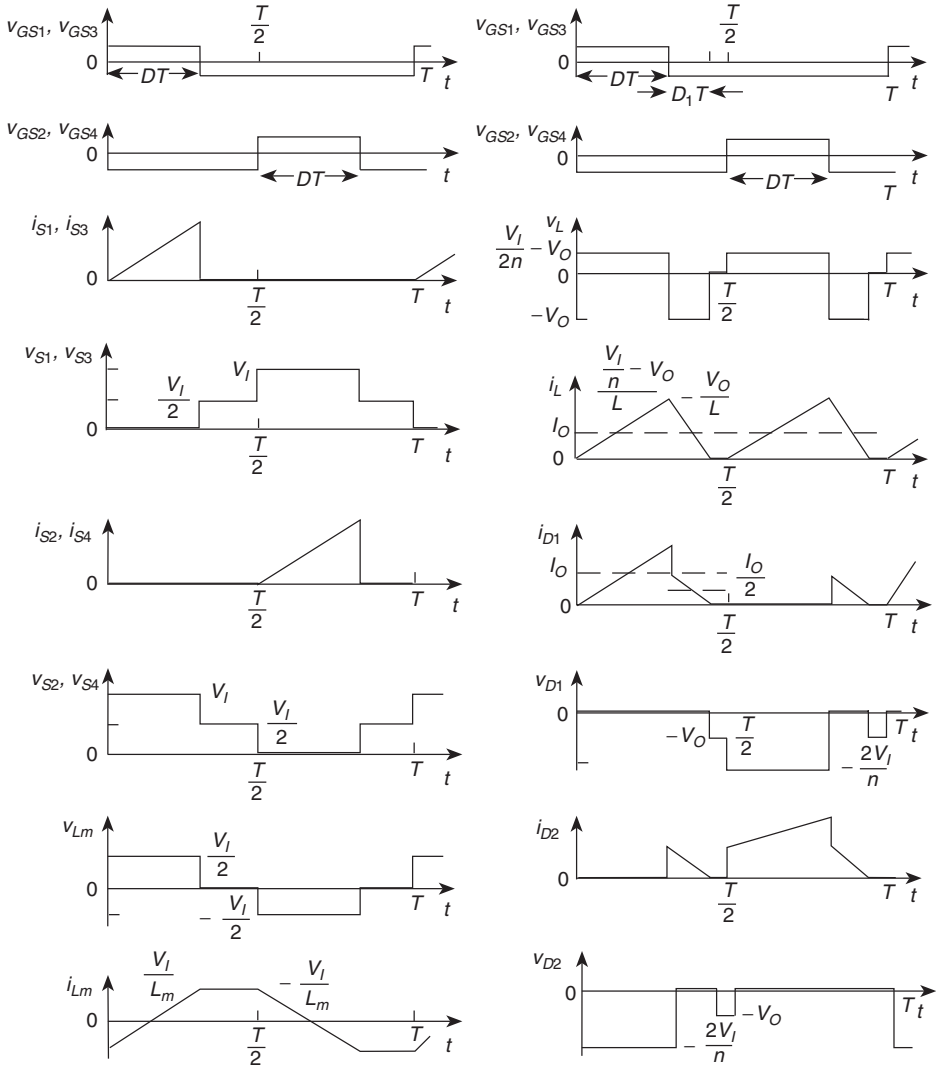


Figure 8.15 Waveforms in the full-bridge converter with a transformer center-tapped rectifier for DCM.

From (8.138) and (8.163), the peak-to-peak inductor current is

$$\Delta i_L = \frac{\left(\frac{V_I}{n} - V_O\right) DT}{L} = \frac{V_O D(1 - nM_{V\,DC})}{nM_{V\,DC} f_s L}. \tag{8.164}$$

The dc output current is equal to the average value of the inductor current. Using (8.163) and (8.164),

$$I_O = \frac{1}{T/2}\int_0^{T/2} i_L\, dt = \frac{2}{T}\,\frac{(D + D_1)T\Delta i_L}{2} = (D + D_1)\Delta i_L$$

$$= \frac{DV_O(D + D_1)(1 - nM_{V\,DC})}{nM_{V\,DC} f_s L} = \frac{V_O D^2(1 - nM_{V\,DC})}{n^2 M_{V\,DC}^2 f_s L}. \tag{8.165}$$

Hence,

$$D = \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L I_O}{(1 - nM_{V\,DC})V_O}}$$

$$= \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L}{(1 - nM_{V\,DC})R_L}} \quad \text{for } D \le \frac{1}{2} - \frac{2f_s L}{R_L} = \frac{1}{2} - \frac{2f_s L I_O}{V_O}. \tag{8.166}$$

At the CCM/DCM boundary,

$$M_{V\,DCB} = \frac{2D_B}{n} \tag{8.167}$$

as in CCM. Substitution of this into (8.166) yields the duty cycle D_B at the CCM/DCM boundary,

$$D_B = \frac{1}{2} - \frac{2f_s L}{R_L}. \tag{8.168}$$

Figures 8.16 and 8.17 respectively show plots of D versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of $nM_{V\,DC}$ for both CCM and DCM for the lossless full-bridge converter.

From (8.166),

$$\frac{f_s L}{D^2 R_L} n^2 M_{V\,DC}^2 + nM_{V\,DC} - 1 = 0. \tag{8.169}$$

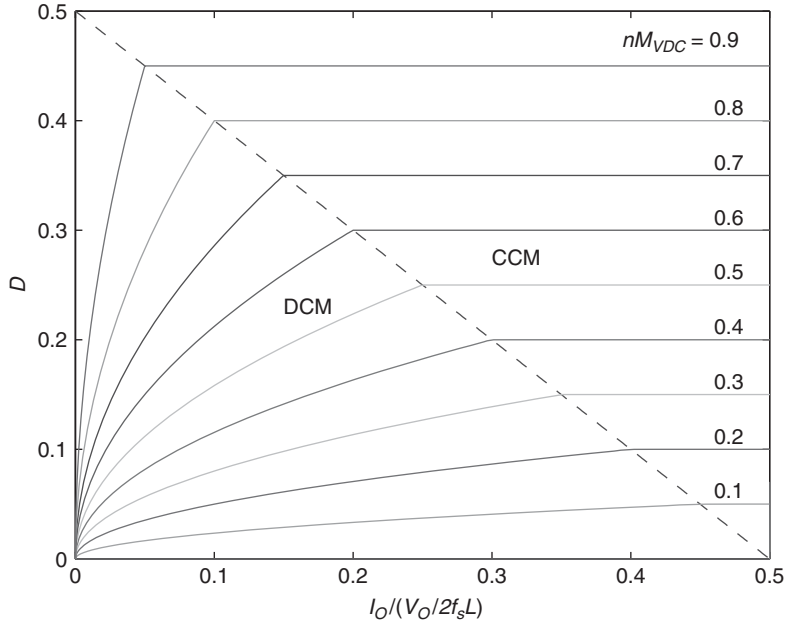


Figure 8.16 Duty cycle D as a function of the normalized load current $I_O/(V_O/2f_sL)$ at fixed values of $nM_{V\,DC}$ for the lossless full-bridge converter.

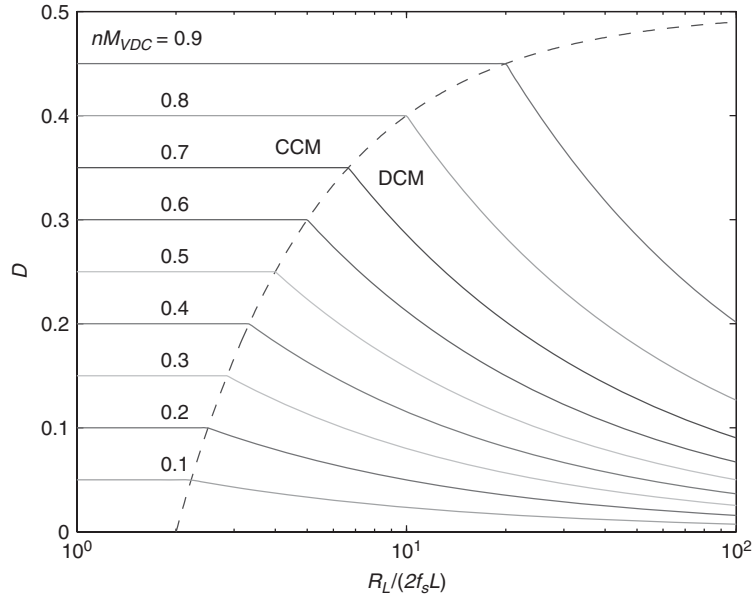


Figure 8.17 Duty cycle D as a function of normalized load resistance $R_L/(2f_sL)$ at fixed values of $nM_{V\,DC}$ for the lossless full-bridge converter.

Solving this equation for $M_{V\,DC}$ gives

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{2}{n\left(1+\sqrt{1+\dfrac{4f_sL}{D^2R_L}}\right)}$$

$$= \frac{2}{n\left(1+\sqrt{1+\dfrac{4f_sLI_O}{D^2V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \quad (8.170)$$

Figures 8.18 and 8.19 respectively show $nM_{V\,DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of D for both CCM and DCM for the lossless full-bridge converter. Notice that $M_{V\,DC}$ depends strongly on D, R_L, L, and f_s for DCM.

Using (8.163) and (8.170),

$$D_1 = D\left(\frac{1}{nM_{V\,DC}} - 1\right) = \frac{D}{2}\left(\sqrt{1+\frac{4f_sL}{D^2R_L}} - 1\right)$$

$$= \frac{D}{2}\left(\sqrt{1+\frac{4f_sLI_O}{D^2V_O}} - 1\right), \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \quad (8.171)$$

The dc input current is

$$i_I = i_{SI} = i_1 + i_{Lm} \approx i_1 = \frac{\dfrac{V_I}{n} - V_O}{nL}t, \quad \text{for } 0 < t \le DT, \quad (8.172)$$

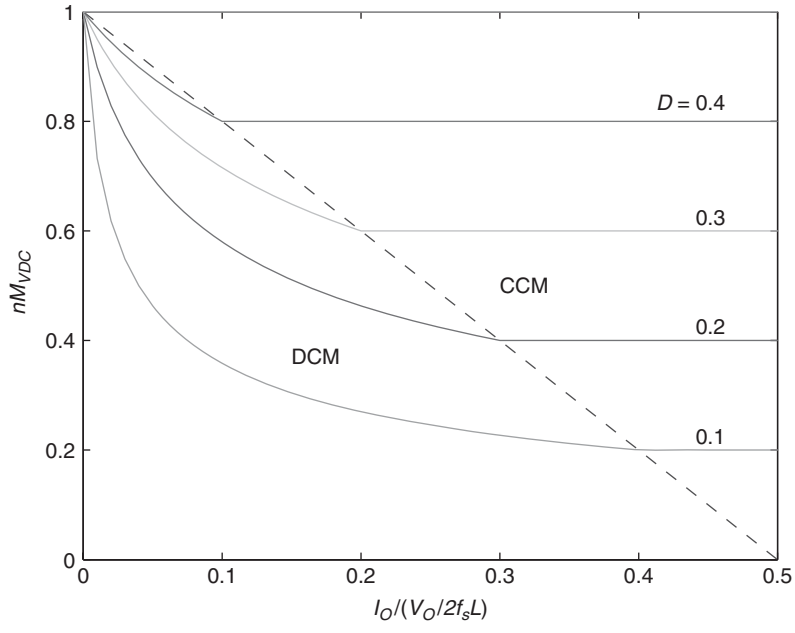


Figure 8.18 DC voltage transfer function $nM_{V\,DC}$ as a function of the normalized load current $I_O/(V_O/2f_sL)$ at fixed values of D for the lossless full-bridge converter.

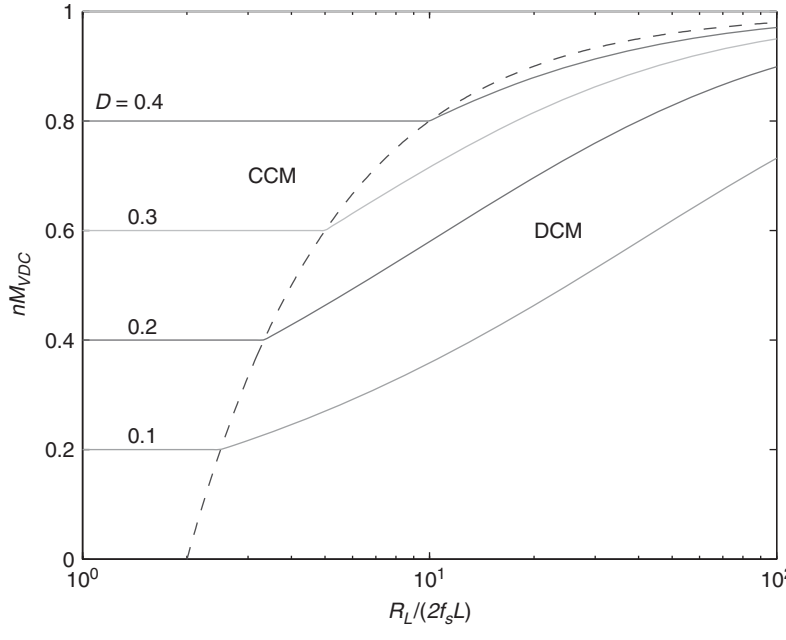


Figure 8.19 DC voltage transfer function $nM_{V\,DC}$ as a function of normalized load resistance $R_L/(2f_sL)$ at fixed values of D for the lossless full-bridge converter.

resulting in the dc input current

$$I_I = \frac{1}{T/2}\int_0^{DT} i_I\,dt = \frac{2}{T}\int_0^{DT} \frac{\frac{V_I}{n} - V_O}{nL} t\,dt = \frac{D^2\left(\frac{V_I}{n} - V_O\right)}{nf_sL} \tag{8.173}$$

and the dc input power

$$P_I = V_I I_I = \frac{D^2\left(\frac{V_I^2}{n} - V_O V_I\right)}{nf_sL}. \tag{8.174}$$

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{8.175}$$

The efficiency of the converter is

$$\eta = \frac{P_O}{P_I} = \frac{f_sLn^2M_{V\,DC}^2}{D^2R_L(1 - nM_{V\,DC})}, \tag{8.176}$$

which gives the duty cycle of the lossy full-bridge converter in DCM,

$$\begin{aligned} D &= \sqrt{\frac{n^2M_{V\,DC}^2 f_sL}{\eta R_L(1 - nM_{V\,DC})}} \\ &= \sqrt{\frac{n^2M_{V\,DC}^2 f_sLI_O}{\eta V_O(1 - nM_{V\,DC})}}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \end{aligned} \tag{8.177}$$

Rearrangement of this yields

$$\begin{aligned} M_{V\,DC} = \frac{V_O}{V_I} &= \frac{2}{n\left(1 + \sqrt{1 + \frac{4f_sL}{\eta D^2R_L}}\right)} \\ &= \frac{2}{n\left(1 + \sqrt{1 + \frac{4f_sLI_O}{\eta D^2V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_sL}{R_L} = \frac{1}{2} - \frac{2f_sLI_O}{V_O}. \end{aligned} \tag{8.178}$$

8.3.5 Maximum Inductance for DCM

The inductor current waveforms at the CCM/DCM boundary for V_{Imin} and V_{Imax} are shown in Figure 8.20. The maximum output current at the boundary is

$$I_{Omax} = I_{OB} = \frac{\Delta i_{Lmin}}{2} = \frac{V_O(0.5 - D_{Bmax})}{2f_sL_{max}} = \frac{V_O}{R_{Lmin}}, \tag{8.179}$$

which gives the maximum inductance required to maintain the converter operation in DCM as

$$L_{max} = \frac{R_{Lmin}(0.5 - D_{Bmax})}{2f_s} = \frac{V_O(0.5 - D_{Bmax})}{2f_sI_{Omax}}. \tag{8.180}$$

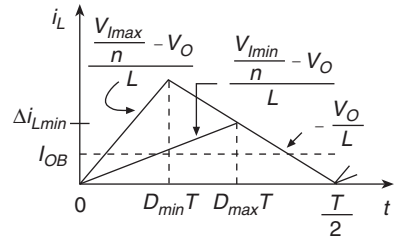


Figure 8.20 Waveform of the inductor current in the full-bridge converter at the boundary between CCM and DCM for V_{Imin} and V_{Imax}.

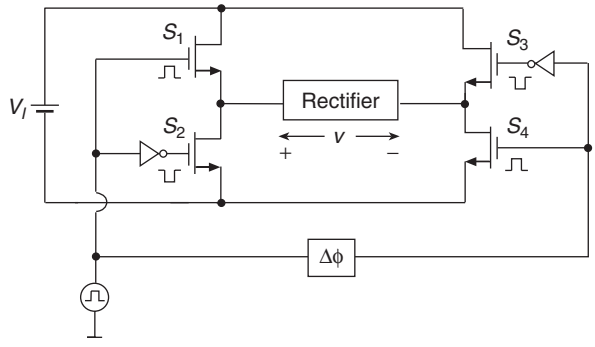


Figure 8.21 Full-bridge converter with phase-shift control.

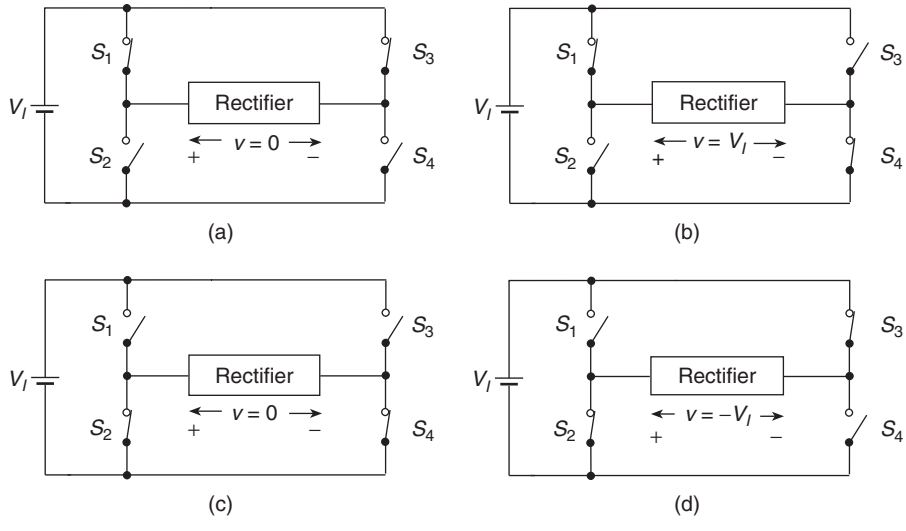


Figure 8.22 Equivalent circuits in full-bridge converter with phase-shift control.

8.4 Phase-controlled Full-bridge Converter

A full-bridge converter with phase-shift control is shown in Figure 8.21. The gate-to-source voltages in the right switching leg are shifted by the phase $\Delta\phi$ with respect to the gate-to-source voltages in the left switching leg. Figure 8.22 depicts the equivalent circuits for the phase-controlled full-bridge converter. Waveforms for this circuit are shown in Figure 8.23. It can be seen that the duty cycle D of the voltage across the rectifier can be controlled by varying the phase shift $\Delta\phi$. The duty cycle D is given by

$$D = \frac{1}{2} - \frac{\Delta\phi}{2\pi}. \tag{8.181}$$

As the phase shift $\Delta\phi$ increases from 0 to π, the duty cycle of the upper pulse and the lower pulse decreases from 0.5 to 0.

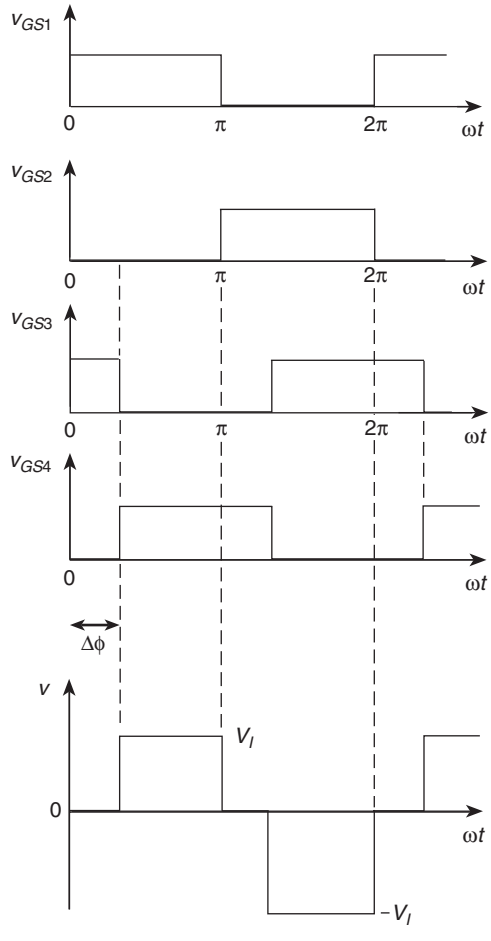


Figure 8.23 Waveforms in full-bridge converter with phase-shift control.

8.5 Summary

- The PWM full-bridge converter is either a step-up or a step-down converter.
- The dc voltage transfer function of the lossless converter is $M_{V\,DC} = 2D/n$.
- The duty cycle must be less than 50 %.
- The transformer is not required to store energy in the full-bridge converter.
- The magnetic core utilization is excellent because the flux can vary between $\pm B_s$, where B_s is the saturation flux density.
- The converter has conduction losses and switching losses.
- The duty cycle D of the lossy converter is greater than that of the lossless converter at the same value of the dc voltage transfer function.
- The peak-to-peak value of the inductor ripple current Δi_L is independent of the dc load current for CCM.
- The peak-to-peak value of the current through the filter capacitor C is relatively low and is equal to the peak-to-peak inductor ripple current Δi_L.
- If the capacitance of the filter capacitor is sufficiently high, the output ripple voltage is determined only by the ESR of the filter capacitor and is independent of the capacitance of the filter capacitor.
- The minimum value of the inductor is determined by the CCM/DCM boundary between CCM and DCM, output ripple voltage, core saturation, or ac losses in the inductor and/or the filter capacitor.
- The input current is pulsating. However, an LC filter can be added at the input of the converter to obtain a nonpulsating input current waveform.
- The corner frequency of the output filter $f_o = 1/(2\pi\sqrt{LC})$ is independent of the load resistance.
- The output inductor can be made smaller because the ripple frequency is twice that of the single-ended converters.
- It is relatively difficult to drive the upper transistors because the gates are not referenced to ground.

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8.7 Review Questions

8.1 Give the expression for the dc voltage transfer function of the lossless full-bridge converter.

8.2 What is the maximum value of the duty cycle for the full-bridge converter?

8.3 What happens when the duty cycle is too large?

8.4 How can cross-conduction be prevented in the full-bridge converter?

8.5 Is the transformer required to store energy in the full-bridge converter?

8.6 What is the dc component of the current through the primary winding of the transformer in the full-bridge converter?

8.7 Is the magnetic core utilization good in the full-bridge converter?

8.8 Is the input current of the basic full-bridge converter pulsating?

8.9 How can the circuit be modified to obtain a nonpulsating input current in the full-bridge converter?

8.10 Are the upper transistors driven with respect to ground in the full-bridge converter?

8.11 What is the correct magnetizing inductance L_m of the transformer?

8.12 Do the losses increase or decrease the duty cycle D of the full-bridge converter at a given value of $M_{V\,DC}$ for CCM?

8.13 Is the corner frequency of the output filter dependent on the load resistance?

8.14 Compare the frequency of the output ripple voltage with the frequency of the gate-to-source voltages of the power transistors.

8.8 Problems

8.1 Derive an expression for the voltage stress of the diodes in the full-bridge converter with a full-bridge rectifier.

8.2 A full-bridge PWM converter has input voltage from a US single-phase rectified line, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, and $f_s = 35\,\text{kHz}$. Find the transformer turns ratio n, the minimum duty cycle D_{min}, and the maximum duty cycle D_{max}.

8.3 A full-bridge PWM converter has $V_{Imin} = 127\,\text{V}$, $V_{Imax} = 187\,\text{V}$, $n = 2$, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, and $f_s = 35\,\text{kHz}$. Find the voltage stresses of the transistors and the diodes.

8.4 A full-bridge PWM converter has $V_{Imin} = 127\,\text{V}$, $V_{Imax} = 187\,\text{V}$, $n = 2$, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, $D_{min} = 0.27$, and $f_s = 35\,\text{kHz}$. Find the minimum inductance required to maintain the converter operation in CCM. Calculate the maximum value of peak-to-peak inductor ripple current and $\Delta i_{Lmax}/I_{Omax}$.

8.5 A full-bridge PWM converter has $V_{Imin} = 127\,\text{V}$, $V_{Imax} = 187\,\text{V}$, $n = 2$, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, $D_{min} = 0.27$, and $f_s = 35\,\text{kHz}$. Find the minimum inductance at which the ratio of the peak-to-peak inductor ripple current to the maximum load current is less than 10 %.

8.6 A full-bridge PWM converter has input voltage from a US single-phase rectified line, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, $L = 70\,\mu\text{H}$, $f_s = 35\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$. Find the filter capacitance and the corner frequency of the output filter.

8.7 A full-bridge PWM converter has input voltage from a US single-phase rectified line, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, and $f_s = 35\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$. Find the minimum magnetizing inductance $L_{m(min)}$ at which its maximum peak-to-peak current is less than 10 % of the maximum peak current of the ideal transformer primary winding.

8.8 A full-bridge PWM converter has $V_{Imin} = 127\,\text{V}$, $V_{Imax} = 187\,\text{V}$, $n = 2$, $V_O = 48\,\text{V}$, $P_O = 1$ to $2.5\,\text{kW}$, $D_{min} = 0.2815$, and $f_s = 35\,\text{kHz}$. Find the current stresses of the transistors and the diodes.

8.9 A full-bridge dc–dc converter accepts the US single-phase rectified line and delivers $V_O = 1\,\text{kV}$. Find the transformer turns ratio n, the minimum duty cycle D_{min}, and the maximum duty cycle D_{max}.

8.10 A full-bridge dc–dc converter with a bridge rectifier accepts the US single-phase rectified line and has $V_O = 1\,\text{kV}$ and $n = 1/10$. Find the voltage stresses of the switches and the diodes.

8.11 A full-bridge dc–dc converter accepts the US single-phase rectified line and has $V_O = 1\,\text{kV}$, $n = 1/10$, $P_O = 100\,\text{W}$ to $1\,\text{kW}$, $D_{min} = 0.2815$, and $f_s = 50\,\text{kHz}$. Find the minimum inductance for CCM operation.

8.12 A full-bridge dc–dc converter accepts the US single-phase rectified line and has $V_O = 1\,\text{kV}$, $n = 1/10$, $P_O = 100\,\text{W}$ to $1\,\text{kW}$, $D_{min} = 0.2814$, $D_{max} = 0.4144$, $L = 25\,\text{mH}$, $V_r/V_O \leq 1\,\%$, and $f_s = 50\,\text{kHz}$. Find the minimum filter capacitance and its minimum ESR.

8.13 A full-bridge dc–dc converter should accept the US three-phase rectified line and deliver $V_O = 1\,\text{kV}$. Find the transformer turns ratio n.

8.14 Design a full-bridge PWM converter suitable for telecommunications applications with $V_I = \sqrt{2}(220\,V \pm 10\,\%)$, $V_O = 48\,\text{V}$, $I_O = 5$ to $50\,\text{A}$, $f_s = 35\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$. Assume $r_{DS} = 0.3\,\Omega$, $C_o = 100\,\text{pF}$, $Q_g = 110\,\text{nF}$, $V_F = 0.7\,\text{V}$, $R_F = 12.5\,\text{m}\Omega$, $r_{T1} = 25\,\text{m}\Omega$, $r_{T2} = 10\,\text{m}\Omega$, and $r_{L(dc)} = 10\,\text{m}\Omega$. Assume initially that the converter efficiency is $\eta = 96\,\%$.

8.15 Design a full-bridge PWM converter for aerospace applications with $V_I = 270\,\text{V} \pm 10\,\%$, $V_O = 28\,\text{V}$, $I_O = 10$ to $100\,\text{A}$, and $V_r/V_O \leq 1\,\%$.

8.16 Design a full-bridge converter to meet the following specifications: $V_I = 48 \pm 6\,\text{V}$, $V_O = 5\,\text{V}$, $I_O = 5$ to $50\,\text{A}$, and $V_r/V_O \leq 1\,\%$. Assume $r_{DS} = 0.18\,\Omega$, $C_o = 100\,\text{pF}$, $Q_g = 110\,\text{nF}$, $V_F = 0.3\,\text{V}$, $R_F = 10\,\text{m}\Omega$, $r_{T1} = 10\,\text{m}\Omega$, $r_{T2} = 3\,\text{m}\Omega$, $r_{L(dc)} = 4\,\text{m}\Omega$, and $f_s = 50\,\text{kHz}$. Assume initially the converter efficiency $\eta = 75\,\%$.

8.17 Design a universal off-line full-bridge converter operating in CCM to meet the following specifications: the input voltage is from a single-phase utility line anywhere in world with the rms voltage $V = 90$ to $240\,\text{Vrms}$, $f = 50/60\,\text{Hz}$, $V_O = 48\,\text{V}$, $I_O = 5$ to $50\,\text{A}$, $f_s = 100\,\text{kHz}$, and $V_r/V_O \leq 1\,\%$.

9

Push-pull PWM DC–DC Converter

9.1 Introduction

The PWM push-pull converter [1]–[18] contains two transistors that are driven with respect to ground. This is the main advantage of the converter. The voltage stress across the switches is high, equal to $2V_I$, which is twice the switch voltage stress in the half-bridge and full-bridge converters. The push-pull converter uses a relatively small double-center-tapped transformer that is excited in both directions. However, the circuit suffers from flux imbalance of the transformer core because the dc current flows through the primary and therefore the core may saturate. The converter is used in medium-power applications, from 150 to 500 W. It belongs to the family of buck-derived converters. In this chapter, analysis and design principles for the converter are given.

9.2 DC Analysis of PWM Push-pull Converter for CCM

9.2.1 Circuit Description

Figure 9.1 shows two circuits of the PWM push-pull dc–dc converter with a transformer center-tapped rectifier. The converter consists of two power MOSFETs used as controllable switches S_1 and S_2, a transformer, two diodes D_1 and D_2, and a filter capacitor C. The converter employs a center-tapped transformer on both the primary and the secondary sides. The turns ratio of the upper primary winding to the upper secondary winding, and of the lower primary winding to the lower secondary winding, is $n : 1$. The number of turns in both primaries is the same, and the number of turns in both secondaries is also the same. Both windings of the primary are wound in the same direction, and both windings of the secondary are also wound in the same direction. Therefore, the magnetic flux generated

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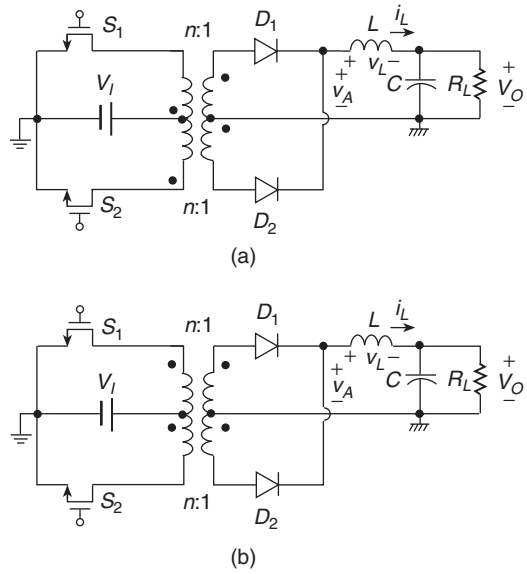


Figure 9.1 Push-pull PWM converter. (a) With one possible polarity of the transformer. (b) With another polarity of the transformer.

within the core takes on both positive and negative values, resulting in a better core utilization and in a reduced required core size. The only difference between the circuits shown in Figure 9.1 is in the polarity of the primary windings with respect to the secondary windings. In the converter of Figure 9.1(a), when the switch S_1 is ON, the diode D_1 is ON and the diode D_2 is OFF. When the switch S_2 is ON, the diode D_2 is ON and the diode D_1 is OFF. In the converter of Figure 9.1(b), when the switch S_1 is ON, the diode D_2 is ON and the diode D_1 is OFF. When the switch S_2 is ON, the diode D_1 is ON and the diode D_2 is OFF. The transistors are driven by nonoverlapping voltages that are out of phase by 180°. The maximum duty cycle of the gate-to-drive voltages is slightly less than 50 %.

One of the main advantages of the push-pull converter is that the gates of both transistors are referenced to ground. Therefore, it is easy to drive both transistors. The isolation transformer does not have to store energy. Its magnetizing inductances should be large enough to reduce the current through and the energy stored in these inductances. Normally, the magnetizing current should be less than 10 % of the primary current. The voltage stresses of the switches are $2V_I$ and the voltage stresses of the diodes in the center-tapped rectifier are $2V_I/n$. The push-pull converter may also have a bridge rectifier. Typical output power levels are in the range 150–500 W. Multiple-output power supplies can be built using push-pull converter topology. A bridge rectifier can be also used.

The main disadvantage of the push-pull converter is the so-called flux imbalance. Notice that there are no coupling capacitors in series with both halves of the primary. Therefore, a direct dc path exists through the transformer primary. In reality, the two power transistors, the two drive gate voltages, and the two halves of the primary winding are not perfectly identical. For example, one transistor may have a slightly higher on-voltage than the other, the on-duty cycle of one transistor may be slightly less than the other, or one half of the primary may have a fraction of a turn less than the other. Therefore, the transformer core will never operate symmetrically about the origin of the $B-H$ curve. When switch S_1 is ON, the volt-second product is equal to the product of the voltage across the upper primary and the on-time of S_1. When switch S_2 is ON, the volt-second product is equal to the product

of the voltage across the lower primary and the on-time of S_2. Even if these volt-second products differ by only a small fraction of a percent, the core does not return to its starting point at the beginning of the next cycle. If this process continues for many cycles, the operating point of the core will drift off the center of the hysteresis loop to saturation. This will cause a high current to flow through the transistor connected in series with the half of the transformer which entered saturation. The high current normally leads to transistor destruction. One way to avoid this situation is to add high-speed pulse-by-pulse current sensors to both transistors and connect them to the control circuit, which should reduce the duty cycle when either switch current exceeds a safe value. Current-mode control, which inherently has overcurrent protection, should be used in push-pull converters. Because of the core imbalance problem, the push-pull converter is less attractive than half-bridge and full-bridge converters. This is especially true in applications with dynamic loads.

9.2.2 Assumptions

The analysis of the push-pull PWM converter is based on the following assumptions:

1. The power MOSFETs and the diodes are ideal switches.
2. The transistor and diode capacitances and the lead inductances are zero.
3. The transformer is modeled as an ideal transformer and its magnetizing inductance L_m. Leakage inductances and stray capacitances are neglected.
4. Passive components are linear, time-invariant, and frequency-independent.
5. The output impedance of the input voltage source V_I is zero for both dc and ac components.
6. The circuit is symmetrical.
7. The converter is operated in steady state.

9.2.3 Time Interval $0 < t \leq DT$

The push-pull converter of Figure 9.1(a) will be considered. During the time interval $0 < t \leq DT$, the switch S_1 and diode D_1 are ON and the switch S_2 and diode D_2 are OFF. An ideal equivalent circuit for this time interval is shown in Figure 9.2(a). The voltage across the upper primary and the upper magnetizing inductance L_{m1} of the transformer is

$$v_1 = v_{Lm1} = -V_I, \tag{9.1}$$

which yields the voltage across the lower primary and the lower magnetizing inductance L_{m2},

$$v_2 = v_1 = -V_I. \tag{9.2}$$

The voltage across the upper secondary is

$$v_3 = -\frac{v_1}{n} = \frac{V_I}{n}, \tag{9.3}$$

and the voltage across the lower secondary is

$$v_4 = v_3 = \frac{V_I}{n}. \tag{9.4}$$

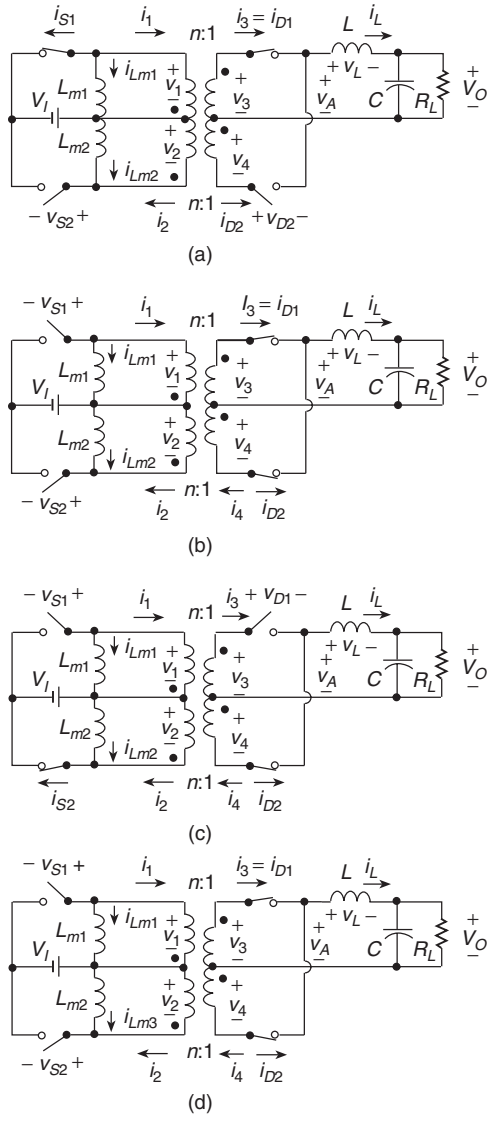


Figure 9.2 Equivalent circuit of the push-pull converter with a transformer center-tapped rectifier for CCM. (a) For $0 < t \le DT$. (b) For $DT < t \le T/2$. (c) For $T/2 < t \le T/2 + DT$. (d) For $T/2 + DT < t \le T$.

Hence, one obtains the voltage across the switch S_2,

$$v_{S2} = V_I - v_2 = V_I - (-V_I) = 2V_I, \tag{9.5}$$

and the voltage across the diode D_2,

$$v_{D2} = -(v_3 + v_4) = -\left(\frac{V_I}{n} + \frac{V_I}{n}\right) = -\frac{2V_I}{n}. \tag{9.6}$$

The voltage across the upper magnetizing inductance is

$$v_{Lm1} = v_1 = -V_I = L_{m1}\frac{di_{Lm1}}{dt}, \tag{9.7}$$

which yields the current through the upper magnetizing inductance,

$$i_{Lm1} = \frac{1}{L_{m1}}\int_0^t v_{Lm1}dt + i_{Lm1}(0) = \frac{1}{L_{m1}}\int_0^t (-V_I)\,dt + i_{Lm1}(0) = -\frac{V_I}{L_{m1}}t + i_{Lm1}(0). \quad (9.8)$$

Thus,

$$i_{Lm1}(DT) = -\frac{V_I DT}{L_{m1}} + i_{Lm1}(0) = -\frac{V_I D}{f_s L_{m1}} + i_{Lm1}(0), \quad (9.9)$$

$$\Delta i_{Lm1} = i_{Lm1}(0) - i_{Lm1}(DT) = \frac{V_I D}{f_s L_{m1}}, \quad (9.10)$$

$$i_{Lm1}(0) = \frac{\Delta i_{Lm1}}{2} = \frac{V_I D}{2 f_s L_{m1}}, \quad (9.11)$$

$$i_{Lm1}(DT) = -\frac{\Delta i_{Lm1}}{2} = -\frac{V_I D}{2 f_s L_{m1}}, \quad (9.12)$$

$$i_{Lm1} = -\frac{V_I}{L_{m1}}t + \frac{V_I D}{2 f_s L_{m1}}, \quad (9.13)$$

and

$$\Delta i_{Lm1(max)} = \frac{V_{Imax} D_{min}}{f_s L_{m1(min)}}. \quad (9.14)$$

The minimum magnetizing inductance is

$$L_{m1(min)} = \frac{D_{min} V_{Imax}}{f_s \Delta i_{Lm1(max)}}. \quad (9.15)$$

Likewise, the current through the lower magnetizing inductance L_{m2} is

$$i_{Lm2} = i_{Lm1} = -\frac{V_I}{L_{m2}}t + i_{Lm2}(0) = -\frac{V_I}{L_{m2}}t + \frac{V_I D}{2 f_s L_{m2}}. \quad (9.16)$$

The voltage at the input to the low-pass filter is

$$v_A = v_3 = \frac{V_I}{n}. \quad (9.17)$$

Therefore, the voltage across the inductor L is

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}, \quad (9.18)$$

which results in the current through the upper secondary, diode D_1, and inductor L,

$$i_3 = i_{D1} = i_L = \frac{1}{L}\int_0^t v_L\,dt + i_L(0) = \frac{1}{L}\int_0^t \left(\frac{V_I}{n} - V_O\right)dt + i_L(0) = \frac{\dfrac{V_I}{n} - V_O}{L}t + i_L(0). \quad (9.19)$$

Hence, the peak inductor current becomes

$$i_L(DT) = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} + i_L(0), \quad (9.20)$$

and the peak-to-peak value of the current ripple through inductor L is

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} = \frac{\left(\dfrac{V_I}{n} - V_O\right)D}{f_s L} = \frac{V_O(0.5 - D)}{f_s L}, \quad (9.21)$$

where $V_I = nV_O/(2D)$ as shown in Section 9.2.8.

The current through the upper primary is

$$i_1 = -\frac{i_3}{n} = -\frac{\frac{V_I}{n} - V_O}{nL}t - \frac{i_L(0)}{n}, \tag{9.22}$$

and the current through the switch S_1 is

$$i_{S1} = -i_1 - i_{Lm1} = \frac{\frac{V_I}{n} - V_O}{nL}t + \frac{i_L(0)}{n} + \frac{V_I}{L_{m1}}t - i_{Lm1}(0)$$

$$= \frac{\frac{V_I}{n} - V_O}{nL}t + \frac{i_L(0)}{n} + \frac{V_I}{L_{m1}}t - \frac{V_I D}{2f_s L_{m1}}. \tag{9.23}$$

9.2.4 Time Interval $DT < t \leq T/2$

Figure 9.2(b) shows an equivalent circuit of the push-pull converter for the time interval $DT < t \leq T/2$, during which both switches are OFF and both diodes are ON. The currents through the secondaries are equal in magnitude and flow in opposite directions, resulting in zero magnetic flux in the core. Therefore, the voltages across the transformer windings are

$$v_1 = v_2 = v_3 = v_4 = L_{m1}\frac{di_{Lm1}}{dt} = L_{m2}\frac{di_{Lm2}}{dt} = 0, \tag{9.24}$$

resulting in the currents through the magnetizing inductances,

$$i_{Lm1} = i_{Lm1}(DT) = -\frac{V_I D}{2f_s L_{m1}}, \tag{9.25}$$

$$i_{Lm2} = i_{Lm2}(DT) = -\frac{V_I D}{2f_s L_{m2}}, \tag{9.26}$$

and the voltages across the switches,

$$v_{S1} = v_{S2} = V_I. \tag{9.27}$$

The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{9.28}$$

which leads to the current through the inductor,

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L\, dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t} (-V_O)\, dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT), \tag{9.29}$$

and the currents through the diodes,

$$i_3 = i_{D1} = i_{D2} = -i_4 = \frac{i_L}{2} = -\frac{V_O}{2L}(t - DT) + \frac{i_L(DT)}{2}. \tag{9.30}$$

9.2.5 Time Interval $T/2 < t \leq T/2 + DT$

Figure 9.2(c) shows an equivalent circuit of the converter for the time interval $T/2 < t \leq T/2 + DT$, during which the switch S_1 and diode D_1 are OFF and the switch S_2 and diode

D_2 are ON. The voltage across the lower secondary and the lower magnetizing inductance L_{m1} is

$$v_2 = V_I, \tag{9.31}$$

from which

$$v_1 = v_2 = V_I, \tag{9.32}$$

$$v_3 = -\frac{v_1}{n} = -\frac{V_I}{n}, \tag{9.33}$$

and

$$v_4 = v_3 = -\frac{V_I}{n}. \tag{9.34}$$

Hence, one arrives at the voltage across the switch,

$$v_{S1} = V_I + v_1 = 2V_I, \tag{9.35}$$

and the voltage across the diode,

$$v_{D1} = v_3 + v_4 = -\frac{V_I}{n} - \frac{V_I}{n} = -\frac{2V_I}{n}. \tag{9.36}$$

The voltage across the lower magnetizing inductance L_{m2} is

$$v_{Lm2} = V_I = L_{m2}\frac{di_{Lm2}}{dt}, \tag{9.37}$$

resulting in the current through the lower magnetizing inductance,

$$\begin{aligned} i_{Lm2} &= \frac{1}{L_{m2}}\int_{T/2}^{t} v_{Lm2}\,dt + i_{Lm2}\left(\frac{T}{2}\right) = \frac{V_I}{L_{m2}}\left(t - \frac{T}{2}\right) + i_{Lm2}\left(\frac{T}{2}\right) \\ &= \frac{V_I}{L_{m2}}\left(t - \frac{T}{2}\right) - \frac{V_I D}{2f_s L_{m2}}. \end{aligned} \tag{9.38}$$

Similarly, the current through the upper magnetizing inductance L_{m1} is

$$i_{Lm1} = \frac{V_I}{L_{m1}}\left(t - \frac{T}{2}\right) + i_{Lm1}\left(\frac{T}{2}\right) = \frac{V_I}{L_{m1}}\left(t - \frac{T}{2}\right) - \frac{V_I D}{2f_s L_{m1}}. \tag{9.39}$$

The output filter input voltage is

$$v_A = \frac{V_I}{n}. \tag{9.40}$$

Therefore,

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}, \tag{9.41}$$

from which

$$i_{D2} = i_L = \frac{1}{L}\int_{T/2}^{t} v_L\,dt + i_L\left(\frac{T}{2}\right) = \frac{\dfrac{V_I}{n} - V_O}{L}\left(t - \frac{T}{2}\right) + i_L\left(\frac{T}{2}\right). \tag{9.42}$$

9.2.6 Time Interval $T/2 + DT < t \leq T$

An equivalent circuit of the converter for the time interval $T/2 + DT < t \leq T$ is shown in Figure 9.2(d). Both switches are OFF and both diodes are ON during this time interval.

This equivalent circuit is the same as that of Figure 9.2(b). Therefore, the analysis of the converter is the same as that given in Section 9.2.4. However, the magnetizing inductance currents are

$$i_{Lm1} = i_{Lm1}\left(\frac{T}{2} + DT\right) = \frac{V_I D}{2 f_s L_{m1}} \tag{9.43}$$

and

$$i_{Lm2} = i_{Lm2}\left(\frac{T}{2} + DT\right) = \frac{V_I D}{2 f_s L_{m2}}. \tag{9.44}$$

9.2.7 Device Stresses

The maximum peak voltage across each switch is

$$V_{SMmax} = 2V_{Imax}, \tag{9.45}$$

and the maximum peak current through each switch is

$$I_{SMmax} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Smax}}{2n} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} + \frac{\Delta i_{Lm1(max)}}{2}. \tag{9.46}$$

The maximum peak current through each diode is

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = I_{Omax} + \frac{V_O(0.5 - D_{min})}{2 f_s L}. \tag{9.47}$$

The maximum peak voltage across each diode for the center-tapped rectifier is

$$V_{DMmax} = \frac{2V_{Imax}}{n} \tag{9.48}$$

and for the bridge rectifier is

$$V_{DMmax} = \frac{V_{Imax}}{n}. \tag{9.49}$$

9.2.8 DC Voltage Transfer Function of Lossless Full-wave Converter for CCM

From Figure 9.3, the volt-second balance produces

$$\left(\frac{V_I}{n} - V_O\right) DT = V_O\left(\frac{1}{2} - D\right) T, \tag{9.50}$$

resulting in the dc voltage transfer function of the lossless converter,

$$M_{V\,DC} \equiv \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2D}{n}, \qquad \text{for } D < 0.5. \tag{9.51}$$

The range of $M_{V\,DC}$ is

$$0 \le M_{V\,DC} \le \frac{1}{n}. \tag{9.52}$$

For the lossless converter, the output voltage V_O is independent of the load resistance R_L and depends only on the dc input voltage V_I.

From (9.51), one obtains $V_I = nV_O/(2D)$. Substitution of this into (9.21) gives

$$\Delta i_L = \frac{V_O(\frac{1}{2} - D)}{f_s L}. \tag{9.53}$$

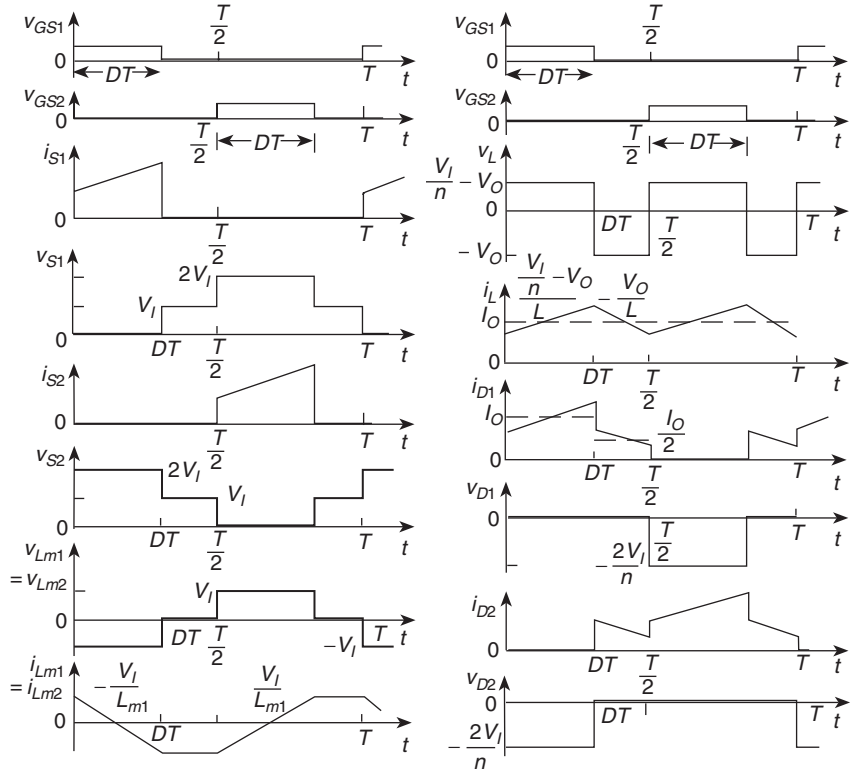


Figure 9.3 Waveforms in the push-pull converter for CCM.

The sensitivity of the output voltage with respect to the duty cycle is

$$S \equiv \frac{dV_O}{dD} = \frac{2V_I}{n}. \tag{9.54}$$

The dc current transfer function is

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n}{2D}. \tag{9.55}$$

As D is increased from 0 to 0.5, $M_{I\,DC}$ decreases from ∞ to n.

From (9.45), (9.46), and (9.51), $V_{SM} = nV_O/(2D)$ and $I_{SM} \approx I_O/n$, resulting in the switch utilization in the push-pull converter,

$$c_p \equiv \frac{P_O}{V_{SM}I_{SM}} = \frac{V_O I_O}{V_{SM}I_{SM}} \approx \frac{nV_O}{V_{SM}} = \frac{nV_O}{2V_I} = D. \tag{9.56}$$

As D is increased from 0 to 0.5, c_p increases from 0 to 0.5.

9.2.9 Boundary between CCM and DCM

The inductor current waveform at the CCM/DCM boundary is shown in Figure 9.4 and is given by

$$i_L = \frac{\dfrac{V_I}{n} - V_O}{L} t, \qquad \text{for } 0 < t \le DT, \tag{9.57}$$

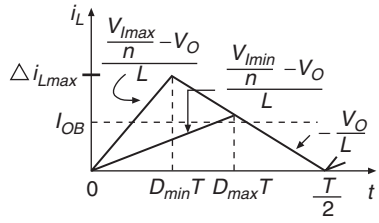


Figure 9.4 Waveform of the inductor current in the push-pull converter at the CCM/DCM boundary.

which produces the maximum peak-to-peak value of the inductor current ripple,

$$\Delta i_{Lmax} = i_L(D_{min}T) = \frac{\left(\frac{V_{Imax}}{n} - V_O\right) D_{min}T}{L_{min}} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{f_s L_{min}}. \tag{9.58}$$

The dc output current at the CCM/DCM boundary is

$$I_{OB} = I_{Omin} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s L_{min}} = \frac{V_O}{R_{Lmax}}. \tag{9.59}$$

The load resistance at the boundary is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L}{\frac{1}{2} - D}. \tag{9.60}$$

Hence, one arrives at the minimum value of the inductance L,

$$L_{min} = \frac{V_O\left(\frac{1}{2} - D_{min}\right)}{2f_s I_{Omin}} = \frac{R_{Lmax}\left(\frac{1}{2} - D_{min}\right)}{2f_s} = \frac{D_{min}\left(\frac{V_{Imax}}{n} - V_O\right)}{2f_s I_{Omin}}. \tag{9.61}$$

Figures 9.5 and 9.6 respectively show the normalized load current $I_{OB}/(V_O/2f_sL)$ and load resistance $R_{LB}/(2f_sL)$ at the CCM/DCM boundary as functions of the duty cycle D.

9.2.10 Ripple Voltage in Push-pull Converter for CCM

The minimum value of the filter capacitor is

$$C \geq C_{min} = \max\left\{\frac{D_{max}}{2r_C f_s}, \frac{\frac{1}{2} - D_{min}}{2r_C f_s}\right\}, \tag{9.62}$$

where $D_{max} \leq 0.5$. The ripple voltage is determined only by the ESR of the filter capacitor at any value of $D \leq 0.5$ if

$$C \geq C_{min} = \frac{1}{4r_C f_s}. \tag{9.63}$$

If condition (9.62) is met, the peak-to-peak ripple voltage V_r is given by

$$V_r = r_C \Delta i_{Lmax} = \frac{r_C V_O(\frac{1}{2} - D_{min})}{f_s L}. \tag{9.64}$$

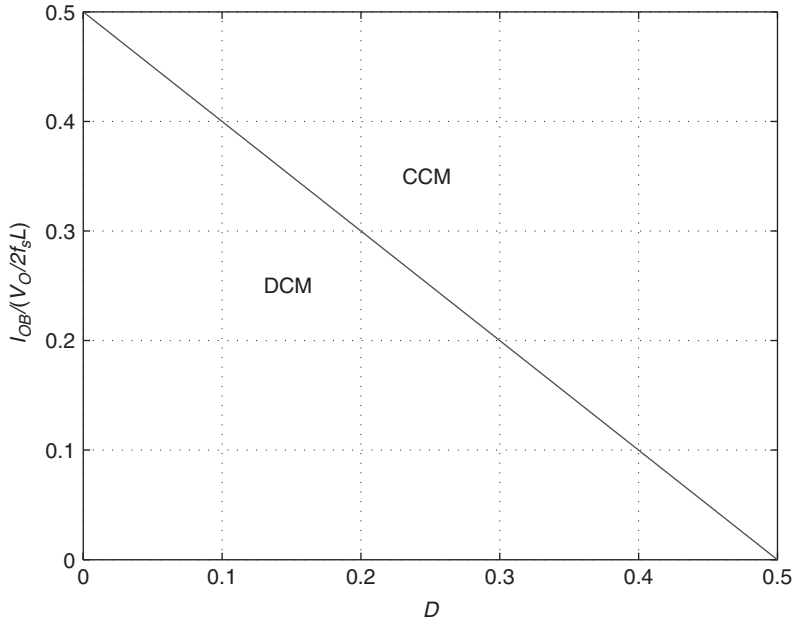


Figure 9.5 Normalized load current $I_{OB}/(V_O/2f_sL)$ at the CCM/DCM boundary for the push-pull converter.

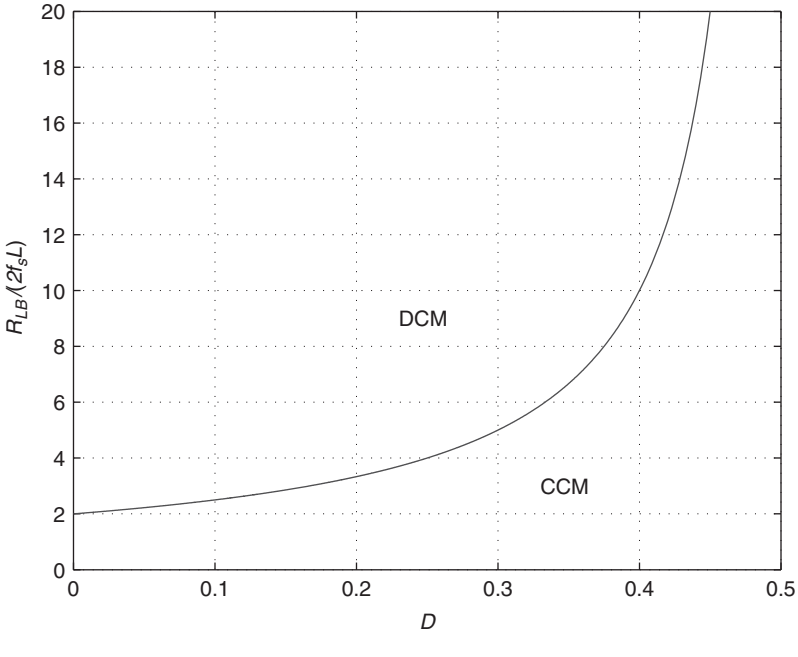


Figure 9.6 Normalized load resistance $R_{LB}/(2f_sL)$ at the CCM/DCM boundary for the push-pull converter.

If condition (9.62) is not met, the peak-to-peak ripple voltage depends on both the voltage drop across the filter capacitance and the ESR. The peak-to-peak voltage across the filter capacitance is

$$V_{Cpp} = \frac{\Delta Q}{C_{min}} = \frac{1}{2}\,\frac{T}{4}\,\frac{\Delta i_{Lmax}}{2}\,\frac{1}{C_{min}} = \frac{T\Delta i_{Lmax}}{16C_{min}} = \frac{\Delta i_{Lmax}}{16 f_s C_{min}} = \frac{V_O(\frac{1}{2} - D_{min})}{16 f_s^2 L C_{min}}$$
$$= \frac{(\frac{1}{2} - D_{min})V_O \pi^2 f_o^2}{4 f_s^2}, \tag{9.65}$$

from which

$$C_{min} = \frac{\Delta i_{Lmax}}{16 f_s V_{Cpp}} = \frac{V_O(\frac{1}{2} - D_{min})}{16 f_s V_{Cpp}}. \tag{9.66}$$

Hence, the output voltage can be approximated by

$$V_r \approx V_{Cpp} + V_{rcpp} = \frac{V_O(\frac{1}{2} - D_{min})}{16 f_s^2 LC} + \frac{r_C V_O(\frac{1}{2} - D_{min})}{f_s L}. \tag{9.67}$$

9.2.11 Power Losses and Efficiency of Push-pull Converter for CCM

Figure 9.7 shows an equivalent circuit of the push-pull converter with parasitic resistances, where r_{DS} is the MOSFET on-resistance, R_F is the diode forward resistance, V_F is the diode threshold voltage, r_L is the dc ESR of the inductor L, and r_C is the ESR of the filter capacitor C. The conduction losses will be determined assuming that the inductor ripple current is zero. Therefore, the inductor current can be approximated as

$$i_L \approx I_O. \tag{9.68}$$

The current through switch S_1 can be expressed as

$$i_{S1} = \begin{cases} \dfrac{I_O}{n}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T/2. \end{cases} \tag{9.69}$$

The rms current of switch S_1 is

$$I_{S1rms} = \sqrt{\frac{1}{T}\int_0^T i_{S1}^2\, dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{I_O}{n}\right)^2 dt} = \frac{I_O\sqrt{D}}{n}, \tag{9.70}$$

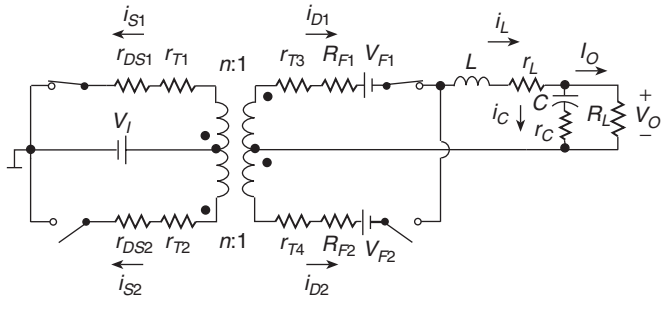


Figure 9.7 Equivalent circuit of the push-pull converter with parasitic components.

and the conduction loss in the upper MOSFET is

$$P_{rDS1} = r_{DS} I_{S1rms}^2 = \frac{D r_{DS} I_O^2}{n^2} = \frac{D r_{DS}}{n^2 R_L} P_O. \tag{9.71}$$

The conduction loss in the lower MOSFET P_{DS2} is the same as that in the upper transistor. Assuming that the transistor output capacitance C_o is linear, the switching loss per transistor is

$$P_{sw} = f_s C_o V_{SM}^2 = f_s C_o (2V_I)^2 = 4 f_s C_o V_I^2 = \frac{f_s C_o n^2 V_O^2}{D^2} = \frac{4 f_s C_o V_O^2}{M_{V\,DC}^2}$$

$$= \frac{f_s C_o n^2 R_L}{D^2} P_O = \frac{4 f_s C_o R_L}{M_{V\,DC}^2} P_O. \tag{9.72}$$

Hence, one obtains the total power dissipation in the MOSFET (excluding the drive power)

$$P_{FET} = P_{rDS} + \frac{P_{sw}}{2} = \frac{D r_{DS} I_O^2}{n^2} + 2 f_s C_o V_I^2 = \left(\frac{D r_{DS}}{n^2 R_L} + \frac{f_s C_o n^2 R_L}{2D^2} \right) P_O$$

$$= \left(\frac{D r_{DS}}{n^2 R_L} + \frac{2 f_s C_o R_L}{M_{V\,DC}^2} \right) P_O. \tag{9.73}$$

The rms current through the upper primary winding is the same as that of switch i_{S1}. Therefore, the conduction loss in the upper primary winding is

$$P_{rT1} = r_{T1} I_{T1rms}^2 = \frac{D r_{T1} I_O^2}{n^2} = \frac{D r_{T1}}{n^2 R_L} P_O. \tag{9.74}$$

The power in the lower primary winding is $P_{rT2} = P_{rT1}$.

The diode current can be approximated by

$$i_{D1} = \begin{cases} I_O, & \text{for } 0 < t \le DT, \\ \dfrac{I_O}{2}, & \text{for } DT < t \le T/2, \\ 0, & \text{for } T/2 < t \le T/2 + DT, \\ \dfrac{I_O}{2}, & \text{for } T/2 + DT < t \le T, \end{cases} \tag{9.75}$$

leading to its rms value

$$I_{D1rms} = \sqrt{\frac{1}{T} \int_0^T i_{D1}^2 \, dt} = \sqrt{\frac{1}{T} \left[\int_0^{DT} I_O^2 \, dt + 2 \int_{DT}^{T/2} \left(\frac{I_O}{2} \right)^2 dt \right]} = \frac{I_O \sqrt{2D+1}}{2}, \tag{9.76}$$

and the power loss in R_F,

$$P_{RF1} = R_F I_{D1rms}^2 = \frac{(2D+1) R_F I_O^2}{4} = \frac{(2D+1) R_F}{4 R_L} P_O. \tag{9.77}$$

The average value of the diode current is

$$I_D = \frac{1}{T} \int_0^T i_{D1} \, dt = \frac{I_O}{2} \tag{9.78}$$

which gives the power loss associated with the voltage V_F,

$$P_{VF1} = V_F I_D = \frac{V_F I_O}{2} = \frac{V_F}{2V_O} P_O. \tag{9.79}$$

Thus, the overall diode conduction loss is

$$P_{D1} = P_{RF1} + P_{VF1} = \frac{(2D+1)R_F I_O^2}{4} + \frac{V_F I_O}{2} = \left[\frac{(2D+1)R_F}{4R_L} + \frac{V_F}{2V_O}\right] P_O. \quad (9.80)$$

The power loss in diode D_2 is $P_{D2} = P_{D1}$.

The current through the upper secondary winding is the same as that through the diode D_1. Therefore, the conduction loss in the upper secondary winding is

$$P_{rT3} = r_{T3} I_{D1rms}^2 = \frac{(2D+1)r_{T3} I_O^2}{4} = \frac{(2D+1)r_{T3}}{4R_L} P_O. \quad (9.81)$$

The power of the lower secondary winding is $P_{rT4} = P_{rT3}$.

The rms inductor current is

$$I_{Lrms} \approx I_O, \quad (9.82)$$

and the inductor conduction loss is

$$P_{rL} = r_L I_{Lrms}^2 = r_L I_O^2 = \frac{r_L}{R_L} P_O. \quad (9.83)$$

The current through the filter capacitor is

$$i_C \approx i_L - I_O = \begin{cases} \dfrac{\Delta i_L}{DT} t - \dfrac{\Delta i_L}{2}, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L}{\left(\frac{1}{2} - D\right) T} + \dfrac{\Delta i_L}{2}, & \text{for } DT < t \le T/2. \end{cases} \quad (9.84)$$

Using (9.53) and (9.84), one can find the rms value of the current through the filter capacitor,

$$I_{Crms} = \sqrt{\frac{1}{(T/2)} \int_0^T i_C^2 \, dt} = \frac{\Delta i_L}{\sqrt{12}} = \frac{V_O(\frac{1}{2} - D)}{\sqrt{12} f_s L}, \quad (9.85)$$

and the power loss in the ESR of the filter capacitor,

$$P_{rC} = r_C I_{Crms}^2 = \frac{r_C (\Delta i_L)^2}{12} = \frac{r_C V_O^2 (\frac{1}{2} - D)^2}{12 f_s^2 L^2} = \frac{r_C R_L (\frac{1}{2} - D)^2}{12 f_s^2 L^2} P_O. \quad (9.86)$$

The overall power loss is given by

$$\begin{aligned} P_{LS} &= 2P_{rDS1} + 2P_{sw} + 2P_{rT1} + 2P_{rT3} + 2P_{D1} + P_{rL} + P_{rC} \\ &= \frac{2DI_O^2(r_{DS} + r_{T1})}{n^2} + 8 f_s C_o V_I^2 + \frac{(2D+1)(R_F + r_{T3}) I_O^2}{2} \\ &\quad + V_F I_O + r_L I_O^2 + \frac{r_C (\Delta i_L)^2}{12} \\ &= \left[\frac{2D(r_{DS} + r_{T1})}{n^2 R_L} + \frac{8 f_s C_o R_L}{M_{VDC}^2} + \frac{(2D+1)(R_F + r_{T3})}{2R_L} + \frac{V_F}{V_O} + \frac{r_L}{R_L} \right. \\ &\quad \left. + \frac{r_C R_L (\frac{1}{2} - D)^2}{12 f_s^2 L^2}\right] P_O. \end{aligned} \quad (9.87)$$

Thus, the efficiency of the push-pull converter for CCM is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}$$

$$= \frac{1}{1 + \dfrac{2D(r_{DS} + r_{T1})}{n^2 R_L} + \dfrac{8 f_s C_o R_L}{M_{V\,DC}^2} + \dfrac{(2D+1)(R_F + r_{T3})}{2R_L} + \dfrac{V_F}{V_O} + \dfrac{r_L}{R_L} + \dfrac{r_C R_L (\frac{1}{2} - D)^2}{12 f_s^2 L^2}}. \tag{9.88}$$

9.2.12 DC Voltage Transfer Function of Lossy Converter for CCM

The dc component of the input current is

$$I_I = \frac{1}{T/2}\int_0^{DT} i_{S1}\,dt = \frac{1}{T/2}\int_0^{DT}\left(\frac{I_O}{n}\right)dt = \frac{2DI_O}{n}, \tag{9.89}$$

leading to the dc current transfer function of the push-pull converter,

$$M_{I\,DC} \equiv \frac{I_O}{I_I} = \frac{n}{2D}. \tag{9.90}$$

This equation is valid for both lossless and lossy converters. The converter efficiency can be expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = M_{V\,DC} M_{I\,DC} = \frac{n M_{V\,DC}}{2D}, \tag{9.91}$$

from which the voltage transfer function of the lossy push-pull converter is

$$M_{V\,DC} = \frac{\eta}{M_{I\,DC}} = \frac{2\eta D}{n}$$

$$= \frac{D}{n\left[1 + \dfrac{2D(r_{DS} + r_{T1})}{n^2 R_L} + \dfrac{2 f_s C_o n^2 R_L}{D^2} + \dfrac{(2D+1)(R_F + r_{T3})}{2R_L} + \dfrac{V_F}{V_O} + \dfrac{r_L}{R_L} + \dfrac{r_C R_L\left(\frac{1}{2} - D\right)^2}{12 f_s^2 L^2}\right]}. \tag{9.92}$$

From (9.92), the on-duty cycle is

$$D = \frac{n M_{V\,DC}}{2\eta}. \tag{9.93}$$

For a given dc voltage transfer function, the duty cycle D is greater for the lossy converter than for the lossless converter.

Substituting (9.93) into (9.88), one obtains the efficiency of the push-pull converter

$$\eta = \frac{N_\eta}{D_\eta}, \tag{9.94}$$

where

$$N_\eta = 1 - n M_{V\,DC}\left(\frac{r_{DS} + r_{T1}}{n^2 R_L} + \frac{R_F + r_{T3}}{2R_L} - \frac{r_C R_L}{24 f_s^2 L^2}\right)$$

$$+\left\{\left[nM_{V\,DC}\left(\frac{r_{DS}+r_{T1}}{n^2R_L}+\frac{R_F+r_{T3}}{2R_L}-\frac{r_CR_L}{24f_s^2L^2}\right)-1\right]^2\right.$$
$$\left.-\frac{r_CR_Ln^2M_{V\,DC}^2}{12f_s^2L^2}\left[1+\frac{r_L}{R_L}+\frac{R_F+r_{T3}}{2R_L}+\frac{V_F}{V_O}+\frac{8f_sC_oR_L}{M_{V\,DC}^2}+\frac{r_CR_L}{48f_s^2L^2}\right]\right\}^{\frac{1}{2}} \quad (9.95)$$

and

$$D_\eta = 2\left(1+\frac{r_L}{R_L}+\frac{R_F+r_{T3}}{2R_L}+\frac{V_F}{V_O}+\frac{8f_sC_oR_L}{M_{V\,DC}^2}+\frac{r_CR_L}{48f_s^2L^2}\right). \quad (9.96)$$

9.2.13 Design of Push-pull Converter for CCM

Design a PWM push-pull converter operating in CCM to meet the following specifications: $V_{Inom} = \sqrt{2} \times 110 = 156\,\text{V}$, $V_{Imin} = \sqrt{2} \times 90 = 127\,\text{V}$, $V_{Imax} = \sqrt{2} \times 132 = 187\,\text{V}$, $V_O = 12\,\text{V}$, $I_{Omin} = 2\,\text{A}$, $I_{Omax} = 20\,\text{A}$, and $V_r/V_O \leq 1\,\%$.

Solution. The maximum and minimum values of the dc output power are

$$P_{Omax} = V_O I_{Omax} = 12 \times 20 = 240\,\text{W} \quad (9.97)$$

and

$$P_{Omin} = V_O I_{Omin} = 12 \times 2 = 24\,\text{W}. \quad (9.98)$$

The minimum and maximum values of the load resistance are

$$R_{Lmin} = \frac{V_O}{I_{Omax}} = \frac{12}{20} = 0.6\,\Omega \quad (9.99)$$

and

$$R_{Lmax} = \frac{V_O}{I_{Omin}} = \frac{12}{2} = 6\,\Omega. \quad (9.100)$$

The minimum, nominal, and maximum values of the dc voltage transfer function are

$$M_{V\,DCmin} = \frac{V_O}{V_{Imax}} = \frac{12}{187} = 0.06417 = \frac{1}{15.58}, \quad (9.101)$$

$$M_{V\,DCnom} = \frac{V_O}{V_{Inom}} = \frac{12}{156} = 0.07692 = \frac{1}{13}, \quad (9.102)$$

and

$$M_{V\,DCmax} = \frac{V_O}{V_{Imin}} = \frac{12}{127} = 0.09449 = \frac{1}{10.58}. \quad (9.103)$$

Assume initially that $D_{max} \approx 0.4$ and $\eta = 85\,\%$. From (9.93), the transformer turns ratio is

$$n = \frac{2\eta D_{max}}{M_{V\,DCmax}} = \frac{2 \times 0.85 \times 0.4}{0.09449} = 7.2. \quad (9.104)$$

Pick $n = 7$. The minimum, nominal, and maximum values of the duty cycle are

$$D_{min} = \frac{nM_{V\,DCmin}}{2\eta} = \frac{7 \times 0.06417}{2 \times 0.85} = 0.2642, \quad (9.105)$$

$$D_{nom} = \frac{nM_{V\,DCnom}}{2\eta} = \frac{7 \times 0.07692}{2 \times 0.85} = 0.3167, \quad (9.106)$$

and

$$D_{max} = \frac{nM_{DCmax}}{2\eta} = \frac{7 \times 0.09449}{2 \times 0.85} = 0.3891. \tag{9.107}$$

Assume the switching frequency is $f_s = 100\,\text{kHz}$. The minimum inductance required to maintain the converter in CCM is

$$L_{min} = \frac{R_{Lmax}(\frac{1}{2} - D_{min})}{2f_s} = \frac{6 \times (\frac{1}{2} - 0.2642)}{2 \times 100 \times 10^3} = 7.074\,\mu\text{H}. \tag{9.108}$$

Let $L = 10\,\mu\text{H}$.

The maximum ripple of the inductor current is

$$\Delta i_{Lmax} = \frac{V_O(\frac{1}{2} - D_{min})}{f_s L} = \frac{12 \times (\frac{1}{2} - 0.2642)}{100 \times 10^3 \times 10 \times 10^{-6}} = 2.83\,\text{A}. \tag{9.109}$$

The ripple voltage is

$$V_r = \frac{V_O}{100} = \frac{12}{100} = 120\,\text{mV}. \tag{9.110}$$

If the filter capacitance is large enough, $V_r = r_{Cmax}\Delta i_{Lmax}$ and the maximum ESR of the filter capacitor is

$$r_{Cmax} = \frac{V_r}{\Delta i_{Lmax}} = \frac{120 \times 10^{-3}}{2.83} = 42.4\,\text{m}\Omega. \tag{9.111}$$

Pick a capacitor with $r_C = 30\,\text{m}\Omega$.

The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is

$$C_{min} = \max\left\{\frac{D_{max}}{2f_s r_C}, \frac{\frac{1}{2} - D_{min}}{2f_s r_C}\right\} = \max\left\{\frac{0.3891}{2f_s r_C}, \frac{\frac{1}{2} - 0.2642}{2f_s r_C}\right\} = \frac{D_{max}}{2f_s r_C}$$

$$= \frac{0.3891}{2 \times 100 \times 10^3 \times 30 \times 10^{-3}} = 64.85\,\mu\text{F}. \tag{9.112}$$

Pick $C = 100\,\mu\text{F}/25\,\text{V}/30\,\text{m}\Omega$.

The voltage and current stresses of the diodes in the center-tapped rectifier are

$$V_{DMmax} = \frac{2V_{Imax}}{n} = \frac{2 \times 187}{7} = 53.429\,\text{V} \tag{9.113}$$

and

$$I_{DMmax} = I_{Omax} + \frac{\Delta i_{Lmax}}{2} = 20 + \frac{2.83}{2} = 21.415\,\text{A}. \tag{9.114}$$

The maximum peak current through the ideal transformer primary is

$$I_{1max} = \frac{I_{DMmax}}{n} = \frac{21.415}{7} = 3.059\,\text{A}. \tag{9.115}$$

Assuming that the peak-to-peak current through the upper magnetizing inductance is less than 10 % of the maximum peak current through the ideal transformer primary, we have

$$\Delta i_{Lm1(max)} = 0.1I_{1max} = 0.1 \times 3.059 = 0.306\,\text{A}. \tag{9.116}$$

Thus, the minimum magnetizing inductance is

$$L_{m1(min)} = \frac{D_{min}V_{Imax}}{f_s \Delta i_{Lm1(max)}} = \frac{0.2642 \times 187}{100 \times 10^3 \times 0.306} = 1.615\,\text{mH}. \tag{9.117}$$

Pick $L_{m1} = L_{m2} = 1.65\,\text{mH}$.

The voltage and current stresses of the power MOSFETs are

$$V_{SMmax} = 2V_{Imax} = 2 \times 187 = 374\,\text{V} \tag{9.118}$$

and

$$I_{SMmax} = \frac{I_{Omax}}{n} + \frac{\Delta i_{Lmax}}{2n} + \frac{\Delta i_{Lm1(max)}}{2} = \frac{20}{7} + \frac{2.83}{2 \times 7} + \frac{0.306}{2} = 3.212\,\text{A}. \tag{9.119}$$

MTM15N40 power MOSFETs are selected, which have $V_{DSS} = 400\,\text{V}$, $I_{SM} = 15\,\text{A}$ of continuous current, $r_{DS} = 300\,\text{m}\Omega$, $Q_g = 110\,\text{nC}$, and $C_o = 100\,\text{pF}$. MBR2545CT Schottky diodes are also selected, which have $I_{D(AV)max} = 25\,\text{A}$, $I_{FSM} = 150\,\text{A}$, $V_{DM} = 45\,\text{V}$, $V_F = 0.3\,\text{V}$, and $R_F = 20\,\text{m}\Omega$.

The power losses and the efficiency will be calculated for $I_{Omax} = 20\,\text{A}$ and $V_{Imin} = 127\,\text{V}$. The conduction power loss in each MOSFET is

$$P_{rDS1} = \frac{D_{max} r_{DS} I_{Omax}^2}{n^2} = \frac{0.3891 \times 0.3 \times 20^2}{7^2} = 0.953\,\text{W}, \tag{9.120}$$

and the switching loss associated with the turn-on and turn-off of each transistor is

$$P_{sw} = 4 f_s C_o V_{Imin}^2 = 4 \times 100 \times 10^3 \times 100 \times 10^{-12} \times 127^2 = 0.645\,\text{W}. \tag{9.121}$$

The overall power loss in each transistor is

$$P_{MOS} = P_{rDS1} + \frac{P_{sw}}{2} = 0.953 + \frac{0.645}{2} = 1.276\,\text{W}. \tag{9.122}$$

Assuming that the resistances of the primary windings are $r_{T1} = r_{T2} = 50\,\text{m}\Omega$ and the resistances of the secondary windings are $r_{T3} = r_{T4} = 20\,\text{m}\Omega$, then the conduction loss in one of the transformer primary windings is

$$P_{rT1} = \frac{D_{max} r_{T1} I_{Omax}^2}{n^2} = \frac{0.3891 \times 0.05 \times 20^2}{7^2} = 0.159\,\text{W}, \tag{9.123}$$

and the conduction loss in one of the transformer secondary windings is

$$P_{rT3} = \frac{(2D_{max} + 1) r_{T3} I_{Omax}^2}{4} = \frac{(2 \times 0.3891 + 1) \times 0.02 \times 20^2}{4} = 3.556\,\text{W}. \tag{9.124}$$

Hence, the overall conduction power loss in the transformer windings is

$$P_{tr} = 2P_{rT1} + 2P_{rT3} = 2 \times 0.159 + 2 \times 3.556 = 7.43\,\text{W}. \tag{9.125}$$

The conduction loss in the diode due to R_F is

$$P_{RF1} = \frac{(2D_{max} + 1) R_F I_{Omax}^2}{4} = \frac{(2 \times 0.3891 + 1) \times 0.02 \times 20^2}{4} = 3.556\,\text{W}, \tag{9.126}$$

the conduction loss in the diode due to V_F is

$$P_{VF1} = \frac{V_F I_{Omax}}{2} = \frac{0.3 \times 20}{2} = 3\,\text{W}, \tag{9.127}$$

and the total conduction loss in each diode is

$$P_{D1} = P_{RF1} + P_{VF1} = 3.556 + 3 = 6.556\,\text{W}. \tag{9.128}$$

Assuming that the ESR of the dc inductor is $r_L = 25\,\text{m}\Omega$,

$$P_{rL} = r_L I_{Omax}^2 = 0.025 \times 20^2 = 10\,\text{W}. \tag{9.129}$$

The power loss in the capacitor ESR is

$$P_{rC} = \frac{r_C(\Delta i_{Lmax})^2}{12} = \frac{0.03 \times 2.83^2}{12} = 0.02\,\text{W}. \tag{9.130}$$

The total power loss is

$$\begin{aligned} P_{LS} &= 2P_{rDS1} + 2P_{sw} + 2P_{rT1} + 2P_{rT3} + 2P_{D1} + P_{rL} + P_{rC} \\ &= 2 \times 0.953 + 2 \times 0.645 + 2 \times 0.159 + 2 \times 3.556 + 2 \times 6.556 + 10 + 0.02 \\ &= 33.758\,\text{W} \end{aligned} \tag{9.131}$$

and the efficiency of the converter at full load is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{240}{240 + 33.758} = 87.67\,\%. \tag{9.132}$$

The zero-to-peak gate-to-source voltage is $V_{GSm} = 7\,\text{V}$. Hence, the gate-drive power per transistor is found as

$$P_G = f_s V_{GSm} Q_g = 100 \times 10^3 \times 7 \times 110 \times 10^{-9} = 77\,\text{mW}. \tag{9.133}$$

Figures 9.8–9.13 show the characteristics of the converter designed.

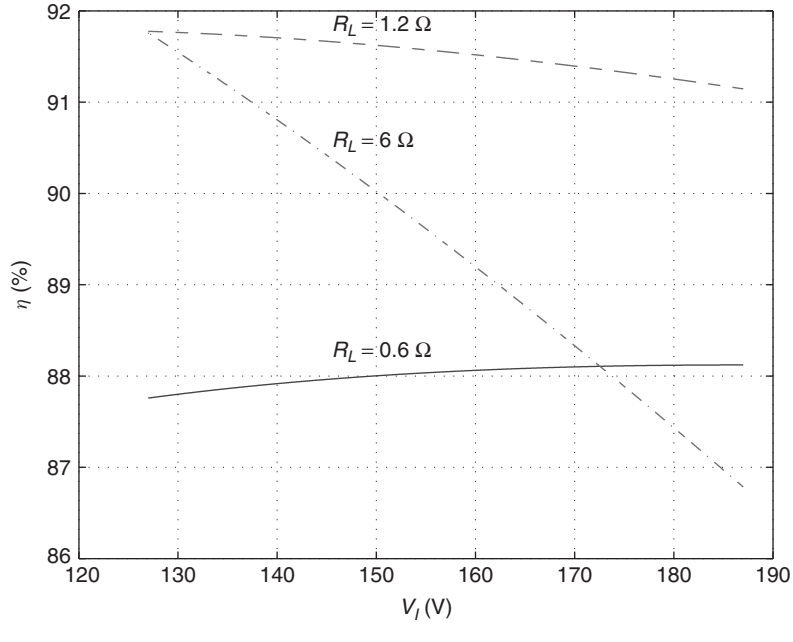


Figure 9.8 Efficiency η as function of the dc input voltage V_I at fixed load resistances R_L for the push-pull converter in CCM.

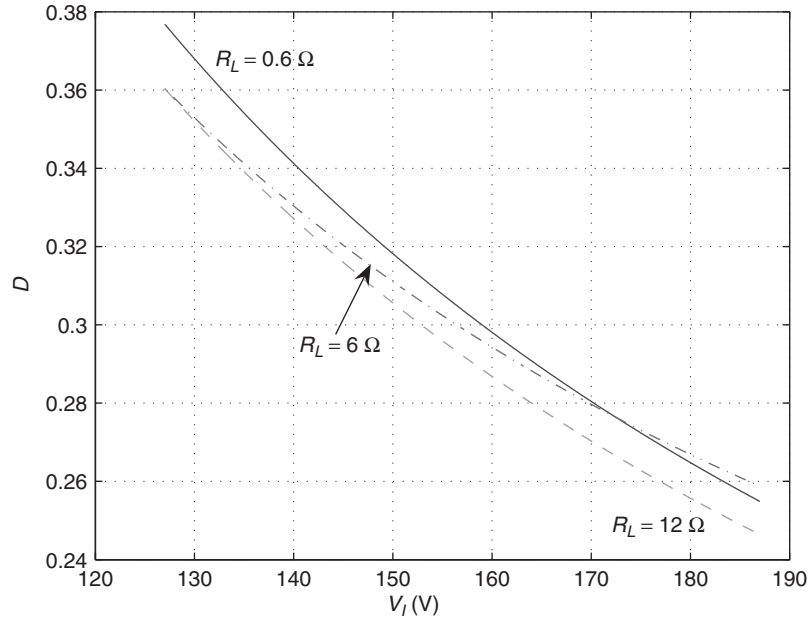


Figure 9.9 Duty cycle D as function of the dc input voltage V_I at fixed load resistances R_L for the push-pull converter in CCM.

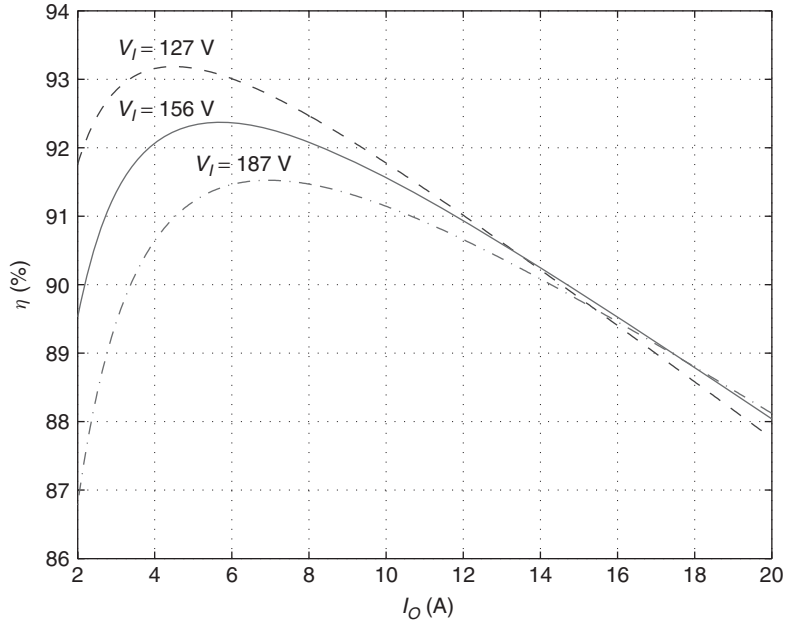


Figure 9.10 Efficiency η as function of the dc load current I_O at fixed input voltages V_I for the push-pull converter in CCM.

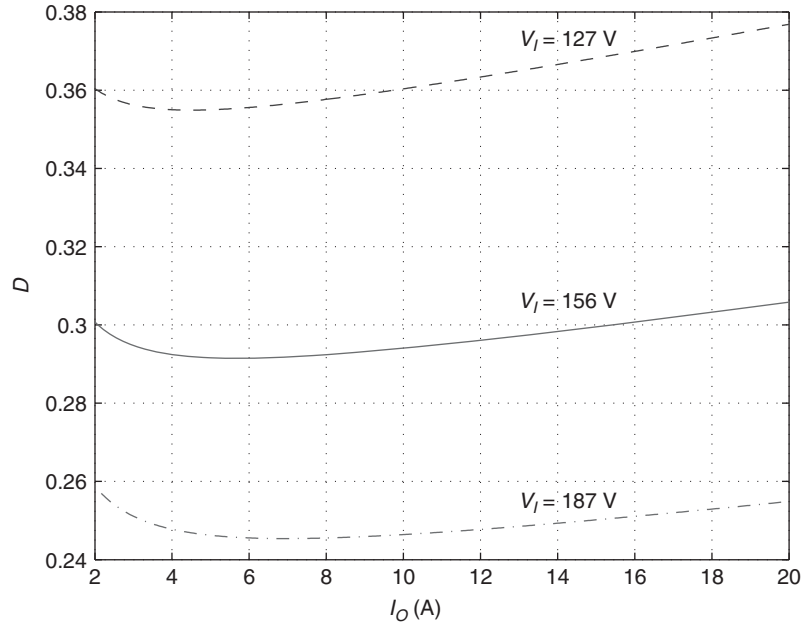


Figure 9.11 Duty cycle D as function of the dc load current I_O at fixed input voltages V_I for the push-pull converter in CCM.

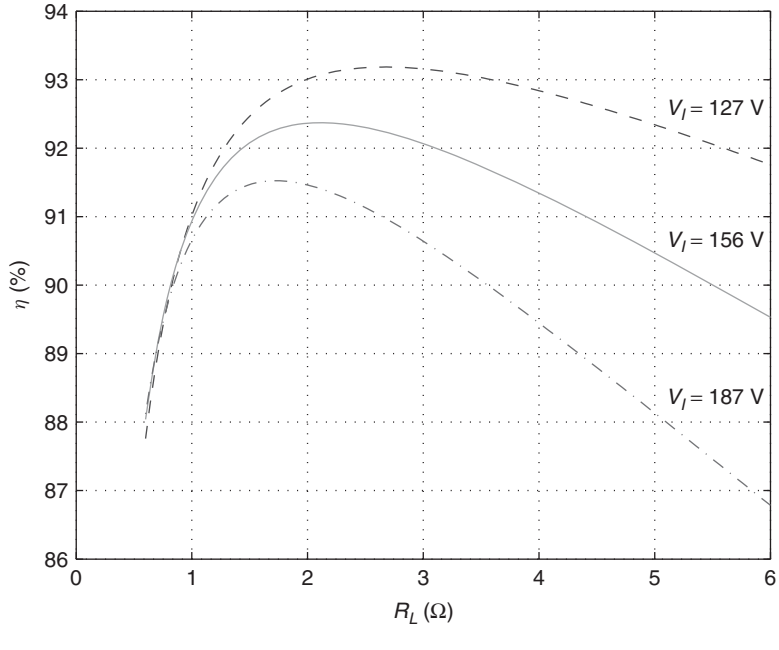


Figure 9.12 Efficiency η as function of the load resistance R_L at fixed input voltages V_I for the push-pull converter in CCM.

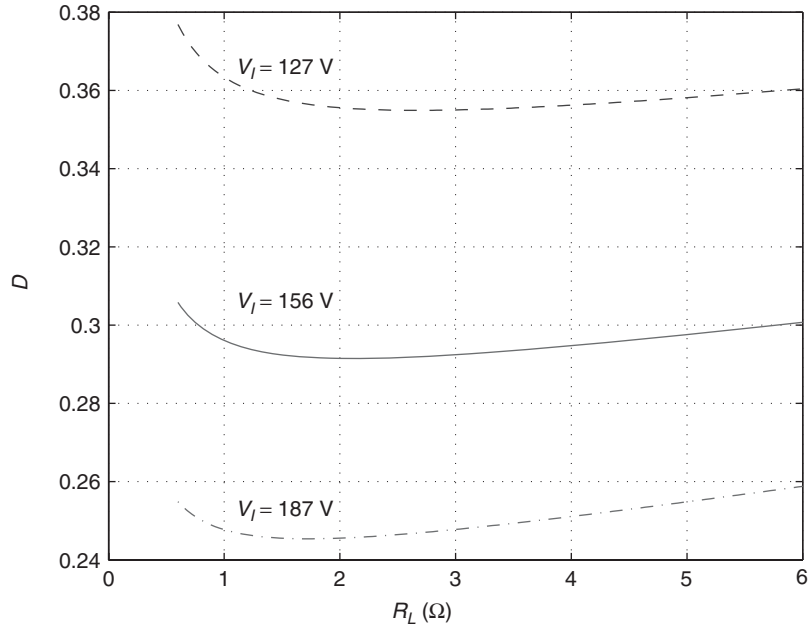


Figure 9.13 Duty cycle D as function of the load resistance R_L at fixed input voltages V_I for the push-pull converter in CCM.

9.3 DC Analysis of PWM Push-pull Converter for DCM

9.3.1 Time Interval $0 < t \leq DT$

During this time interval, the switch S_1 and diode D_1 are ON and the switch S_2 and diode D_2 are OFF. The equivalent circuit is shown in Figure 9.14(a). The voltages across the transformer windings are

$$v_1 = -V_I, \tag{9.134}$$

$$v_2 = v_1 = -V_I, \tag{9.135}$$

$$v_3 = -\frac{v_1}{n} = \frac{V_I}{n}, \tag{9.136}$$

$$v_4 = v_3 = \frac{V_I}{n}. \tag{9.137}$$

The voltage across the switch S_2 is

$$v_{S2} = -(v_1 + v_2) = 2V_I, \tag{9.138}$$

and the voltage across the diode D_2 is

$$v_{D2} = -(v_3 + v_4) = -\frac{2V_I}{n}. \tag{9.139}$$

The voltage across the magnetizing inductance L_{m1} is

$$v_{Lm1} = v_1 = -V_I = L_{m1}\frac{di_{Lm1}}{dt}, \tag{9.140}$$

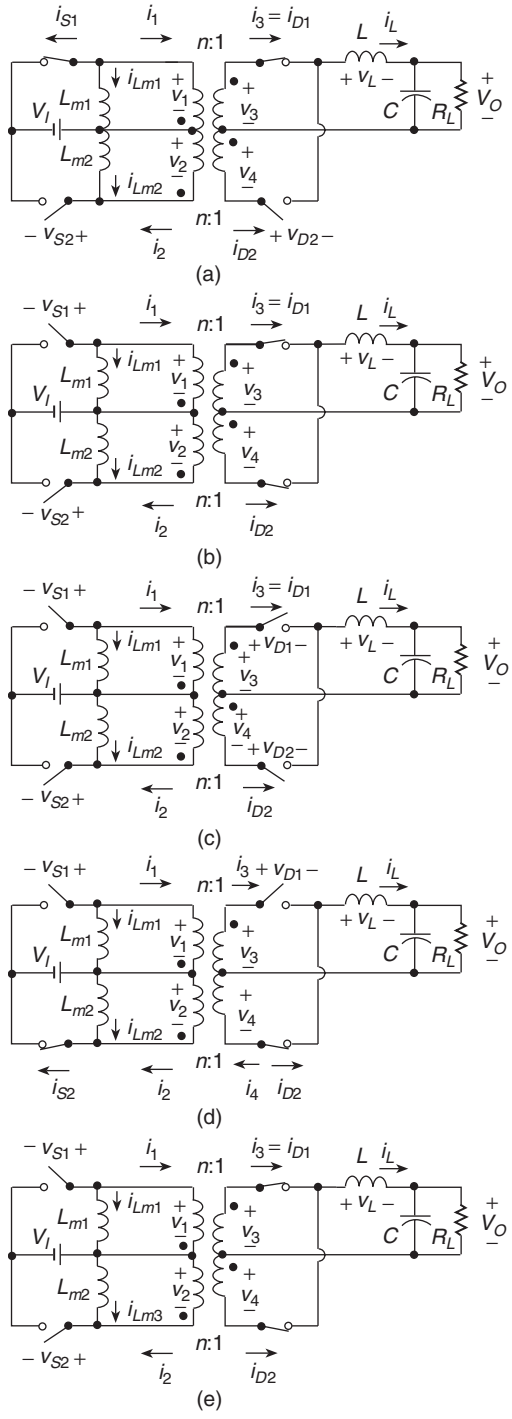


Figure 9.14 Equivalent circuit of the push-pull converter with a transformer center-tapped rectifier for DCM. (a) For $0 < t \le DT$. (b) For $DT < t \le (D + D_1)T$. (c) For $(D + D_1)T \le T/2$. (d) For $T/2 < t \le T/2 + DT$. (e) For $(T/2 + DT \le t \le T/2 + (D + D_1)T$.

which gives

$$i_{Lm1} = \frac{1}{L_{m1}} \int_0^t v_{Lm1}\, dt + i_{Lm1}(0) = -\frac{V_I}{L_{m1}} t + i_{Lm1}(0). \tag{9.141}$$

Hence,

$$i_{Lm1}(DT) = -\frac{V_I DT}{L_{m1}} t + i_{Lm1}(0) = -\frac{V_I D}{f_s L_{m1}} t + i_{Lm1}(0), \tag{9.142}$$

$$\Delta i_{Lm1} = i_{Lm1}(0) - i_{Lm1}(DT) = \frac{V_I D}{f_s L_{m1}}, \tag{9.143}$$

$$i_{Lm1}(0) = \frac{\Delta i_{Lm1}}{2} = \frac{V_I D}{2 f_s L_{m1}}, \tag{9.144}$$

and

$$i_{Lm1}(DT) = -\frac{\Delta i_{Lm1}}{2} = -\frac{V_I D}{2 f_s L_{m1}}. \tag{9.145}$$

The current i_{Lm2} through the magnetizing inductance L_{m2} is equal to the current i_{Lm1}.

The voltage across the inductor L is

$$v_L = \frac{V_I}{n} - V_O = L\frac{di_L}{dt}, \qquad i_L(0) = 0, \tag{9.146}$$

and the inductor and switch current is

$$i_3 = i_{D1} = i_L = \frac{1}{L} \int_0^t v_L\, dt = \frac{1}{L} \int_0^t \left(\frac{V_I}{n} - V_O \right) dt = \frac{\dfrac{V_I}{n} - V_O}{L} t. \tag{9.147}$$

Hence, the peak inductor current is

$$\Delta i_L = i_L(DT) = I_{DM} = \frac{\left(\dfrac{V_I}{n} - V_O \right) DT}{L} = \frac{\left(\dfrac{V_I}{n} - V_O \right) D}{f_s L}. \tag{9.148}$$

The current through the primary is

$$i_1 = -\frac{i_3}{n} = -\frac{\dfrac{V_I}{n} - V_O}{nL} t. \tag{9.149}$$

This leads to the switch current

$$i_{S1} = -i_1 - i_{Lm1} = \frac{\dfrac{V_I}{n} - V_O}{nL} t + \frac{V_I}{L_{m1}} t - i_{Lm1}(0). \tag{9.150}$$

Voltage and current waveforms for DCM are depicted in Figure 9.15.

9.3.2 Time Interval $DT < t \leq (D + D_1)T$

The equivalent circuit for this time interval is shown in Figure 9.14(b). Both switches are OFF and both diodes are ON. The currents through the secondaries flow in opposite directions and are equal in magnitude. Therefore, the magnetic flux in the core is zero and the voltages across the transformer windings are

$$v_1 = v_2 = v_3 = v_4 = L_{m1}\frac{di_{Lm1}}{dt} = L_{m2}\frac{di_{Lm2}}{dt} = 0, \tag{9.151}$$

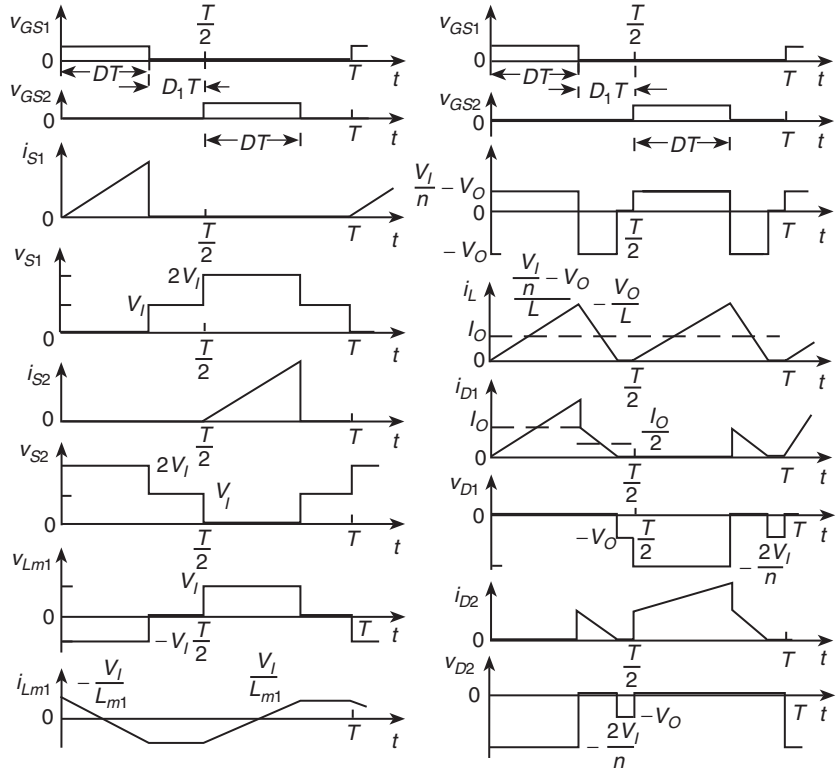


Figure 9.15 Waveforms in the push-pull converter with a transformer center-tapped rectifier for DCM.

which gives the currents through the magnetizing inductances,

$$i_{Lm1} = i_{Lm1}(DT) = -\frac{V_I D}{2 f_s L_{m1}}, \tag{9.152}$$

$$i_{Lm2} = i_{Lm2}(DT) = -\frac{V_I D}{2 f_s L_{m2}}, \tag{9.153}$$

and the voltages across the switches,

$$v_{S1} = v_{S2} = V_I. \tag{9.154}$$

The voltage across the inductor L is

$$v_L = -V_O = L\frac{di_L}{dt}, \tag{9.155}$$

and the inductor and diode current is

$$i_L = \frac{1}{L}\int_{DT}^{t} v_L\, dt + i_L(DT) = \frac{1}{L}\int_{DT}^{t} (-V_O)\, dt + i_L(DT) = -\frac{V_O}{L}(t - DT) + i_L(DT)$$

$$= -\frac{V_O}{L}(t - DT) + \frac{\left(\dfrac{V_I}{n} - V_O\right) DT}{L}. \tag{9.156}$$

The peak inductor current is found to be

$$\Delta i_L = -\frac{1}{L}\int_{(D+D_1)T}^{DT} v_L\,dt = -\frac{1}{L}\int_{(D+D_1)T}^{DT}(-V_O)\,dt = \frac{V_O D_1 T}{L}. \tag{9.157}$$

The diode currents are

$$i_3 = -i_4 = i_{D1} = i_{D2} = \frac{i_L}{2} = -\frac{V_O}{2L}(t - DT) + \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{2L}. \tag{9.158}$$

The peak voltage across the switch is

$$V_{SM} = V_I. \tag{9.159}$$

This time interval ends when the diode current reaches zero.

9.3.3 Time Interval $(D + D_1)T < t \le T/2$

During this time interval, both switches and both diodes are OFF. The equivalent circuit is shown in Figure 9.14(c). The inductor current i_L, inductor voltage v_L, switch currents i_{S1} and i_{S2}, and diode currents i_{D1} and i_{D2} are zero. The voltages across the switches are

$$v_{S1} = v_{S2} = V_I, \tag{9.160}$$

and the voltages across the diodes are

$$v_{D1} = v_{D2} = -V_O. \tag{9.161}$$

The magnetizing currents remain the same as those in the previous time interval. The equivalent circuits for the second half of the period are shown in Figure 9.14(d)–(e).

9.3.4 DC Voltage Transfer Function for DCM

Referring to Figure 9.15 and using the volt-second balance,

$$\left(\frac{V_I}{n} - V_O\right)DT = V_O D_1 T, \tag{9.162}$$

which leads to

$$M_{V\,DC} = \frac{V_O}{V_I} = \frac{D}{n(D + D_1)}. \tag{9.163}$$

From (9.148) and (9.163), the peak-to-peak current is

$$\Delta i_L = \frac{\left(\dfrac{V_I}{n} - V_O\right)DT}{L} = \frac{V_O D(1 - nM_{V\,DC})}{nM_{V\,DC} f_s L}. \tag{9.164}$$

Using (9.163) and (9.164),

$$I_O = \frac{1}{T/2}\int_0^{T/2} i_L\,dt = (D + D_1)\Delta i_L = \frac{DV_O(D + D_1)(1 - nM_{V\,DC})}{nM_{V\,DC} f_s L}$$

$$= \frac{V_O D^2(1 - nM_{V\,DC})}{n^2 M_{V\,DC}^2 f_s L}. \tag{9.165}$$

Hence,

$$D = \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L I_O}{(1 - nM_{V\,DC})V_O}}$$

$$= \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L}{(1 - nM_{V\,DC})R_L}}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_s L}{R_L} = \frac{1}{2} - \frac{2f_s L I_O}{V_O}. \tag{9.166}$$

At the CCM/DCM boundary, the relationship between $M_{V\,DC}$ and D is still valid and is given by

$$M_{V\,DCB} = \frac{2D_B}{n}. \tag{9.167}$$

Substitution of this into (9.166) yields the duty cycle D_B at the boundary,

$$D_B = \frac{1}{2} - \frac{2f_s L}{R_L} = \frac{1}{2} - \frac{2f_s L I_O}{V_O}. \tag{9.168}$$

Figures 9.16 and 9.17 respectively depict plots of D versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of $nM_{V\,DC}$ for both CCM and DCM for the lossless push-pull converter.

Using (9.166), one obtains

$$\frac{f_s L}{D^2 R_L} n^2 M_{V\,DC}^2 + nM_{V\,DC} - 1 = 0. \tag{9.169}$$

Solving this equation for $M_{V\,DC}$ gives

$$M_{V\,DC} = \frac{2}{n\left(1 + \sqrt{1 + \dfrac{4f_s L}{D^2 R_L}}\right)}$$

$$= \frac{2}{n\left(1 + \sqrt{1 + \dfrac{4f_s L I_O}{D^2 V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2f_s L}{R_L} = \frac{1}{2} - \frac{2f_s L I_O}{V_O}. \tag{9.170}$$

Figures 9.18 and 9.19 respectively show $nM_{V\,DC}$ versus normalized load current $I_O/(V_O/2f_sL)$ and normalized load resistance $R_L/(2f_sL)$ at various values of D for both CCM and DCM for the lossless push-pull converter. The dc voltage transfer function $M_{V\,DC}$ is dependent on D, R_L, L, and f_s for DCM.

The dc input current is given by

$$i_I = i_{S1} = -(i_1 + i_{Lm}) \approx -i_1 = \frac{\dfrac{V_I}{n} - V_O}{nL} t, \qquad \text{for } 0 < D \le DT. \tag{9.171}$$

Hence, the dc input power is

$$I_I = \frac{1}{T/2} \int_0^{DT} i_I \, dt = \frac{1}{T/2} \int_0^{DT} \frac{\dfrac{V_I}{n} - V_O}{nL} t \, dt = \frac{D^2 \left(\dfrac{V_I^2}{n} - V_I V_O\right)}{nf_s L}, \tag{9.172}$$

yielding the dc input power

$$P_I = V_I I_I = \frac{D^2 \left(\dfrac{V_I^2}{n} - V_I V_O\right)}{nf_s L}. \tag{9.173}$$

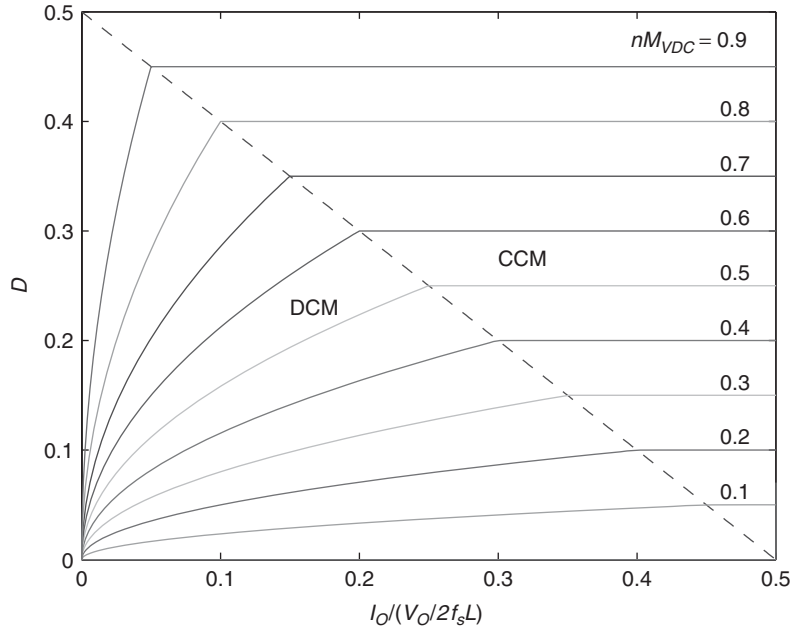


Figure 9.16 D as a function of normalized load current $I_O/(I_O/2f_sL)$ at fixed values of $nM_{V\,DC}$ for the lossless push-pull converter.

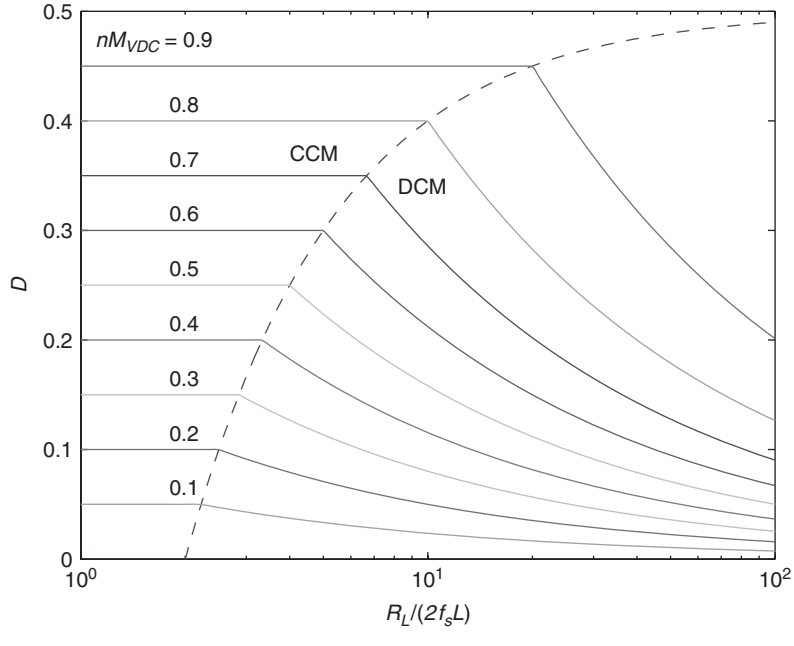


Figure 9.17 D as a function of normalized load resistance $R_L/(2f_sL)$ at fixed values of $nM_{V\,DC}$ for the lossless push-pull converter.

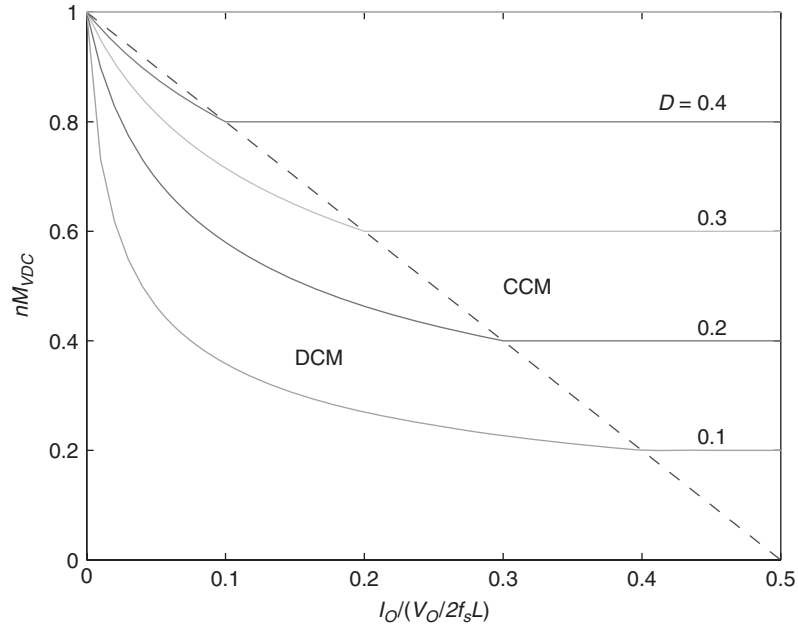


Figure 9.18 $nM_{V\,DC}$ as a function of normalized load current $I_O/(V_O/2f_sL)$ at fixed values of D for the lossless push-pull converter.

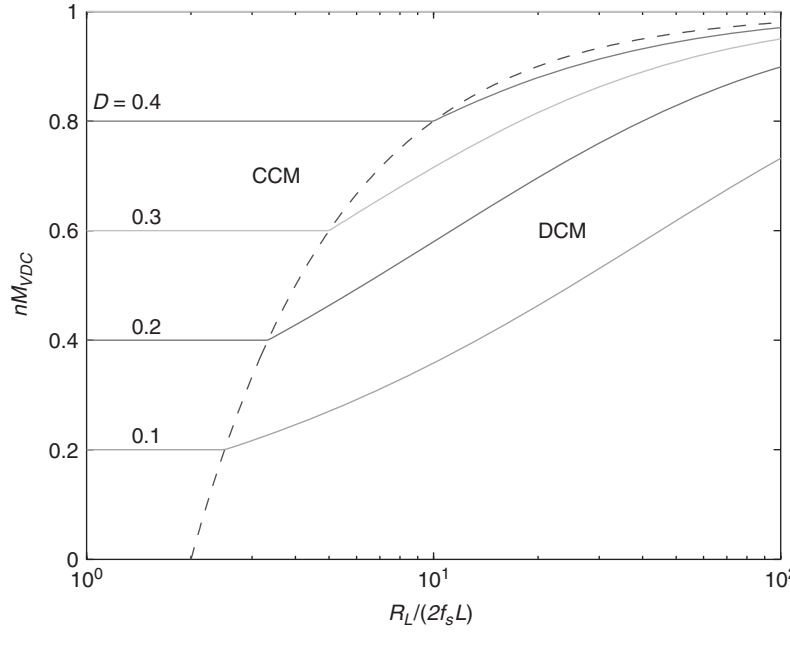


Figure 9.19 $nM_{V\,DC}$ as a function of normalized load resistance $R_L/(2f_sL)$ at fixed values of D for the lossless push-pull converter.

The dc output power is

$$P_O = \frac{V_O^2}{R_L}. \tag{9.174}$$

The efficiency of the push-pull converter is

$$\eta = \frac{P_O}{P_I} = \frac{f_s L n^2 M_{V\,DC}^2}{D^2 R_L (1 - n M_{V\,DC})}. \tag{9.175}$$

Hence, one arrives at the duty cycle of the lossy push-pull converter in DCM,

$$\begin{aligned} D &= \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L}{\eta R_L (1 - n M_{V\,DC})}} \\ &= \sqrt{\frac{n^2 M_{V\,DC}^2 f_s L I_O}{\eta V_O (1 - n M_{V\,DC})}}, \quad \text{for } D \le \frac{1}{2} - \frac{2 f_s L}{R_L} = \frac{1}{2} - \frac{2 f_s L I_O}{V_O}, \end{aligned} \tag{9.176}$$

and the dc voltage transfer function of the lossy push-pull converter for DCM,

$$\begin{aligned} M_{V\,DC} &= \frac{2}{n\left(1 + \sqrt{1 + \dfrac{4 f_s L}{\eta D^2 R_L}}\right)} \\ &= \frac{2}{n\left(1 + \sqrt{1 + \dfrac{4 f_s L I_O}{\eta D^2 V_O}}\right)}, \quad \text{for } D \le \frac{1}{2} - \frac{2 f_s L}{R_L} = \frac{1}{2} - \frac{2 f_s L I_O}{V_O}. \end{aligned} \tag{9.177}$$

9.3.5 Maximum Inductance for DCM

Figure 9.20 shows the inductor current waveform for the CCM/DCM boundary. The minimum peak value of the inductor current at the boundary occurs at $D = D_{Bmax}$ and is given by

$$I_{Omax} = I_{OB} = \frac{\Delta i_{Lmax}}{2} = \frac{V_O (0.5 - D_{Bmax})}{2 f_s L_{max}} = \frac{V_O}{R_{Lmin}}. \tag{9.178}$$

Hence, the maximum inductance required to keep the converter operation in DCM is

$$L_{max} = \frac{R_{Lmin}(0.5 - D_{Bmax})}{2 f_s} = \frac{V_O (0.5 - D_{Bmax})}{2 f_s I_{Omax}}. \tag{9.179}$$

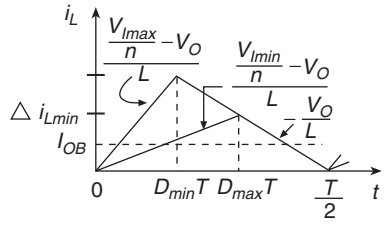


Figure 9.20 Inductor current waveform at the CCM/DCM boundary at V_{Imin} and V_{Imax} for the push-pull converter.

Table 9.1 Properties of PWM dc–dc converters for CCM

Converter	$M_{V\,DC}$	V_{SM}	I_{SM}	V_{DM}	I_{DM}	c_p
Buck	ηD	V_I	I_O	V_I	I_O	D
Boost	$\frac{\eta}{1-D}$	V_O	I_I	V_O	I_I	$1-D$
Buck-boost	$-\frac{\eta D}{1-D}$	V_I+V_O	I_I+I_O	V_I+V_O	I_I+I_O	$D(1-D)$
Flyback	$\frac{\eta D}{n(1-D)}$	V_I+nV_O	$I_I+\frac{I_O}{n}$	$\frac{V_I}{n}+V_O$	nI_I+I_O	$D(1-D)$
Forward	$\frac{\eta D}{n_1}$	$2V_I$	$\frac{I_O}{n_1}$	$\frac{V_I}{n_1}$	I_O	D
Half-bridge	$\frac{\eta D}{n}$	V_I	$\frac{I_O}{n}$	$\frac{V_I}{n}$	I_O	D
Full-bridge	$\frac{2\eta D}{n}$	V_I	$\frac{I_O}{n}$	$\frac{2V_I}{n}$	I_O	$2D$
Push-pull	$\frac{2\eta D}{n}$	$2V_I$	$\frac{I_O}{n}$	$\frac{2V_I}{n}$	I_O	D

Table 9.2 Properties of PWM dc–dc converters for DCM

Converter	$M_{V\,DC}$	V_{SM}	I_{SM}	V_{DM}	I_{DM}
Buck	$\frac{2}{1+\sqrt{\frac{8f_sL}{\eta D^2R_L}}}$	V_I	$\frac{V_{Imax}-V_O}{f_sL}$	V_I	$\frac{V_{Imax}-V_O}{f_sL}$
Boost	$\frac{1+\sqrt{1+\frac{2\eta D^2R_L}{2f_sL}}}{2}$	V_O	$\frac{V_{Imin}D_{max}}{f_sL}$	V_O	$\frac{V_{Imin}D_{max}}{f_sL}$
Buck-boost	$D\sqrt{\frac{\eta R_L}{2f_sL}}$	V_I+V_O	$\frac{V_{Imax}D_{min}}{f_sL}$	V_I+V_O	$\frac{V_{max}D_{min}}{f_sL}$
Flyback	$\frac{D}{n}\sqrt{\frac{\eta R_L}{2f_sL_{ms}}}$	V_I+nV_O	$\frac{V_{Imax}D_{min}}{f_sL_m}$	$\frac{V_I}{n}+V_O$	$\frac{nV_{max}D_{min}}{f_sL_m}$
Forward	$\frac{2}{n_1\left(1+\sqrt{1+\frac{8f_sL}{\eta D^2R_L}}\right)}$	$2V_I$	$\frac{\left(\frac{V_{Imax}}{n_1}-V_O\right)D_{min}}{n_1f_sL}$	$\frac{V_I}{n_1}$	$\frac{\left(\frac{V_{Imax}}{n_1}-V_O\right)D_{min}}{f_sL}$
Half-bridge	$\frac{1}{n\left(1+\sqrt{1+\frac{4f_sL}{\eta D^2R_L}}\right)}$	V_I	$\frac{\left(\frac{V_{Imax}}{2n}-V_O\right)D_{min}}{nf_sL}$	$\frac{V_I}{n}$	$\frac{\left(\frac{V_{Imax}}{2n}-V_O\right)D_{min}}{f_sL}$
Full-bridge	$\frac{2}{n\left(1+\sqrt{1+\frac{4f_sL}{\eta D^2R_L}}\right)}$	V_I	$\frac{\left(\frac{V_{Imax}}{n}-V_O\right)D_{min}}{nf_sL}$	$\frac{2V_I}{n}$	$\frac{\left(\frac{V_{Imax}}{2n}-V_O\right)D_{min}}{f_sL}$
Push-pull	$\frac{2}{n\left(1+\sqrt{1+\frac{4f_sL}{\eta D^2R_L}}\right)}$	$2V_I$	$\frac{\left(\frac{V_{Imax}}{n}-V_O\right)D_{min}}{nf_sL}$	$\frac{2V_I}{n}$	$\frac{\left(\frac{V_{Imax}}{n}-V_O\right)D_{min}}{f_sL}$

9.4 Comparison of PWM DC–DC Converters

The properties of PWM dc–dc converters for CCM and DCM are compared in Tables 9.1 and 9.2, respectively. The equations for the forward converter in the tables are given for $n_1 = n_3$. The equations for the half and full-bridge converters in the tables are given for the center-tapped rectifier.

9.5 Summary

- The PWM push-pull converter acts as either a step-up or a step-down converter.
- The dc voltage transfer function of the lossless push-pull converter is $M_{V\,DC} = 2D/n$.
- The push-pull converter is a buck-derived converter.
- It is easy to drive the transistors in the push-pull converter because the sources of the transistors are connected to ground.
- The maximum duty cycle must be slightly lower than 50 %.
- The voltage stresses of the switches are relatively high, equal to $2V_{Imax}$.
- The transformer does not have to store energy in the push-pull converter.
- The push-pull converter suffers from magnetic flux imbalance in the transformer core.
- The duty cycle D of the lossy converter is greater than that of the lossless converter at the same value of the dc voltage transfer function.
- The peak-to-peak inductor ripple current Δi_L is independent of the dc load current for CCM.
- The filter capacitor peak-to-peak ripple current is relatively low as compared to boost or buck-boost converters. It is equal to the peak-to-peak inductor current ripple Δi_L.
- The filter capacitance is lower than that in the buck converter with the same parameters because the output ripple frequency is twice that of the switching frequency.
- If the capacitance of the filter capacitor is sufficiently high, the output ripple voltage is determined only by the ESR of the filter capacitor and is independent of the capacitance of the filter capacitor.
- The minimum value of the inductor is determined by the CCM/DCM boundary, ripple voltage, or ac losses in the inductor and/or the filter capacitor.
- The input current is pulsating. However, an input LC filter can be added at the converter input to obtain a nonpulsating input current waveform.
- The corner frequency of the output filter $f_o = 1/(2\pi\sqrt{LC})$ is independent of the load resistance.

9.6 References

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9.7 Review Questions

9.1 What is the flux imbalance of the transformer in a push-pull converter?

9.2 Give the expression for the dc voltage transfer function of the lossless push-pull converter.

9.3 What is the maximum duty cycle in the push-pull converter?

9.4 How can core imbalance be prevented?

9.5 Is the transformer required to store energy?

9.6 What is the dc component of the current through the transformer primary?

9.7 Is the input current of the basic push-pull converter pulsating?

9.8 How can you obtain a nonpulsating input current in the push-pull converter?

9.9 Are the transistors driven with respect to ground in the push-pull converter?

9.10 How is the dc voltage transfer function $M_{V\,DC}$ related to the duty cycle D of the lossless push-pull converter for CCM?

9.11 Is the duty cycle D of the lossy push-pull converter less than or greater than that for the lossless converter at a given value of $M_{V\,DC}$ for CCM?

9.12 Is the corner frequency of the output filter dependent on the load resistance?

9.8 Problems

9.1 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$ and $V_O = 180\,\text{V}$. Find the transformer turns ratio n.

9.2 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$, $V_O = 180\,\text{V}$, and $n = 0.2$. Find the maximum and minimum duty cycle.

9.3 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$, $V_O = 180\,\text{V}$, and $n = 0.2$. Find the voltage stresses of the switches and the diodes.

9.4 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$, $V_O = 180\,\text{V}$, $n = 0.2$, $I_O = 0.2$ to 2 A, $D_{min} = 0.3509$, and $f_s = 40\,\text{kHz}$. Find the minimum inductance.

9.5 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$, $V_O = 180\,\text{V}$, $n = 0.2$, $I_O = 0.2$ to 2 A, $L = 2\,\text{mH}$, $D_{min} = 0.3509$, $f_s = 40\,\text{kHz}$, and $V_r/V_O \leq 0.5\,\%$. Find the minimum filter capacitance, the corner frequency of the output filter, and the ratio of the output ripple frequency to the corner frequency.

9.6 A push-pull PWM converter has $V_I = 48 \pm 6\,\text{V}$, $V_O = 180\,\text{V}$, $n = 0.2$, $I_O = 0.2$ to 2 A, $L = 2\,\text{mH}$, $f_s = 40\,\text{kHz}$, and $\Delta i_{Lmax} = 0.3357\,\text{A}$. Find the current stresses of the switches and the diodes.

9.7 Design a push-pull PWM converter to meet the following specifications: the dc input voltage V_I is the US single-phase rectified utility line voltage, $V_O = 5\,\text{V}$, $I_O = 4$ to 40 A, and $V_r/V_O \leq 1\,\%$.

9.8 Design a push-pull converter to meet the following specifications: $V_I = 12\,\text{V} \pm 30\,\%$, $V_O = 48\,\text{V}$, $I_O = 5$ to 50 A, and $V_r/V_O \leq 1\,\%$.

9.9 In a push-pull converter V_I is the US single-phase rectified utility line, $V_O = 12\,\text{V}$, $I_O = 0.2$ to 2 A, and $f_s = 200\,\text{kHz}$. Find the maximum inductance for DCM operation.

9.10 Design a push-pull PWM converter for aerospace applications with $V_I = 270\,\text{V} \pm 10\,\%$, $V_O = 28\,\text{V}$, $I_O = 5$ to 50 A, and $V_r/V_O \leq 1\,\%$. Assume $f_s = 100\,\text{kHz}$, $r_{DS} = 0.21\,\Omega$, $C_o = 100\,\text{pF}$, $V_F = 0.7\,\text{V}$, $R_F = 0.014\,\Omega$, $r_{T1} = 0.05\,\Omega$, $r_{T3} = 0.02\,\Omega$, $r_L = 0.01\,\Omega$, and $r_C = 0.025\,\Omega$.

10

Small-signal Models of PWM Converters for CCM and DCM

10.1 Introduction

Power stages of PWM converters are highly nonlinear systems because they contain at least one transistor and at least one diode, which are operated as switches. The converters normally require control circuits to regulate the dc output voltage against load and line variations. Typical control aspects of interest are frequency response, transient response, and stability. Linear control theory is well developed and may offer valuable tools for studying the dynamic performance of PWM converters. However, in order to apply this theory, nonlinear power stages of PWM converters should be *averaged* and *linearized* [1]–[5]. There are two averaging methods for PWM converters:

- the state-space averaging method [6]–[17];
- the circuit-averaging method [18]–[37].

The state-space averaging method is based on analytical averaging of state-space equations describing linear equivalent circuits for different states of a converter determined by the on–off status of the transistor(s) and the diode(s). The state-space equations are weighed according to the fraction of the switching cycle, during which the converter remains in a given state. However, the state-space averaging method requires considerable matrix algebra manipulation and is sometimes tedious, especially when the converter circuit contains a large number of elements or parasitic components. Moreover, it provides little insight into the converter behavior. On the other hand, in many power electronic circuits, the average values of voltages and currents are of interest, rather than their instantaneous values. The circuit-averaging method leads to linear circuit models. These models

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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are relatively simple, provide good intuitive insight into converter behavior, can be used for deriving various transfer functions and step responses, and are compatible with general-purpose electronic circuit simulators. In addition, control loops for PWM converters can be designed by applying well-known linear control techniques. Some nonlinear control methods have been proposed in [38]–[40].

In this chapter, the averaged large-signal, dc, and ac small-signal linear time-invariant circuit models of the discrete switching network of PWM converters are developed for CCM and DCM, using current- and voltage-dependent sources and the law of conservation of energy [25]–[27]. The dependent sources are used to model the ideal switching network, and the law of conservation of energy is used to model the transistor on-resistance, the diode forward resistance, and the diode offset voltage. The ideal switching network of single-ended transformerless PWM converters consists of two ideal switches. This network can be modeled for the dc components in steady state by two ideal dc dependent sources. The switched forward resistances of the switch and the diode are averaged, using the law of conservation of energy. The currents, voltages, and duty cycle are then perturbed in the average dc model. Hence, the dc dependent sources in the model are replaced by large-signal time-varying dependent sources. Consequently, the large-signal currents, voltages, and duty cycle contain both dc and ac components. Therefore, the large-signal sources can be replaced by dc dependent sources and ac small-signal dependent sources. If the magnitudes of the small-signal components are low enough, the model can be linearized by neglecting products of the ac components. This leads to a linear circuit model, containing both dc and ac dependent sources. Since the model is linear, it can be split into a small-signal low-frequency ac circuit model and a dc circuit model. If the switching network in a PWM converter is replaced by its small-signal model, a small-signal model of the entire power stage is obtained. This model may be used to derive and simulate small-signal transfer functions and step responses of the converter.

10.2 Assumptions

The models are derived under the following assumptions:

1. The transistor output capacitance and the diode capacitance are neglected; therefore, switching losses are neglected.
2. The transistor on-resistance r_{DS} is linear and the transistor off-resistance is infinite.
3. The diode in the on-state is modeled by a linear battery V_F and a linear forward resistance R_F. In the off-state, the diode is modeled by an infinite resistance.
4. Passive components are linear, time-invariant, and frequency-independent.
5. Storage-time modulation of bipolar transistors is neglected.

10.3 Averaged Model of Ideal Switching Network for CCM

A PWM converter consists of a nonlinear discrete part and a linear analog part. The nonlinear part consists of nonlinear semiconductor devices such as transistor(s) and diode(s) operated as switches, that is, as discrete components. The linear part consists of linear components, such as capacitors and inductors with their equivalent series resistances. The

nonlinear part may be replaced by an average circuit model, which emulates its average low-frequency behavior. In the average circuit model, the average low-frequency voltages across the model terminals and the average low-frequency currents into its terminals are identical to those of the original switching network. The waveforms of the average current and voltage do not contain high-frequency components. The high-frequency components can be regarded as carriers. The average model is nonlinear and may be linearized for small ac signals. The linear part of a converter does not require averaging and linearization.

The modeling strategy of PWM converters is similar to the transistor modeling and is based on the following principles:

(i) replacement of the switching network (or components) by an analog (continuous) circuit model;

(ii) leaving the analog part composed of linear components unchanged.

Figure 10.1 shows four basic single-ended transformerless two-switch PWM converters: buck, boost, buck-boost, and Ćuk converters. All these converters have a common

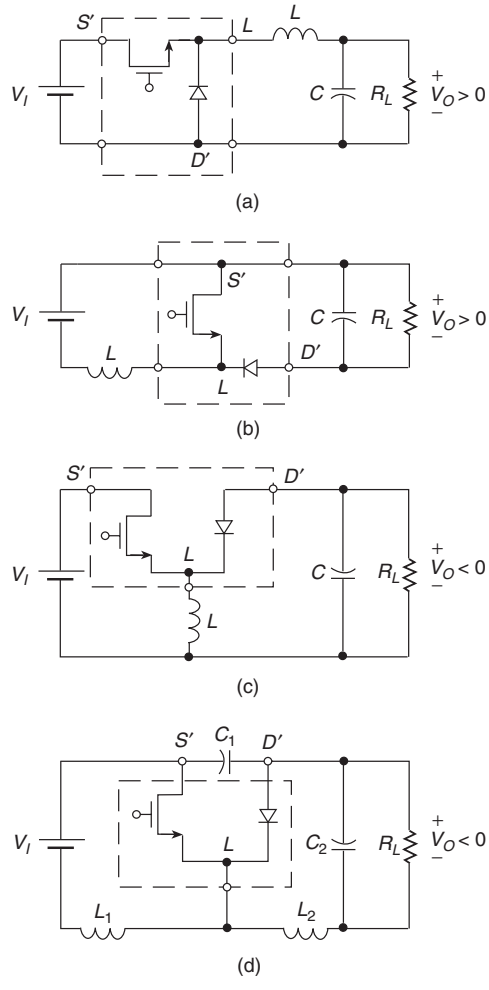


Figure 10.1 Single-ended transformerless two-switch PWM converters. (a) Buck converter. (b) Boost converter. (c) Buck-boost converter. (d) Ćuk converter.

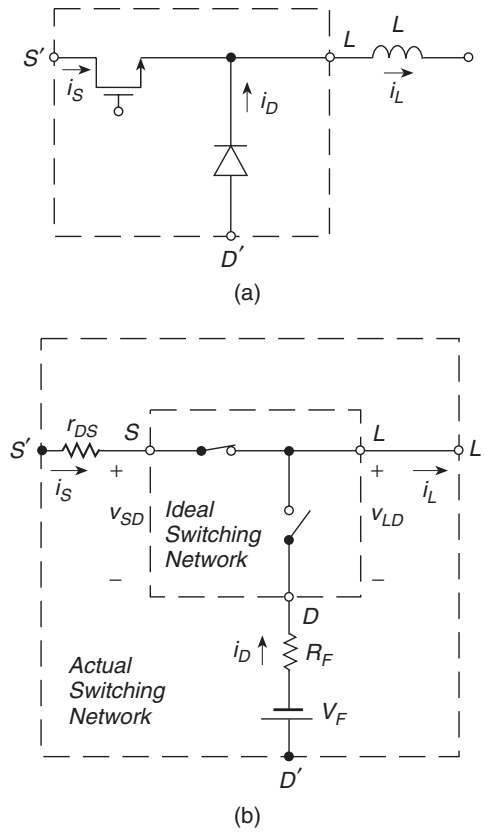


Figure 10.2 Switching network and equivalent circuit of single-ended transformerless two-switch PWM converters. (a) Switching network. (b) Equivalent circuit.

subcircuit that consists of two switching devices: a power MOSFET and a diode. This subcircuit is highly *nonlinear* and is referred to as a *switching network*. Figure 10.2(a) shows the switching network of single-ended transformerless two-switch PWM converters, and Figure 10.2(b) shows an equivalent circuit of the switching network. The *ideal part of the switching network* consists of two ideal switches. One ideal switch represents an ideal MOSFET whose on-resistance is zero, and the other ideal switch represents an ideal diode whose forward resistance and offset voltage are zero. The *actual switching network* consists of an ideal switching network and parasitic components. The MOSFET is represented by an ideal switch and a linear on-resistance r_{DS}, and the diode is represented by an ideal switch, a linear forward resistance R_F, and an offset voltage V_F.

Figure 10.3 shows the steady-state current and voltage waveforms in the ideal switching network for CCM. In this case, all ac external excitations, disturbances, and uncertainties are zero. There is no startup, shutdown, or sudden change in the input voltage and load resistance. Since the steady-state waveforms are periodic, all the current and voltage waveforms, their dc components, and the duty cycle D are the same in every cycle of the switching frequency $f_s = 1/T$. The waveforms of the inductor current i_L and the voltage across the combination of the switch and the diode v_{SD} are continuous, whereas the waveforms of the switch current i_S and the diode reverse voltage v_{LD} are pulsating. Averaging the high-frequency instantaneous values of converter waveforms is simply extracting the corresponding dc components over one cycle of the switching frequency f_s. Note that

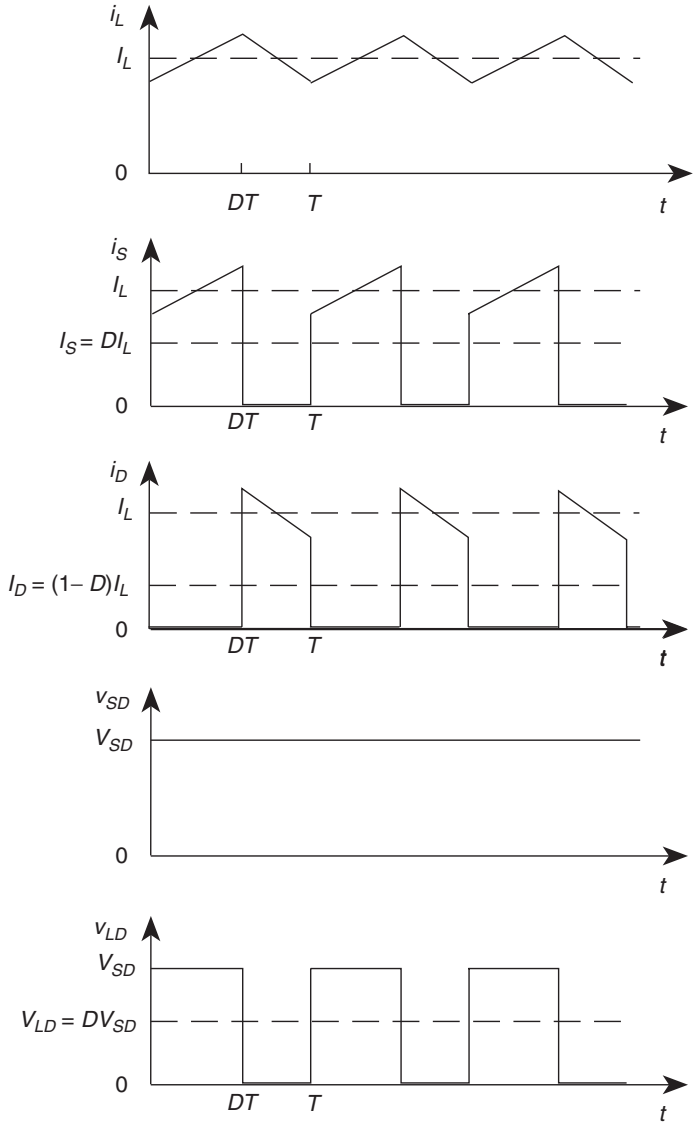


Figure 10.3 Steady-state waveforms in the ideal switching network for CCM.

averaging the steady-state waveforms (with zero ac excitations) over many cycles gives the same result.

Neglecting parasitic components in Figure 10.1 for the buck converter, $V_{SD} = V_I$, $V_{SL} = V_I - V_O$, and $V_{LD} = V_O$. For the boost converter, $V_{SD} = V_O$, $V_{SL} = V_I$, and $V_{LD} = V_O - V_I$. For the buck-boost converter, $V_{SD} = V_I - V_O = V_I + |V_O|$, $V_{SL} = V_I$, and $V_{LD} = V_O$. For the Ćuk converter, $V_{SD} = V_I - V_O = V_I + |V_O|$, $V_{SL} = V_I$, and $V_{LD} = V_O$.

According to Figure 10.3, the steady-state waveform of the switch current can be approximated by

$$i_S \approx \begin{cases} I_L, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T. \end{cases} \tag{10.1}$$

Hence, the dc component of the switch current is

$$I_S = \frac{1}{T}\int_0^T i_S\,dt = \frac{1}{T}\int_0^{DT} I_L\,dt = DI_L. \tag{10.2}$$

This expression describes an ideal dc *current-dependent current source* controlled by the inductor current I_L. An equivalent circuit representing this expression is an averaged model of an ideal switch and is shown in Figure 10.4(a).

Referring to Figure 10.3, the steady-state waveform of the voltage across ideal diode is given by

$$v_{LD} \approx \begin{cases} V_{SD}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{10.3}$$

yielding its dc component,

$$V_{LD} = \frac{1}{T}\int_0^T v_{LD}\,dt = \frac{1}{T}\int_0^{DT} V_{SD}\,dt = DV_{SD}. \tag{10.4}$$

This expression describes an ideal dc *voltage-dependent voltage source* controlled by the switch-diode voltage V_{SD}. Figure 10.4(b) shows an equivalent circuit representing an averaged model of an ideal diode.

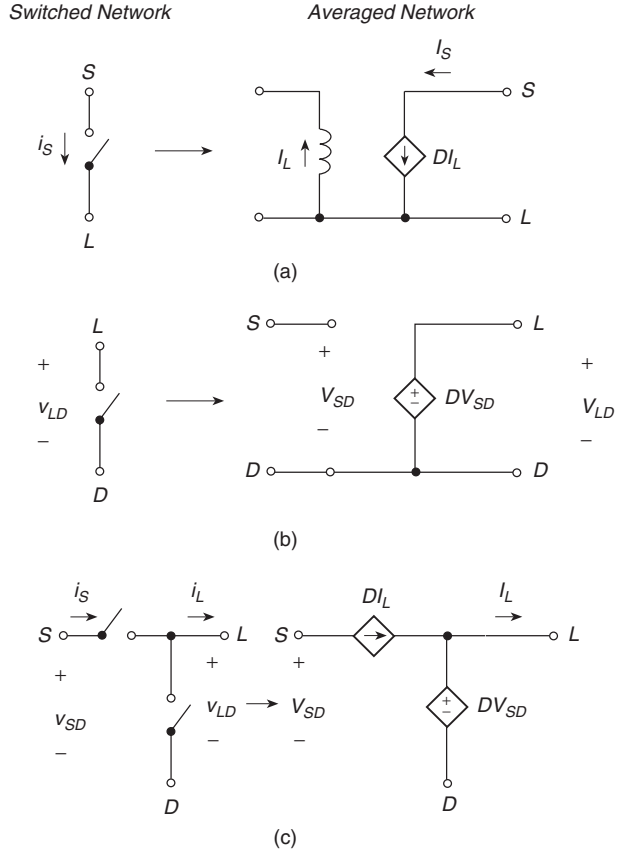


Figure 10.4 Averaged model of ideal switch, ideal diode, and ideal switching network for the dc components in steady state for CCM. (a) Averaged model of an ideal switch. (b) Averaged model of an ideal diode. (c) Averaged model of an ideal switching network of two-switch PWM converters.

Using the averaged models of an ideal switch and an ideal diode, an averaged model of an ideal switching network of two-switch PWM converters is obtained, as depicted in Figure 10.4(c). This model describes the performance of an ideal switching network for the dc components under steady-state conditions. It does not contain information about the inductor ripple current as well as the pulsating nature of the switch and diode current and voltage waveforms. The model of the switching network for the dc components under steady-state operating conditions is referred to as the 'dc model'.

10.4 Averaged Values of Switched Resistances

The transistor on-resistance r_{DS} and the diode forward resistance R_F are in series with the ideal switches in the switching network of Figure 10.2(b). These resistances should be averaged. Other resistances of a converter, such as the ESR of the inductor and the ESR of the filter capacitor, need not be averaged because they are not connected in series with the switches. The law of conservation of energy is used to determine the average values of the switched resistances.

The diode current can be approximated by

$$i_D \approx \begin{cases} 0, & \text{for } 0 < t \le DT, \\ I_L, & \text{for } DT < t \le T. \end{cases} \tag{10.5}$$

Thus, the dc component of the diode current is

$$I_D = \frac{1}{T}\int_{DT}^{T} I_L\, dt = I_L(1-D). \tag{10.6}$$

From (10.2) and (10.6),

$$I_L = \frac{I_S}{D} = \frac{I_D}{1-D}. \tag{10.7}$$

Using (10.1) and (10.2), the rms value of the switch current is obtained as

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\, dt} = \sqrt{\frac{1}{T}\int_0^{DT} I_L^2\, dt} = I_L\sqrt{D} = \frac{I_S}{\sqrt{D}} = \frac{I_D\sqrt{D}}{1-D}. \tag{10.8}$$

The power loss in the MOSFET on-resistance r_{DS} is

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{r_{DS}}{D} I_S^2. \tag{10.9}$$

On the other hand, the power loss in the averaged MOSFET on-resistance $r_{DSAV(S)}$ in the switch branch is

$$P_{rDSAV(S)} = r_{DSAV(S)}\, I_S^2. \tag{10.10}$$

Using the law of conservation of energy, the energy dissipated in the switched MOSFET on-resistance r_{DS} is the same as that in the averaged switch resistance $r_{DSAV(S)}$. Hence, the equivalent averaged resistance of r_{DS} in the switch branch is

$$r_{DSAV(S)} = \frac{r_{DS}}{D} \tag{10.11}$$

as shown in Figure 10.5(a).

Using (10.5), the rms value of the diode current is obtained as

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \sqrt{\frac{1}{T}\int_{DT}^T I_L^2\, dt} = I_L\sqrt{1-D} = \frac{I_S\sqrt{1-D}}{D} = \frac{I_D}{\sqrt{1-D}}, \tag{10.12}$$

resulting in the power loss in the diode forward resistance R_F,

$$P_{RF} = R_F I_{Drms}^2 = \frac{R_F}{1-D} I_D^2. \tag{10.13}$$

The power dissipated in the equivalent averaged diode forward resistance $R_{F\ AV(D)}$ in the diode branch is

$$P_{RF\ AV(D)} = R_{F\ AV(D)} I_D^2. \tag{10.14}$$

Consequently, the equivalent averaged resistance of R_F in the diode branch is obtained as

$$R_{F\ AV(D)} = \frac{R_F}{1-D} \tag{10.15}$$

as shown in Figure 10.5(b).

The power dissipated in the diode offset voltage source V_F is

$$P_{VF} = V_F I_D, \tag{10.16}$$

and the power dissipated in the equivalent averaged voltage $V_{F\ AV(D)}$ of the offset voltage source in the diode branch is

$$P_{VF\ AV(D)} = V_{F\ AV(D)} I_D. \tag{10.17}$$

Equating the right-hand sides of (10.16) and (10.17), one obtains the averaged diode offset voltage in the diode branch,

$$V_{F\ AV(D)} = V_F, \tag{10.18}$$

as shown in Figure 10.5(b).

Figure 10.6(a)–(b) depicts the actual switching network and its averaged dc model, respectively. If a bipolar junction transistor or an insulated gate bipolar transistor is used as a switch, the offset voltage source can be averaged in a similar manner. The inductance L is not a part of the model.

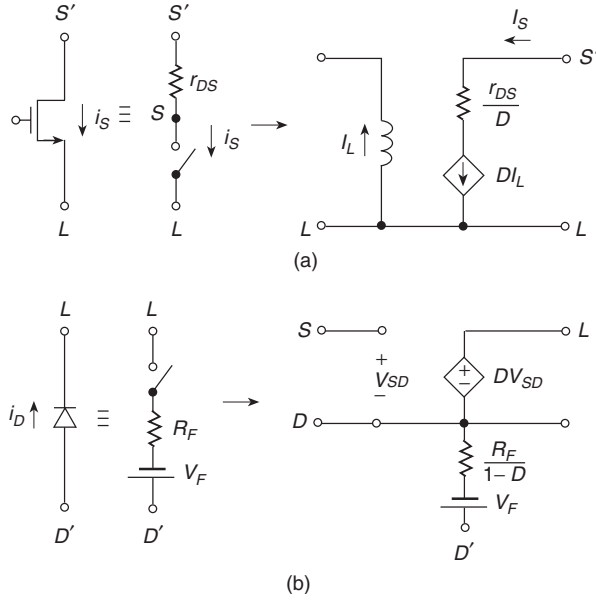


Figure 10.5 Averaged models of the actual MOSFET and the actual diode in steady state for CCM. (a) Averaged model of the actual MOSFET. (b) Averaged model of the actual diode.

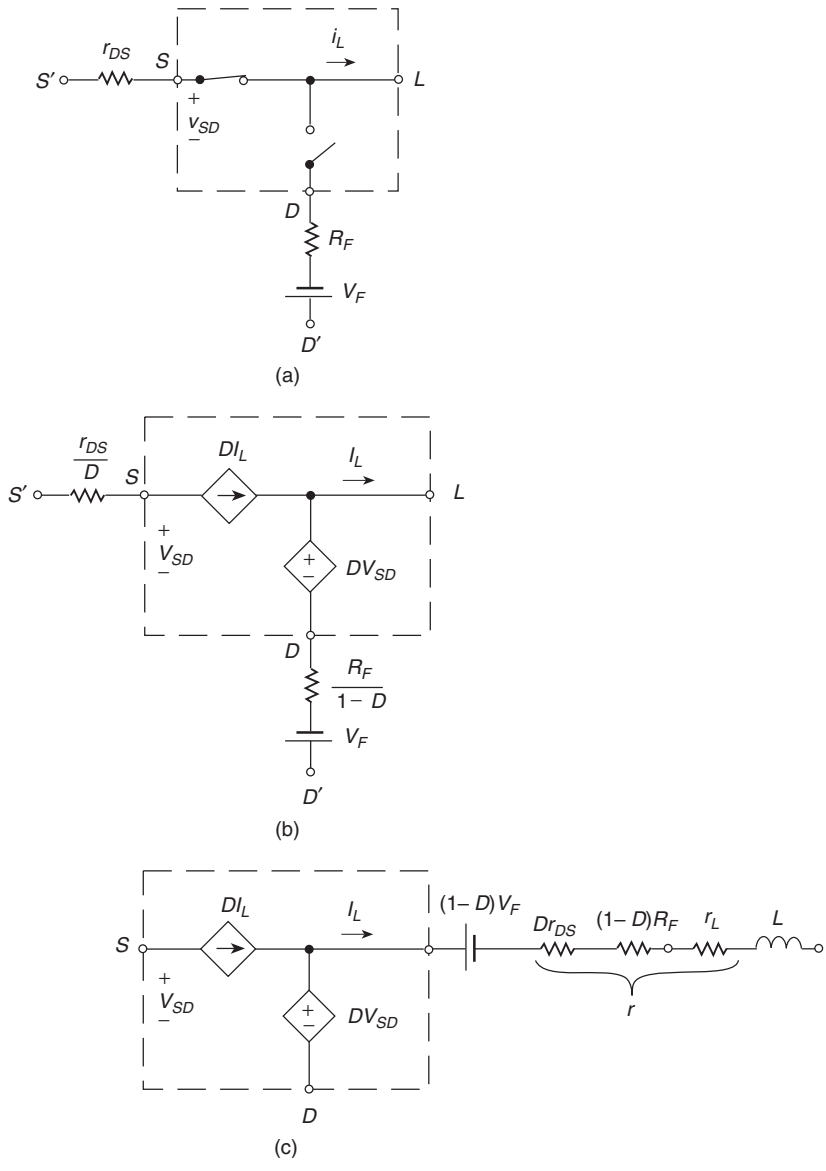


Figure 10.6 Modeling of the actual switching network under steady-state conditions for two-switch PWM converters operating in CCM. (a) Actual switching network. (b) Averaged dc model of the actual switching network. (c) Simplified averaged dc model of the actual switching network with the averaged resistances moved to the inductor branch.

10.5 Model Reduction

The averaged model of the actual switching network shown in Figure 10.6(b) contains two resistors. This does not cause any problem if the model is used for converter simulation purposes, such as PSPICE. However, a simpler form of the model is desirable, if it is used to derive various transfer functions and impedances. Reflection rules are used to derive a simplified model of the actual switching network.

Substitution of (10.7) into (10.9) yields

$$P_{rDS} = \frac{r_{DS}}{D} I_S^2 = D r_{DS} I_L^2 = \frac{D r_{DS}}{(1-D)^2} I_D^2. \tag{10.19}$$

Hence, the averaged MOSFET resistance in the MOSFET branch is

$$r_{DSAV(S)} = \frac{r_{DS}}{D}, \tag{10.20}$$

the averaged MOSFET resistance in the inductor branch is

$$r_{DSAV(L)} = D r_{DS}, \tag{10.21}$$

and the averaged MOSFET resistance in the diode branch is

$$r_{DSAV(D)} = \frac{D r_{DS}}{(1-D)^2}. \tag{10.22}$$

The ratios of these resistances are

$$\frac{r_{DSAV(L)}}{r_{DSAV(S)}} = D^2, \tag{10.23}$$

$$\frac{r_{DSAV(L)}}{r_{DSAV(D)}} = (1-D)^2, \tag{10.24}$$

and

$$\frac{r_{DSAV(S)}}{r_{DSAV(D)}} = \left(\frac{1-D}{D}\right)^2. \tag{10.25}$$

Thus, the relationship among the averaged MOSFET resistances in the different branches is

$$r_{DSAV(L)} = D^2 r_{DSAV(S)} = (1-D)^2 r_{DSAV(D)}. \tag{10.26}$$

Substituting (10.7) into (10.13), one obtains

$$P_{RF} = \frac{R_F I_D^2}{1-D} = (1-D) R_F I_L^2 = \frac{(1-D) R_F}{D^2} I_S^2, \tag{10.27}$$

which results in the averaged diode resistance in the diode branch,

$$R_{F\ AV(D)} = \frac{R_F}{1-D} \tag{10.28}$$

the averaged diode resistance in the inductor branch,

$$R_{F\ AV(L)} = (1-D) R_F, \tag{10.29}$$

and the averaged diode resistance in the MOSFET branch

$$R_{F\ AV(S)} = \frac{(1-D) R_F}{D^2}. \tag{10.30}$$

The ratios of these resistances are

$$\frac{R_{F\ AV(L)}}{R_{F\ AV(S)}} = D^2, \tag{10.31}$$

$$\frac{R_{F\ AV(L)}}{R_{F\ AV(D)}} = (1-D)^2, \tag{10.32}$$

and

$$\frac{R_{F\ AV(S)}}{R_{F\ AV(D)}} = \left(\frac{1-D}{D}\right)^2. \tag{10.33}$$

Hence, the relationship among the averaged diode forward resistances in the different branches is

$$R_{F\ AV(L)} = D^2 R_{F\ AV(S)} = (1-D)^2 R_{F\ AV(D)}. \tag{10.34}$$

Substitution of (10.7) into (10.16) gives

$$P_{VF} = V_F I_D = (1-D) V_F I_L = \frac{1-D}{D} V_F I_S. \tag{10.35}$$

This leads to the averaged offset diode voltage in the diode branch,

$$V_{F\ AV(D)} = V_F, \tag{10.36}$$

the averaged offset diode voltage in the inductor branch,

$$V_{F\ AV(L)} = (1-D) V_F, \tag{10.37}$$

and the averaged offset diode voltage in the MOSFET branch,

$$V_{F\ AV(S)} = \frac{(1-D) V_F}{D}. \tag{10.38}$$

The ratios of these averaged voltages are

$$\frac{V_{F\ AV(L)}}{V_{F\ AV(S)}} = D, \tag{10.39}$$

$$\frac{V_{F\ AV(L)}}{V_{F\ AV(D)}} = 1-D, \tag{10.40}$$

and

$$\frac{V_{F\ AV(S)}}{V_{F\ AV(D)}} = \frac{1-D}{D}. \tag{10.41}$$

Finally, the relationship among the averaged diode offset voltages in various branches is

$$V_{F\ AV(L)} = D V_{F\ AV(S)} = (1-D) V_{F\ AV(D)}. \tag{10.42}$$

Using (10.11), (10.15), and (10.19)–(10.41), general reflection rules are as follows:

$$r_l = D^2 r_s = (1-D)^2 r_d, \tag{10.43}$$

$$V_l = D V_s = (1-D) V_d, \tag{10.44}$$

where r_l, r_s, and r_d are the equivalent averaged resistances in the inductor branch, switch branch, and diode branch, respectively, and V_l, V_s, and V_d are the equivalent averaged voltage sources in the inductor branch, switch branch, and diode branch, respectively.

The equivalent resistance of the inductor branch is given by

$$r = r_{DSAV(L)} + R_{F\ AV(L)} + r_L = D r_{DS} + (1-D) R_F + r_L. \tag{10.45}$$

A simplified averaged dc model of the actual switching network is shown in Figure 10.6(c). The reflection rules can be applied to move the parasitic components from one branch to another, yielding other averaged models equivalent to that of Figure 10.6(b).

10.6 Large-signal Averaged Model for CCM

The actual switching networks is shown in Figure 10.7(a). The dc quantities such as the dc inductor current I_L, dc voltage V_{SD}, and constant duty cycle D in the averaged models

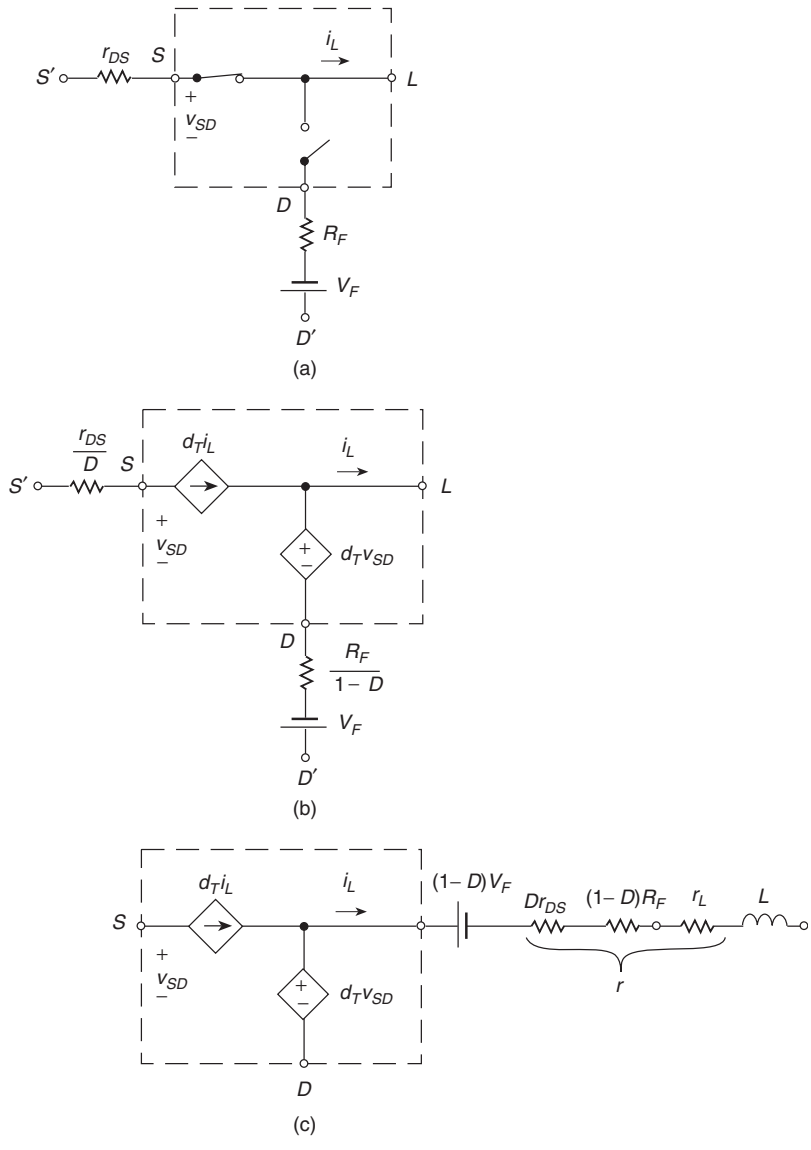


Figure 10.7 Large-signal averaged models of the actual switching network for two-switch PWM converters for CCM. (a) Actual switching network. (b) Large-signal averaged model of the actual switching network. (c) Simplified large-signal averaged model of the actual switching network with the averaged resistances moved to the inductor branch.

shown in Figure 10.6(b)–(c) can be replaced by slowly varying, time-dependent, large-signal quantities such as the current i_L, voltage v_{SD}, and duty cycle d_T. Relationships among the low-frequency large-signal variables can be approximated using the dc relationships (10.2) and (10.4) for the dc variables

$$v_{LD} = d_T v_{SD} \tag{10.46}$$

and

$$i_S = d_T i_L. \tag{10.47}$$

A large-signal, low-frequency, averaged model representing these equations is shown in Figure 10.7(b)–(c).

Example 10.1

Draw a large-signal low-frequency averaged model of a buck PWM converter with parasitic components. Simplify this model using a current source splitting theorem.

Solution. Figure 10.8(a) shows a low-frequency, large-signal, averaged model of a buck converter. This model can be obtained by replacing the actual switching network with the large-signal model shown in Figure 10.7(c) in the buck converter. Note that $v_{SD} = v_I$ for the buck converter. Using the current splitting theorem, the dependent current source can be split into two current sources, as shown in Figure 10.8(b). In general, the parallel combination of a current source and a voltage source is equivalent to the voltage source. Therefore, the model may be simplified by neglecting the dependent current source in parallel with the dependent voltage source, as depicted in Figure 10.8(c).

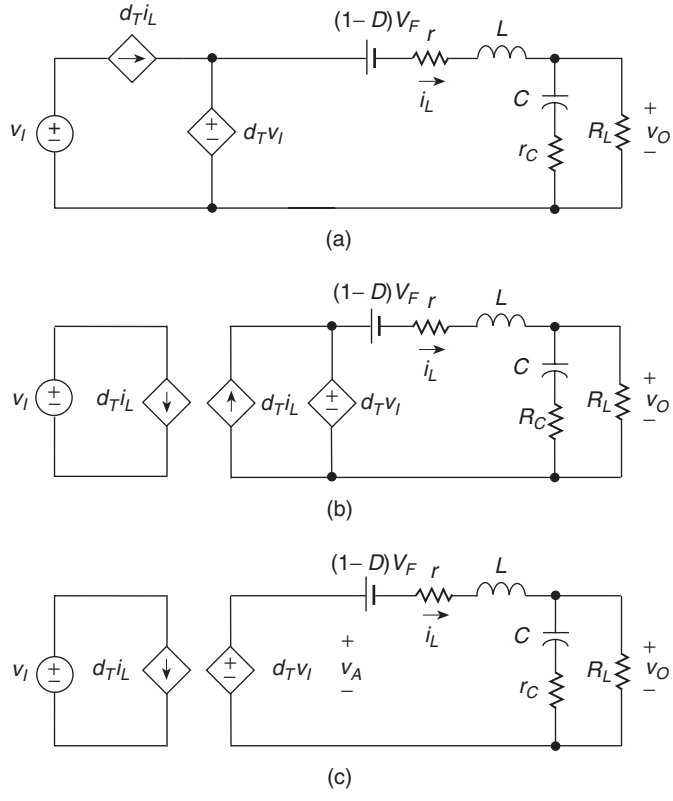


Figure 10.8 Low-frequency large-signal model of a buck PWM converter with parasitic components for CCM. (a) Large-signal model with the dependent sources in the original branches. (b) Large-signal model with the dependent current source split into two sources. (c) Simplified large-signal model.

Example 10.2

In a buck PWM converter, the duty cycle $d_T = D$ is held at a fixed value and the initial boundary conditions of the inductor L and the filter capacitor C are zero. The inductance L is high enough to operate the converter in CCM for steady state. At time $t = 0$, the dc input voltage source V_I is turned on. Find the waveform of the output voltage v_O without the switching-frequency component and its harmonics. Neglect parasitic elements.

Solution. The large-signal, low-frequency, averaged model shown in Figure 10.8(c) with no parasitic elements may be used to find the output voltage. This voltage is a response to a step change of the input voltage, without the switching-frequency component. This model is linear when $d_T = D$. The step change of the input voltage in the time domain is

$$v_I(t) = V_I u(t). \tag{10.48}$$

Therefore, the average voltage at the input of the LCR_L circuit is also a step change given by

$$v_A(t) = Dv_I(t) = DV_I u(t), \tag{10.49}$$

which in the s-domain is

$$v_A(s) = \frac{DV_I}{s}. \tag{10.50}$$

The voltage transfer function of the LCR_L circuit is

$$A_v(s) = \frac{v_O(s)}{v_A(s)} = \frac{\dfrac{R_L \dfrac{1}{sC}}{R_L + \dfrac{1}{sC}}}{\dfrac{R_L \dfrac{1}{sC}}{R_L + \dfrac{1}{sC}} + sL} = \frac{1}{LC} \frac{1}{s^2 + s\dfrac{1}{CR_L} + \dfrac{1}{LC}}. \tag{10.51}$$

The undamped resonant frequency (or the natural frequency) is

$$\omega_0 = \frac{1}{\sqrt{LC}}, \tag{10.52}$$

and the damping factor is

$$\xi = \frac{1}{2R_L}\sqrt{\frac{L}{C}}. \tag{10.53}$$

Hence,

$$A_v(s) = \frac{\omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2}. \tag{10.54}$$

The output voltage in the s-domain is

$$v_O(s) = A_v(s)v_A(s) = \frac{DV_I\omega_0^2}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)} = DV_I\left[\frac{1}{s} - \frac{s + 2\xi\omega_0}{s^2 + 2\xi\omega_0 s + \omega_0^2}\right], \tag{10.55}$$

resulting in the output voltage in the time domain,

$$v_O(t) = \mathcal{L}^{-1}\{v_O(s)\} = DV_I\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_0 t}\sin(\omega_0\sqrt{1-\xi^2}t + \phi)\right], \tag{10.56}$$

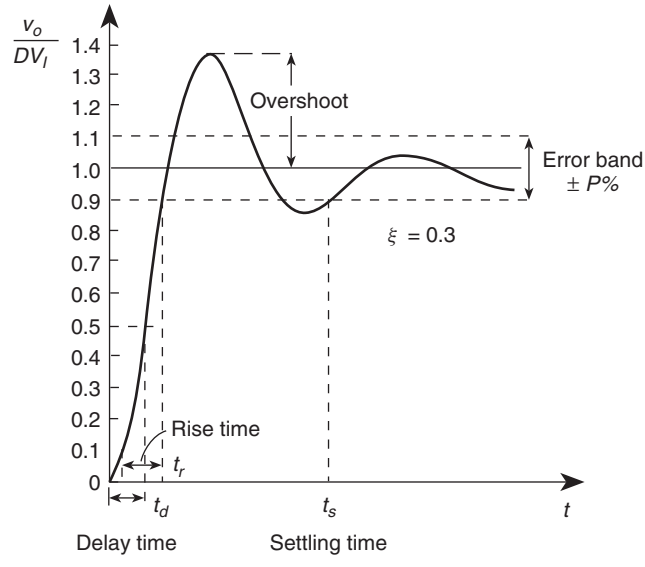


Figure 10.9 Normalized output voltage $v_O/(DV_I)$ as a response to a step change in the dc input voltage at $\xi = 0.3$, neglecting the switching-frequency component.

where

$$\phi = \arccos\xi. \tag{10.57}$$

Figure 10.9 shows the normalized output voltage waveform $v_O/(DV_I)$ without the switching-frequency component. The output voltage is the response of the second-order low-pass filter to a step change from zero to DV_I.

10.7 DC and Small–signal Circuit Linear Models of Switching Network for CCM

Consider the operation of a PWM converter under external low-frequency excitation (also called low-frequency perturbation) superimposed on the dc component. Each of the waveforms in a PWM converter under low-frequency excitation contains three components:

- a dc component;
- a low-frequency component of the frequency $f = \omega/(2\pi)$ and its harmonics;
- a high-frequency component of the switching frequency f_s and its harmonics.

Only the dc components and the low-frequency components are of interest when studying control aspects of PWM converters. This is because the control signals of the closed-loop PWM converters normally consist of dc and low-frequency components. Consequently, the low-frequency components are used to characterize the dynamics of PWM systems. The purpose of the averaged low-frequency dynamic models is to emulate the average

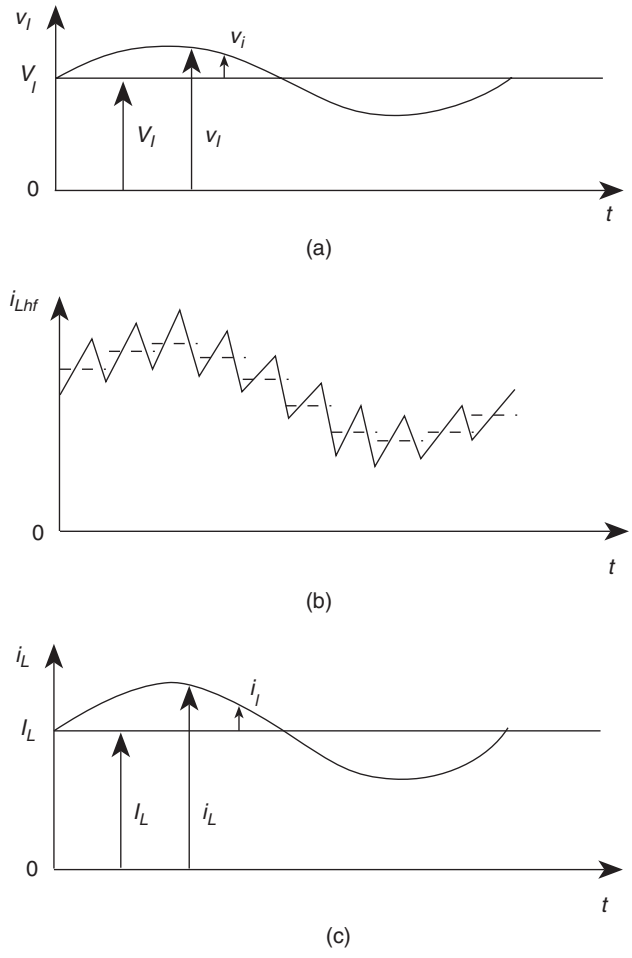


Figure 10.10 Waveforms of the input voltage and the inductor current under sinusoidal low-frequency small-signal perturbations for CCM. (a) Waveform of the input voltage. (b) Waveform of the high-frequency inductor current. (c) Waveform of the averaged low-frequency inductor current.

behavior (in particular, dynamics) of the open- and closed-loop PWM converters in the low-frequency range.

In the simplest case, the low-frequency perturbation signals can be sinusoidal. They are especially useful for test purposes to study the frequency response of a PWM system. As an illustrative example, Figure 10.10 shows the waveforms of the input voltage and the inductor current under a sinusoidal low-frequency perturbation. Figure 10.10(a) shows the ac low-frequency sinusoidal component of the input voltage

$$v_i = V_{im} \sin \omega t \tag{10.58}$$

superimposed on the dc component of the input voltage V_I, resulting in the large-signal input voltage

$$v_I = V_I + v_i = V_I + V_{im} \sin \omega t. \tag{10.59}$$

The high-frequency waveform of the inductor current $i_{L_{hf}}$ is depicted in Figure 10.10(b). Figure 10.10(c) shows the averaged low-frequency sinusoidal component of the inductor current

$$i_l = I_{lm} \sin \omega t \tag{10.60}$$

superimposed on the dc component I_L, and the averaged low-frequency large-signal inductor current

$$i_L = I_L + i_l = I_L + I_{lm} \sin \omega t. \tag{10.61}$$

The procedure for extracting the averaged dc and low-frequency components of the inductor current consists of two steps. First, the average values of the instantaneous inductor current for every cycle of the switching frequency $f_s = 1/T$ (also called local average values) are found to be

$$i_{L(av)}(kT) = \frac{1}{T} \int_{kT}^{(k+1)T} i_{L_{hf}} dt, \tag{10.62}$$

as shown in Figure 10.10(b) by the dashed lines. Second, the averaged low-frequency component of Figure 10.10(c) is obtained by connecting the average values in Figure 10.10(b), for example, in the middle or at the beginning of every cycle of the switching frequency $f_s = 1/T$.

In reality, the low-frequency perturbation signal may be more complex. An example of such a signal is a ripple voltage of a frequency of 100 or 120 Hz on the rectified voltage obtained from a single-phase front-end bridge rectifier.

According to Shannon's sampling theorem, the frequency f of the perturbation signal must be less than or equal to one-half of the switching frequency f_s, called the Nyquist frequency. As a result, the low-frequency dynamic models of PWM converters are valid only in the frequency range $0 \leq f \leq f_s/2$.

If the dc independent external variables, such as the dc input voltage V_I and/or the duty cycle D, are perturbed in a converter circuit at a low frequency $f < f_s/2$, all other variables will vary around their corresponding dc levels at a low frequency f. As a result, the averaged voltages, currents, and duty cycle can be expressed as the sums of dc components and ac low-frequency components as follows:

$$v_{SD} = V_{SD} + v_{sd}, \tag{10.63}$$

$$i_S = I_S + i_s, \tag{10.64}$$

$$v_{LD} = V_{LD} + v_{ld}, \tag{10.65}$$

$$i_L = I_L + i_l, \tag{10.66}$$

$$v_O = V_O + v_o, \tag{10.67}$$

$$i_D = I_D + i_d, \tag{10.68}$$

and

$$d_T = D + d. \tag{10.69}$$

The large-signal model shown in Figure 10.11(a) is nonlinear. *Linearization* of the large-signal averaged model at a given operating point can be performed by expanding the large-signal nonlinear equations into a Taylor's series about the operating point, and neglecting the higher-order terms. A linear small-signal model can be obtained by assuming

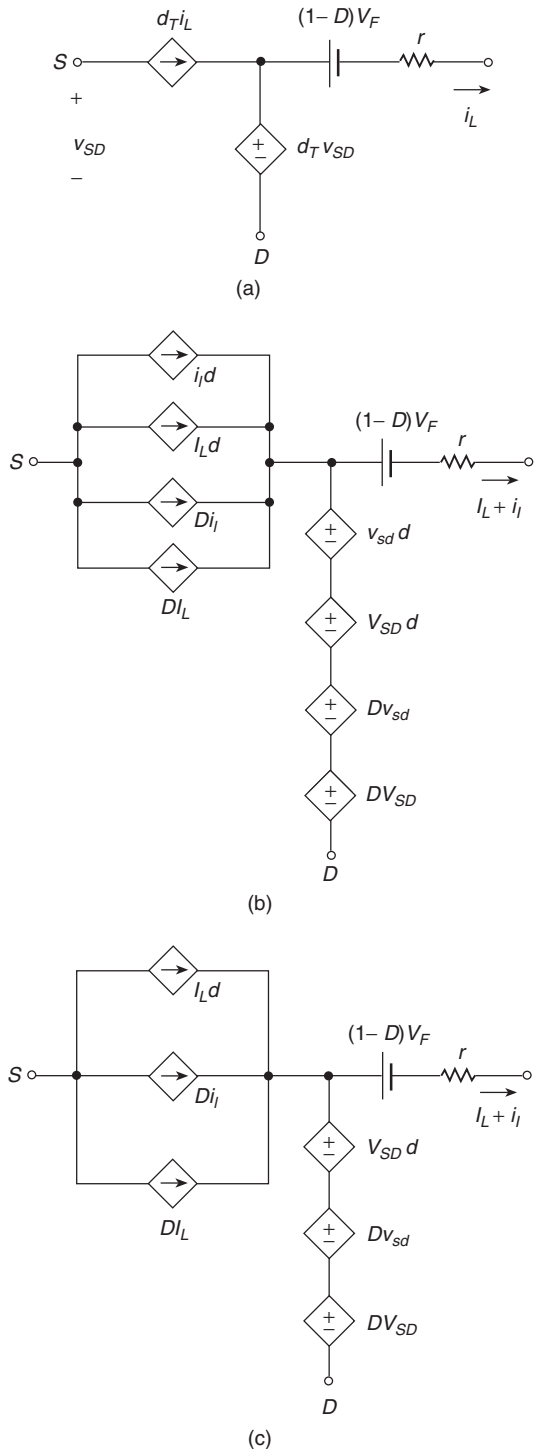


Figure 10.11 Averaged low-frequency large-signal and bilinear models of the actual switching network for two-switch PWM converters for CCM. (a) Averaged low-frequency large-signal nonlinear model. (b) Averaged low-frequency bilinear model. (c) Averaged dc and low-frequency small-signal model.

small-signal perturbations, which allows us to take into account only the first-order terms. The assumption of the small-signal perturbation implies that the magnitudes of the ac low-frequency components are much lower than those of the corresponding dc components.

Substituting (10.64), (10.66), and (10.69) into (10.47), one obtains a nonlinear equation,

$$I_S + i_s = (D + d)(I_L + i_l) = DI_L + Di_l + I_L d + i_l d. \tag{10.70}$$

This operation is equivalent to expanding (10.47) into a two-dimensional Taylor series around the dc operating point $Q(D, I_L)$ and neglecting higher-order terms. Similarly, substitution of (10.63), (10.65), and (10.69) into (10.46) yields a nonlinear equation,

$$V_{LD} + v_{ld} = (D + d)(V_{SD} + v_{sd}) = DV_{SD} + Dv_{sd} + V_{SD}d + v_{sd}d. \tag{10.71}$$

Equations (10.70) and (10.71) can be represented by a circuit model of the actual switching network, shown in Figure 10.11(b). This model is nonlinear, and is known as a bilinear model. To linearize this model, let us assume that

$$i_l d \ll Di_l, \tag{10.72}$$

$$i_l d \ll I_L d, \tag{10.73}$$

$$v_{sd}d \ll Dv_{sd}, \tag{10.74}$$

and

$$v_{sd}d \ll V_{SD}d. \tag{10.75}$$

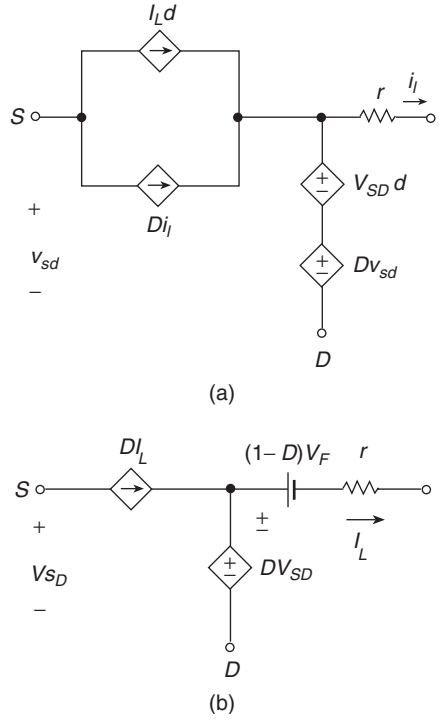


Figure 10.12 Small-signal low-frequency and dc linear circuit models of the actual switching network for two-switch PWM converters for CCM. (a) Linear low-frequency small-signal circuit model of the actual switching network. (b) DC model of the actual switching network.

Simplifying these inequalities, one obtains the *small-signality conditions*

$$d \ll D, \tag{10.76}$$

$$i_l \ll I_L, \tag{10.77}$$

and

$$v_{sd} \ll V_{SD}. \tag{10.78}$$

Neglecting the products of the small-signal components $i_l d$ and $v_{sd} d$ in (10.70) and (10.71), one obtains a set of linear equations

$$I_S + i_s = DI_L + Di_l + I_L d \tag{10.79}$$

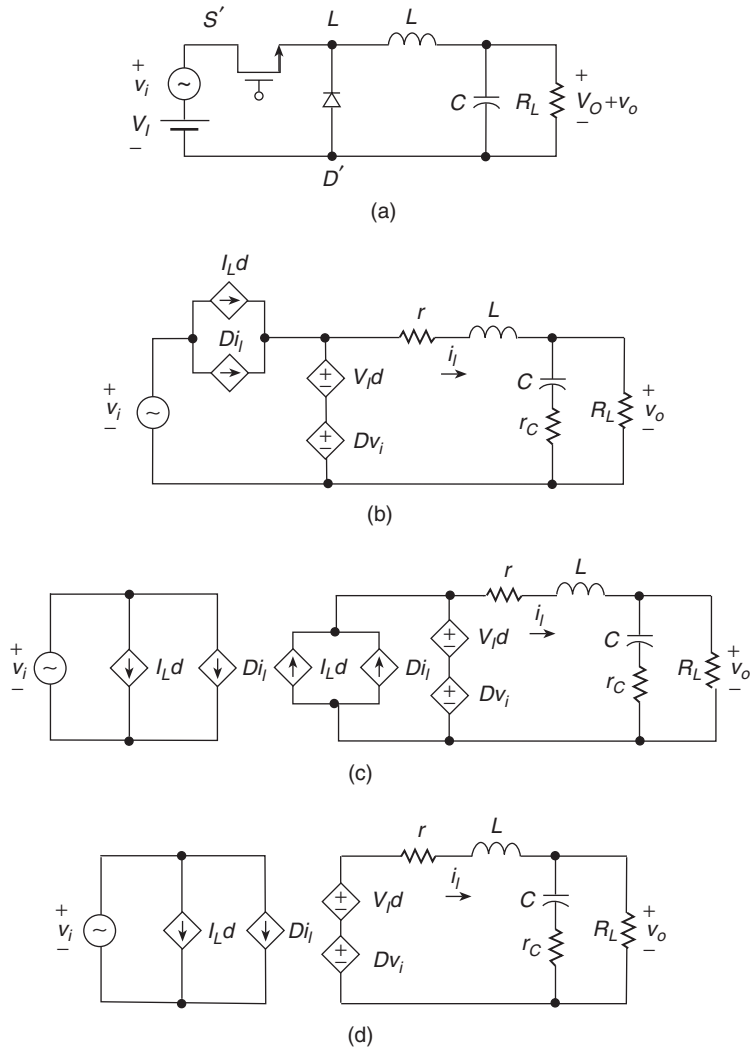


Figure 10.13 Small-signal low-frequency model of the buck PWM converter with parasitic components for CCM. (a) Circuit of the physical buck PWM converter. (b) Small-signal model of the buck converter. (c) Small-signal model of the buck converter with two sets of the dependent current sources. (d) Simplified small-signal model of the buck converter.

and

$$V_{LD} + v_{ld} = DV_{SD} + Dv_{sd} + V_{SD}d. \tag{10.80}$$

This set of linear equations can be represented by a linear circuit model of the actual switching network for both dc and small-signal ac components depicted in Figure 10.11(c). Since this model is linear, the principle of superposition can be used to split the model of Figure 10.11(c) into a small-signal circuit model, as shown in Figure 10.12(a), and a dc circuit model of the actual switching network, as shown in Figure 10.12(b).

A circuit of the buck PWM converter is depicted in Figure 10.13(a). Figure 10.13(b) shows a small-signal low-frequency model of the buck converter with parasitic components. This model can be obtained by replacing the actual switching network in the buck converter with the small-signal low-frequency model shown in Figure 10.12(a). For the buck converter, $V_{SD} = V_I$ and $v_{sd} = v_i$. The dependent current sources can be split into two sets of current sources: one set in parallel with the input voltage source v_i and the other set in parallel with the series combination of the dependent voltage sources, as shown in Figure 10.13(c). The parallel combination of the current sources and the voltage sources is equivalent to the voltage sources; therefore, the model may be simplified by neglecting the parallel dependent current sources, as shown in Figure 10.13(d). Figures 10.14 and 10.15 show small-signal models of the boost and buck-boost converters, respectively. For the boost converter, $V_{SD} = V_O$ and $v_{sd} = v_o$. For the buck-boost converter, $V_{SD} = V_I - V_O$ and $v_{sd} = v_i - v_o$, where $V_O < 0$.

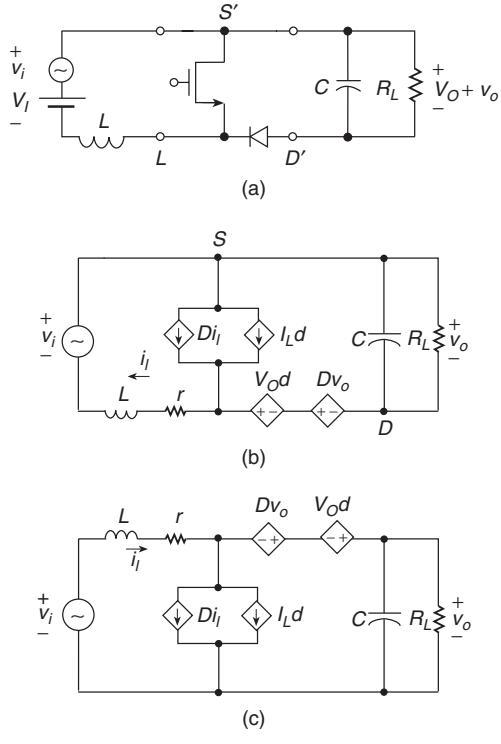


Figure 10.14 Small-signal low-frequency model of a boost PWM converter with parasitic components for CCM. (a) Circuit of the physical boost PWM converter. (b) Small-signal model of the boost converter. (c) Simplified small-signal model of the boost converter.

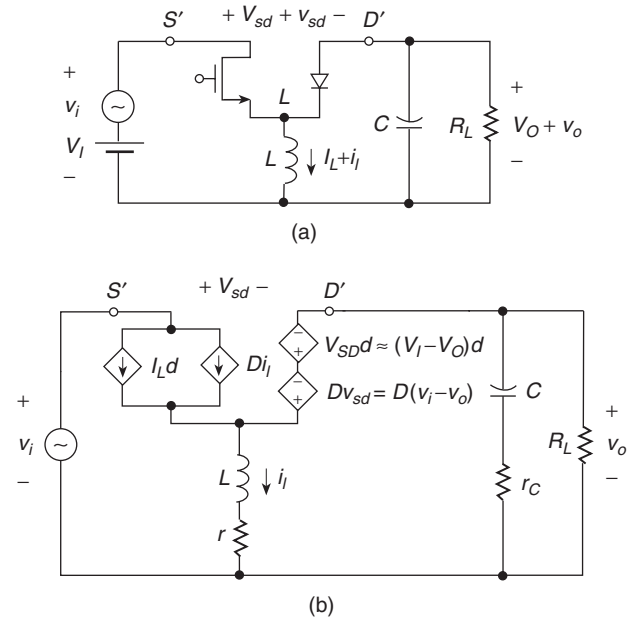


Figure 10.15 Small-signal low-frequency model of the buck-boost PWM converter with parasitic components for CCM. (a) Circuit of the physical buck-boost PWM converter. (b) Small-signal model of the buck-boost converter.

10.8 Family of PWM Converter Models for CCM

The relationships among the averaged large-signal variables for the single-ended transformerless PWM converters operated in CCM are given by

$$i_L = \frac{i_S}{d_T} = \frac{i_D}{1 - d_T} \tag{10.81}$$

and

$$v_{SD} = \frac{v_{LD}}{d_T} = \frac{v_{SL}}{1 - d_T}. \tag{10.82}$$

These relationships lead to six topologies of the averaged large-signal models of the ideal switching network for CCM, shown in Figure 10.16. Each topology contains one ideal current-dependent current source and one ideal voltage-dependent voltage source. Each current-dependent current source can be controlled by the current through one of the remaining branches. Similarly, each voltage-dependent voltage-source can be controlled by one of the remaining inter-terminal voltages. Therefore, there are 24 pairs of descriptive combinations for the current- and voltage-dependent sources. These combinations are given in Table 10.1, and there are 24 averaged large-signal models of the ideal switching network. Only six of them are shown in Figure 10.16. The averaged resistances and the averaged offset voltage source can be added to each model to obtain an averaged large-signal model of the actual switching network. Any of these models can be linearized to obtain an averaged small-signal model and a dc model in a similar manner to that shown in this chapter for the model of Figure 10.16(a).

The same technique may also be used to derive models for transformer PWM converters (e.g., flyback or forward converters), multiple-switch converters (e.g., half-bridge,

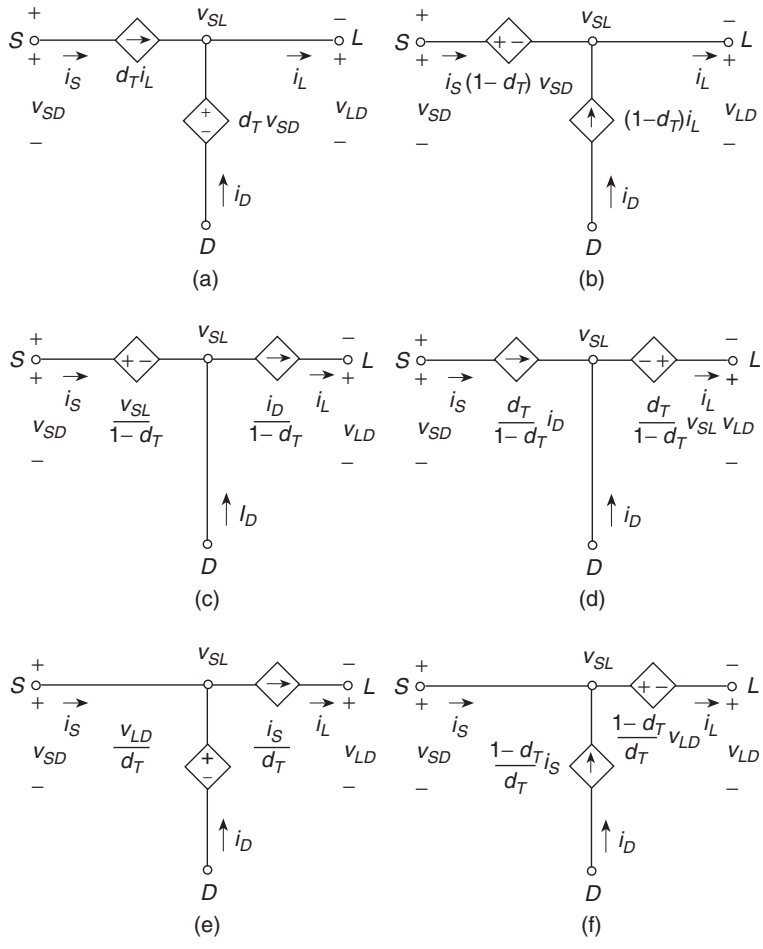


Figure 10.16 A family of averaged large-signal models of the ideal switching network for basic two-switch PWM converters in CCM.

full-bridge, or push-pull converters), and for converters operating in the discontinuous conduction mode.

10.9 PWM Small-signal Switch Model for CCM

Figure 10.17 shows a PWM small-signal switch model for the switching network of all two-switch PWM converters proposed in [21]. The symbols a, p, and c denote the 'active', 'passive', and 'common' terminals, respectively. In this model, D is the steady-state dc component of the on-duty cycle, V_{ap} is the steady-state dc component of the voltage across the series combination of the active switch (a transistor) and the passive switch (a diode), $V_{ap} = V_{SD}$, and I_C is the steady-state dc component of the current flowing out of the common node, that is, the steady-state dc component of the inductor current I_L. For a given operating point, V_{ap}, D, and I_C are constant quantities. The quantities d and i_c are the small-signal duty cycle and the small-signal inductor current, respectively. As the frequency approaches zero, the transformer becomes a dc transformer, which is not a circuit-theory

Table 10.1 Descriptions of dependent sources in large-signal models of Figure 10.16 for CCM

Model no.	Figure	Current source	Voltage source
1	10.16(a)	$d_T i_L$	$d_T v_{SD}$
2		$d_T i_L$	$\frac{d_T}{1-d_T} v_{SL}$
3		$\frac{d_T}{1-d_T} i_D$	$d_T v_{SD}$
4		$\frac{d_T}{1-d_T} i_D$	$\frac{d_T}{1-d_T} v_{SL}$
5	10.16(b)	$(1-d_T) i_L$	$(1-d_T) v_{SD}$
6		$(1-d_T) i_L$	$\frac{1-d_T}{d_T} v_{LD}$
7		$\frac{1-d_T}{d_T} i_S$	$(1-d_T) v_{SD}$
8		$\frac{1-d_T}{d_T} i_S$	$\frac{d_T}{1-d_T} v_{LD}$
9	10.16(c)	$\frac{i_D}{1-d_T}$	$\frac{v_{SL}}{1-d_T}$
10		$\frac{i_D}{1-d_T}$	$\frac{v_{LD}}{d_T}$
11		$\frac{i_S}{d_T}$	$\frac{v_{SL}}{1-d_T}$
12		$\frac{i_S}{d_T}$	$\frac{v_{LD}}{d_T}$
13	10.16(d)	$d_T i_L$	$d_T v_{SD}$
14		$d_T i_L$	$\frac{d_T}{1-d_T} v_{SL}$
15		$\frac{d_T}{1-d_T} i_D$	$d_T v_{SD}$
16		$\frac{d_T}{1-d_T} i_D$	$\frac{d_T}{1-d_T} v_{SL}$
17	10.16(e)	$\frac{i_D}{1-d_T}$	$\frac{v_{SL}}{1-d_T}$
18		$\frac{i_D}{1-d_T}$	$\frac{v_{LD}}{d_T}$
19		$\frac{i_S}{d_T}$	$\frac{v_{SL}}{1-d_T}$
20		$\frac{i_S}{d_T}$	$\frac{v_{LD}}{d_T}$
21	10.16(f)	$(1-d_T) i_L$	$(1-d_T) v_{SD}$
22		$(1-d_T) i_L$	$\frac{1-d_T}{d_T} v_{LD}$
23		$\frac{1-d_T}{d_T} i_S$	$(1-d_T) v_{SD}$
24		$\frac{1-d_T}{d_T} i_S$	$\frac{1-d_T}{d_T} v_{LD}$

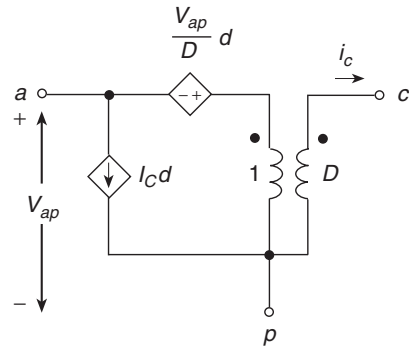


Figure 10.17 A PWM small-signal switch model of the nonlinear switching network for basic two-switch PWM converters operating in CCM.

component. Substitution of the nonlinear switching network (a transistor and a diode) by its PWM small-signal model of Figure 10.17 gives the small-signal model of the entire power stage of a two-switch PWM converter. The small-signal model shown in Figure 10.17 and proposed in [21] has a different topology than that shown in Figure 10.12(a) and developed in [25], [26], even if the transformer in Figure 10.17 is replaced by dependent sources.

10.10 Modeling of the Ideal Switching Network for DCM

10.10.1 Relationships among DC Components for DCM

Circuit models of PWM converters operated in DCM [22], [27] will be derived below. Let us consider the ideal switching network shown in Figure 10.2(b). Figure 10.18 shows the steady-state voltage waveforms in PWM converters for DCM. From Figure 10.1, the dc components of the terminal voltages (i.e., the average voltages) of the switching network can be expressed in terms of the converter dc input and output voltages V_I and V_O as follows: $V_{SD} = V_I$, $V_{SL} = V_I - V_O$, and $V_{LD} = V_O$ for the buck converter; $V_{SD} = V_O$, $V_{SL} = V_I$, $V_{LD} = V_O - V_I$ for the boost converter; and $V_{SD} = V_I - V_O = V_I + |V_O|$, $V_{SL} = V_I$, $V_{LD} = -V_O$ for the buck-boost and Ćuk converters.

Referring to Figures 10.1 and 10.2, and neglecting the parasitic components r_{DS}, R_F, and V_F, note that the voltages $v_{SL'}$ and $v_{L'D}$ contain only dc components $V_{SL'}$ and $V_{L'D}$, respectively, that is,

$$v_{SL'} = V_{SL'} \tag{10.83}$$

and

$$v_{L'D} = V_{L'D}. \tag{10.84}$$

Since the average inductor voltage $V_{L(AV)} = 0$, the dc component of the voltage across the series combination of the switch and the inductor $V_{SL'}$ is equal to the dc component of the switch voltage V_{SL},

$$V_{SL'} = V_{SL} + V_{L(AV)} = V_{SL}. \tag{10.85}$$

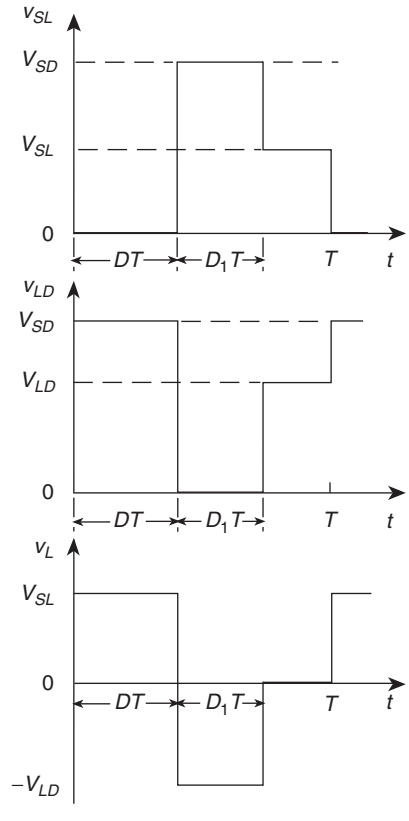


Figure 10.18 Voltage waveforms in PWM converters for DCM.

The dc component of the voltage across the series combination of the diode and the inductor $V_{DL'}$ is equal to the dc component of the diode voltage V_{LD},

$$V_{L'D} = V_{LD} - V_{L(AV)} = V_{LD}. \tag{10.86}$$

By Kirchhoff's voltage law, the inductor voltage can be expressed as

$$v_L = v_{SL'} - v_{SL} = V_{SL'} - v_{SL} = V_{SL} - v_{SL} \tag{10.87}$$

or

$$v_L = v_{LD} - v_{L'D} = v_{LD} - V_{L'D} = v_{LD} - V_{LD}. \tag{10.88}$$

For $0 < t \leq DT$, the switch is on, $v_{SL} = 0$, and

$$v_L = V_{SL}. \tag{10.89}$$

For $DT < t \leq (D + D_1)T$, the diode is on, $v_{LD} = 0$, and

$$v_L = -V_{LD}. \tag{10.90}$$

For $(D + D_1)T < t \leq T$, $i_L = 0$, and therefore $v_L = 0$. Hence, the voltage across the inductor can be summarized as follows:

$$v_L = \begin{cases} V_{SL}, & \text{for } 0 < t \leq DT, \\ -V_{LD}, & \text{for } DT < t \leq (D + D_1)T, \\ 0, & \text{for } (D + D_1)T < t \leq T, \end{cases} \tag{10.91}$$

resulting in the inductor current

$$i_L = \frac{1}{L}\int_0^t v_L\,dt = \frac{V_{SL}}{L}t, \quad \text{for } 0 < t \le DT, \tag{10.92}$$

from which the peak inductor current is found to be

$$\Delta i_L = i_L(DT) = \frac{DV_{SL}}{f_s L}. \tag{10.93}$$

Similarly,

$$i_L = \frac{1}{L}\int_{DT}^t v_L\,dt = \frac{-V_{LD}}{L}(t - DT), \quad \text{for } DT < t \le (D + D_1)T. \tag{10.94}$$

The peak inductor current can also be calculated as follows:

$$\Delta i_L = \frac{1}{L}\int_{(D+D_1)T}^{DT} i_L\,dt = \frac{1}{L}\int_{(D+D_1)T}^{DT} (-V_{LD})\,dt = \frac{D_1 V_{LD}}{f_s L}. \tag{10.95}$$

Thus,

$$\frac{D_1}{D} = \frac{V_{SL}}{V_{LD}}. \tag{10.96}$$

Figure 10.19 shows the steady-state current waveforms for DCM. The inductor current waveform is given by

$$i_L = \begin{cases} \dfrac{\Delta i_L}{DT}t, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L}{D_1 T}(t - DT), & \text{for } DT < t \le (D + D_1)T, \\ 0, & \text{for } (D + D_1)T < t \le T, \end{cases} \tag{10.97}$$

yielding the dc component of the inductor current,

$$I_L = \frac{1}{T}\int_0^T i_L\,dt = \frac{D + D_1}{2}\Delta i_L. \tag{10.98}$$

The waveform of the switch current is described by

$$i_S = \begin{cases} \dfrac{\Delta i_L}{DT}t, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le T, \end{cases} \tag{10.99}$$

which gives the dc component of the switch current,

$$I_S = \frac{1}{T}\int_0^T i_S\,dt = \frac{D}{2}\Delta i_L. \tag{10.100}$$

Substitution of (10.93) into (10.100) yields

$$I_S = \frac{D^2 V_{SL}}{2 f_s L}. \tag{10.101}$$

Similarly, the diode current waveform is given by

$$i_D = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ -\dfrac{\Delta i_L}{D_1 T}(t - DT), & \text{for } DT < t \le (D + D_1)T, \\ 0, & \text{for } (D + D_1)T < t \le T, \end{cases} \tag{10.102}$$

resulting in the dc component of the diode current,

$$I_D = \frac{1}{T}\int_0^T i_D\,dt = \frac{D_1}{2}\Delta i_L. \tag{10.103}$$

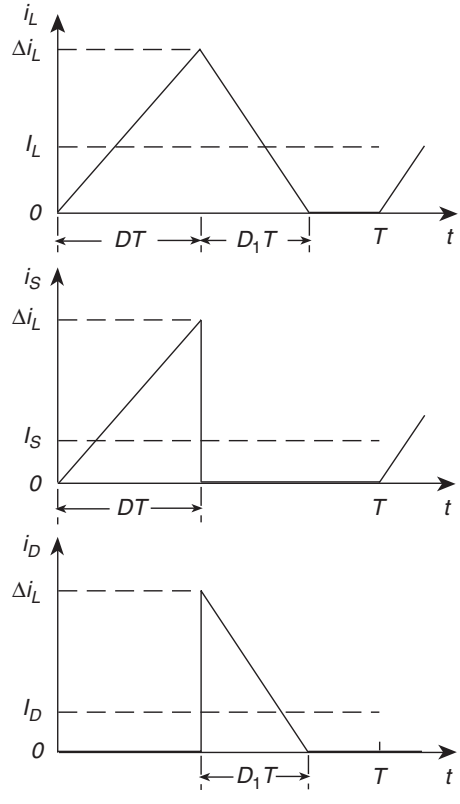


Figure 10.19 Current waveforms in PWM converters for DCM.

Dividing (10.103) by (10.100),

$$\frac{I_D}{I_S} = \frac{D_1}{D}. \tag{10.104}$$

Substituting (10.93) into (10.103) gives

$$I_D = \frac{D_1 D V_{SL}}{2 f_s L}. \tag{10.105}$$

Hence, using (10.96), one obtains

$$I_D = \frac{D^2 V_{SL}^2}{2 f_s L V_{LD}}. \tag{10.106}$$

From (10.96) and (10.104),

$$\frac{I_D}{I_S} = \frac{V_{SL}}{V_{LD}} = \frac{D_1}{D}. \tag{10.107}$$

The voltage v_{SD} across the series combination of the switch and the diode is not pulsating and is equal to its dc component V_{SD}. Hence, the voltage across the switch is

$$v_{SL} = \begin{cases} 0, & \text{for } 0 < t \le DT, \\ V_{SD}, & \text{for } DT < t \le (D + D_1)T, \\ V_{SL}, & \text{for } (D + D_1)T < t \le T, \end{cases} \tag{10.108}$$

where V_{SL} is the dc component of the voltage across the switch, and V_{SD} is the dc component of the voltage across both the switch and the diode. This leads to the dc component of the voltage across the switch,

$$V_{SL} = \frac{1}{(D+D_1)T}\int_0^{(D+D_1)T} v_{SL}\,dt = \frac{1}{(D+D_1)T}\int_{DT}^{(D+D_1)T} V_{SD}\,dt = \frac{D_1}{D+D_1}V_{SD}. \tag{10.109}$$

The voltage across the diode is

$$v_{LD} = \begin{cases} V_{SD}, & \text{for } 0 < t \le DT, \\ 0, & \text{for } DT < t \le (D+D_1)T, \\ V_{LD}, & \text{for } (D+D_1)T < t \le T, \end{cases} \tag{10.110}$$

where V_{LD} is the dc component of the voltage across the diode. The dc component of the diode voltage is

$$V_{LD} = \frac{1}{(D+D_1)T}\int_0^{(D+D_1)T} v_{LD}\,dt = \frac{1}{(D+D_1)T}\int_0^{DT} V_{SD}\,dt = \frac{D}{D+D_1}V_{SD}. \tag{10.111}$$

Dividing (10.111) by (10.109), one obtains

$$\frac{D_1}{D} = \frac{V_{SL}}{V_{LD}}. \tag{10.112}$$

10.10.2 Small-signal Model of Ideal Switching Network for DCM

Using relationship (10.101) for the dc components, one can write the identical relationship among the large-signal, slowly-varying components,

$$i_S = \frac{d_T^2 v_{SL}}{2f_s L}, \tag{10.113}$$

where each large-signal component may be expressed as a sum of a dc component and an ac component,

$$i_S = I_S + i_s, \tag{10.114}$$

$$v_{SL} = V_{SL} + v_{sl}, \tag{10.115}$$

and

$$d_T = D + d. \tag{10.116}$$

Substituting (10.114), (10.115), and (10.116) into (10.113), one obtains the switch current

$$I_S + i_s = \frac{(D+d)^2(V_{SL}+v_{sl})}{2f_s L} = \frac{(D^2+2Dd+d^2)(V_{SL}+v_{sl})}{2f_s L}. \tag{10.117}$$

For $d \ll D$, this equation can be approximated by

$$\begin{aligned} I_S + i_s &\approx \frac{(D^2+2Dd)(V_{SL}+v_{sl})}{2f_s L} \\ &= \frac{D^2 V_{SL}}{2f_s L} + \frac{D^2}{2f_s L}v_{sl} + \frac{DV_{SL}}{f_s L}d + \frac{D}{f_s L}v_{sl}d. \end{aligned} \tag{10.118}$$

Neglecting the product of the small-signal component $v_{sl}d$, one arrives at

$$I_S + i_s = \frac{D^2 V_{SL}}{2f_s L} + \frac{D^2}{2f_s L} v_{sl} + \frac{DV_{SL}}{f_s L} d = G_i V_{SL} + g_i v_{sl} + k_i d,$$
$$= \frac{V_{SL}}{R_i} + \frac{v_{sl}}{r_i} + k_i d, \tag{10.119}$$

from which one obtains the dc component of the switch current,

$$I_S = \frac{D^2 V_{SL}}{2f_s L} = \frac{V_{SL}}{R_i}, \tag{10.120}$$

and the ac small-signal component of the switch current,

$$i_s = \frac{v_{sl}}{r_i} + k_i d, \tag{10.121}$$

where

$$R_i = \frac{1}{G_i} \equiv \frac{V_{SL}}{I_S} = \frac{2f_s L}{D^2} = \frac{V_{SL}}{I_S} = \frac{V_{SL}^2}{I_D V_{LD}}, \tag{10.122}$$

$$r_i = \frac{1}{g_i} \equiv \frac{v_{sl}}{i_s} \mid_{d=0} = \frac{2f_s L}{D^2} = \frac{V_{SL}}{I_S} = \frac{V_{SL}^2}{I_D V_{LD}}, \tag{10.123}$$

and

$$k_i \equiv \frac{i_s}{d} \mid_{v_{sl}=0} = \frac{DV_{SL}}{f_s L} = \frac{2I_S}{D} = \frac{2I_D V_{LD}}{DV_{SL}}. \tag{10.124}$$

Note that $R_i = r_i$.

Using (10.106), the relationship among the large-signal, slowly-varying quantities is given by

$$i_D = \frac{d_T^2 v_{SL}^2}{2f_s L v_{LD}}, \tag{10.125}$$

where each large-signal component can be expressed as a sum of a dc components and an ac components

$$i_D = I_D + i_d, \tag{10.126}$$

$$d_T = D + d, \tag{10.127}$$

$$v_{SL} = V_{SL} + v_{sl}, \tag{10.128}$$

$$v_{LD} = V_{LD} + v_{ld}. \tag{10.129}$$

Substitution of (10.126)–(10.129) into (10.125) yields

$$I_D + i_d = \frac{(D+d)^2 (V_{SL} + v_{sl})^2}{2f_s L (V_{LD} + v_{ld})} = \frac{(D^2 + 2Dd + d^2)(V_{SL}^2 + 2V_{SL} v_{sl} + v_{sl}^2)}{2f_s L V_{LD} \left(1 + \dfrac{v_{ld}}{V_{LD}}\right)}. \tag{10.130}$$

Next, the approximation

$$\frac{1}{1 + \dfrac{v_{ld}}{V_{LD}}} \approx 1 - \frac{v_{ld}}{V_{LD}}, \quad \text{for } v_{ld} \ll V_{LD}, \tag{10.131}$$

can be made. Hence, for $v_{sl} \ll V_{SL}$ and $d \ll D$, the terms d^2 and v_{sl}^2 can be neglected and relationship (10.130) can be approximated by

$$I_D + i_d \approx \frac{(D^2 + 2Dd)(V_{SL}^2 + 2V_{SL}v_{sl})}{2f_sLV_{LD}}\left(1 - \frac{v_{ld}}{V_{LD}}\right)$$
$$= \frac{D^2V_{SL}^2 + 2D^2V_{SL}v_{sl} + 2DV_{SL}^2d + 4DV_{SL}v_{sl}d}{2f_sLV_{LD}}\left(1 - \frac{v_{ld}}{V_{LD}}\right). \quad (10.132)$$

Neglecting the small-signal component product $v_{sl}d$,

$$I_D + i_d \approx \frac{D^2V_{SL}^2}{2f_sLV_{LD}} + \frac{D^2V_{SL}}{f_sLV_{LD}}v_{sl} + \frac{DV_{SL}^2}{f_sLV_{LD}}d - \frac{D^2V_{SL}^2}{2f_sLV_{LD}^2}v_{ld}$$
$$- \frac{D^2V_{SL}}{f_sLV_{LD}^2}v_{sl}v_{ld} - \frac{DV_{SL}^2}{f_sLV_{LD}^2}v_{sl}d. \quad (10.133)$$

Neglecting the terms containing the products of small-signal components $v_{sl}v_{ld}$ and $v_{ld}d$, one obtains

$$I_D + i_d \approx \frac{D^2V_{SL}^2}{2f_sLV_{LD}} + \frac{D^2V_{SL}}{f_sLV_{LD}}v_{sl} + \frac{DV_{SL}^2}{f_sLV_{LD}}d - \frac{D^2V_{SL}^2}{2f_sLV_{LD}^2}v_{ld}$$
$$= \frac{D^2V_{SL}^2}{2f_sV_{LD}} + g_mv_{sl} + k_od - g_ov_{ld}$$
$$= \frac{D^2V_{SL}^2}{2f_sV_{LD}} + g_mv_{sl} + k_od - \frac{v_{ld}}{r_o}, \quad (10.134)$$

from which

$$I_D = \frac{D^2V_{SL}^2}{2f_sLV_{LD}} \quad (10.135)$$

and

$$i_d = g_mv_{sl} + k_od - \frac{v_{ld}}{r_o}, \quad (10.136)$$

where

$$g_m \equiv \frac{i_d}{v_{sl}}\Big|_{d=0 \text{ and } v_{ld}=0} = \frac{D^2V_{SL}}{f_sLV_{LD}} = \frac{2I_D}{V_{SL}} = \frac{2I_S}{V_{LD}}, \quad (10.137)$$

$$k_o \equiv \frac{i_d}{d}\Big|_{v_{sl}=v_{ld}=0} = \frac{DV_{SL}^2}{f_sLV_{LD}} = \frac{2I_D}{D} = \frac{2I_SV_{SL}}{DV_{LD}}, \quad (10.138)$$

and

$$r_o = \frac{1}{g_o} \equiv \frac{v_{ld}}{i_d}\Big|_{d=0 \text{ and } v_{sl}=0} = \frac{2f_sLV_{LD}^2}{D^2V_{SL}^2} = \frac{V_{LD}}{I_D} = \frac{V_{LD}^2}{I_SV_{SL}}. \quad (10.139)$$

The combination of the dc and small-signal models of PWM converters for DCM described by (10.119) and (10.134) is shown in Figure 10.20(a). Figure 10.20(b) depicts a small-signal model of the PWM converters for DCM described by (10.121) and (10.136). Figure 10.20(c) shows a dc model of the PWM converters for DCM described by (10.120) and (10.135).

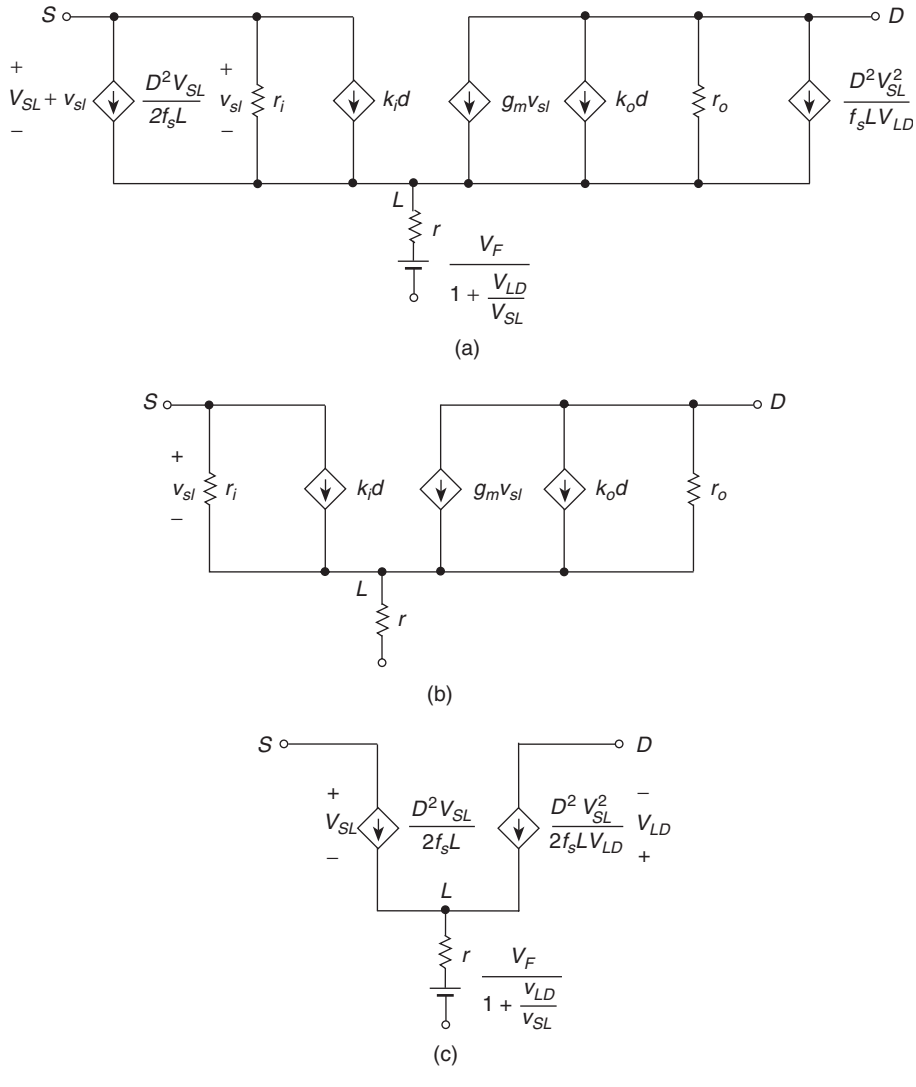


Figure 10.20 Models of PWM converters for DCM. (a) DC and small-signal model. (b) Small-signal model. (c) DC model.

10.11 Averaged Parasitic Resistances for DCM

Using (10.98), the rms values of the inductor, switch, and diode currents are

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^T i_L^2\,dt} = \Delta i_L\sqrt{\frac{D+D_1}{3}} = I_L\sqrt{\frac{4}{3(D+D_1)}}, \tag{10.140}$$

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2\,dt} = \Delta i_L\sqrt{\frac{D}{3}} = I_L\sqrt{\frac{4D}{3(D+D_1)^2}}, \tag{10.141}$$

and

$$I_{Drms} = \sqrt{\frac{1}{T}\int_0^T i_D^2\, dt} = \Delta i_L \sqrt{\frac{D_1}{3}} = I_L \sqrt{\frac{4D_1}{3(D+D_1)^2}}. \tag{10.142}$$

From (10.98) and (10.140), the power loss in the inductor resistance r_L is

$$P_{rL} = r_L I_{Lrms}^2 = \left(\frac{D+D_1}{3}\right) r_L \Delta i_L^2 = \frac{4}{3(D+D_1)} r_L I_L^2. \tag{10.143}$$

The power loss in the inductor resistance r_L may also be described in terms of the inductor average current I_L and the averaged inductor resistance in the inductor branch $r_{rLAV(L)}$,

$$P_{rLAV(L)} = r_{LAV(L)} I_L^2. \tag{10.144}$$

Hence, using the law of conservation of energy, one arrives at the averaged inductor resistance connected in series with the inductor L,

$$r_{LAV(L)} = \frac{4r_L}{3(D+D_1)}. \tag{10.145}$$

The power loss in the switch on-resistance r_{DS} is

$$P_{rDS} = r_{DS} I_{Srms}^2 = \left(\frac{D}{3}\right) r_{DS} \Delta i_L^2 = \frac{4D}{3(D+D_1)^2} r_{DS} I_L^2. \tag{10.146}$$

This power loss can be also expressed in terms of the dc inductor current I_L as

$$P_{rDSAV(L)} = r_{DSAV(L)} I_L^2. \tag{10.147}$$

Thus, the switch averaged resistance in the inductor branch is

$$r_{DSAV(L)} = \frac{4Dr_{DS}}{3(D+D_1)^2}. \tag{10.148}$$

The power loss in the diode forward resistance R_F is

$$P_{RF} = R_F I_{Drms}^2 = \left(\frac{D_1}{3}\right) R_F \Delta i_L^2 = \frac{4D_1}{3(D+D_1)^2} R_F I_L^2. \tag{10.149}$$

The power loss in the diode forward resistance can be also expressed in terms of the dc inductor current as

$$P_{RF\ AV(L)} = R_{F\ AV(L)} I_L^2. \tag{10.150}$$

Thus, the diode averaged resistance in the inductor branch is

$$R_{F\ AV(L)} = \frac{4D_1 R_F}{3(D+D_1)^2}. \tag{10.151}$$

From (10.145), (10.148), and (10.151), one obtains the total averaged resistance connected in series with the inductor L,

$$\begin{aligned} r &= r_{LAV(L)} + r_{DSAV(L)} + R_{F\ AV(L)} = \frac{4}{3(D+D_1)}\left(r_L + \frac{Dr_{DS} + D_1 R_F}{D+D_1}\right) \\ &= \frac{4}{3D\left(\dfrac{V_{SL}}{V_{LD}} + 1\right)}\left(r_L + \frac{r_{DS} + \dfrac{V_{SL}}{V_{LD}} R_F}{\dfrac{V_{SL}}{V_{LD}} + 1}\right). \end{aligned} \tag{10.152}$$

The power loss in the diode offset voltage is

$$P_{VF} = V_F I_D = \frac{D_1 I_L V_F}{D + D_1}. \tag{10.153}$$

On the other hand, this power may be written as

$$P_{VF\,AV(L)} = V_{F\ AV(L)} I_L. \tag{10.154}$$

Hence, the averaged diode offset voltage connected in series with inductor L is

$$V_{F\,AV(L)} = \frac{D_1}{D + D_1} V_F = \frac{V_F}{\dfrac{D}{D_1} + 1} = \frac{V_F}{\dfrac{V_{LD}}{V_{SL}} + 1}. \tag{10.155}$$

10.12 Small-signal Models of PWM Converters for DCM

Figures 10.21–10.23 depict small-signal models for buck, boost, and buck-boost converters, respectively. Figure 10.24 shows a block diagram of a small-signal model for a power stage of PWM dc–dc converters. There are three small-signal inputs d, v_i, and i_o, where v_i and i_o are disturbances and d is a control parameter used to control the converter against these disturbances. There are also two small-signal outputs v_o and i_l. The small-signal model may be described by six transfer functions: $T_p = v_o'/d$, $M_v = v_o''/v_i$, $Z_o = -v_o'''/i_o$, $T_{pi} = i_l'/d$, $M_{vi} = i_l''/v_i$, and $A_i = i_l'''/i_o$. These transfer functions will be studied in subsequent chapters.

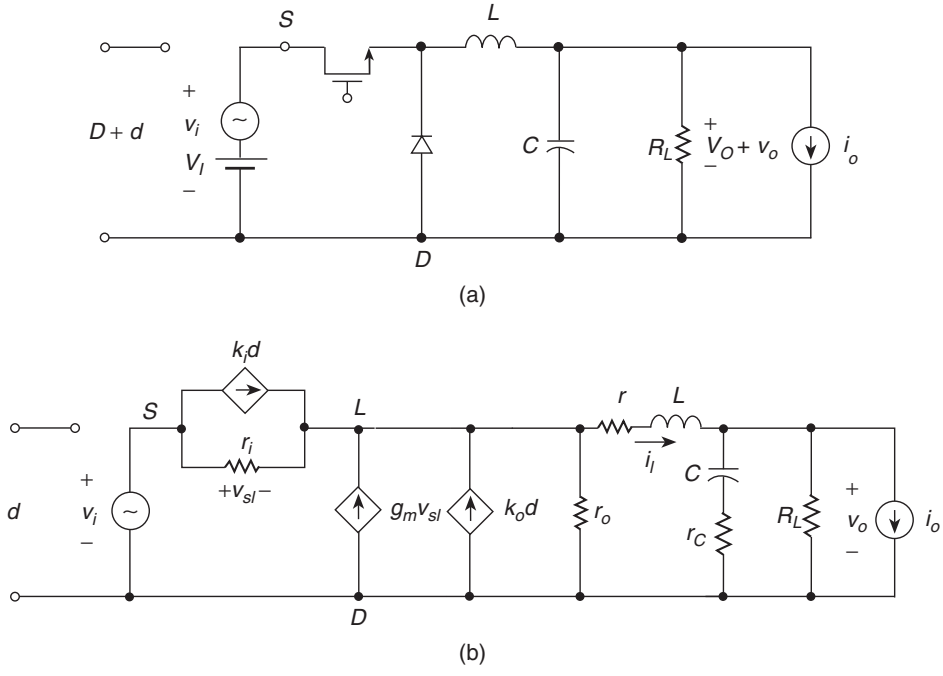


Figure 10.21 Small-signal model of PWM buck converter for DCM. (a) Buck converter. (b) Small-signal model for DCM.

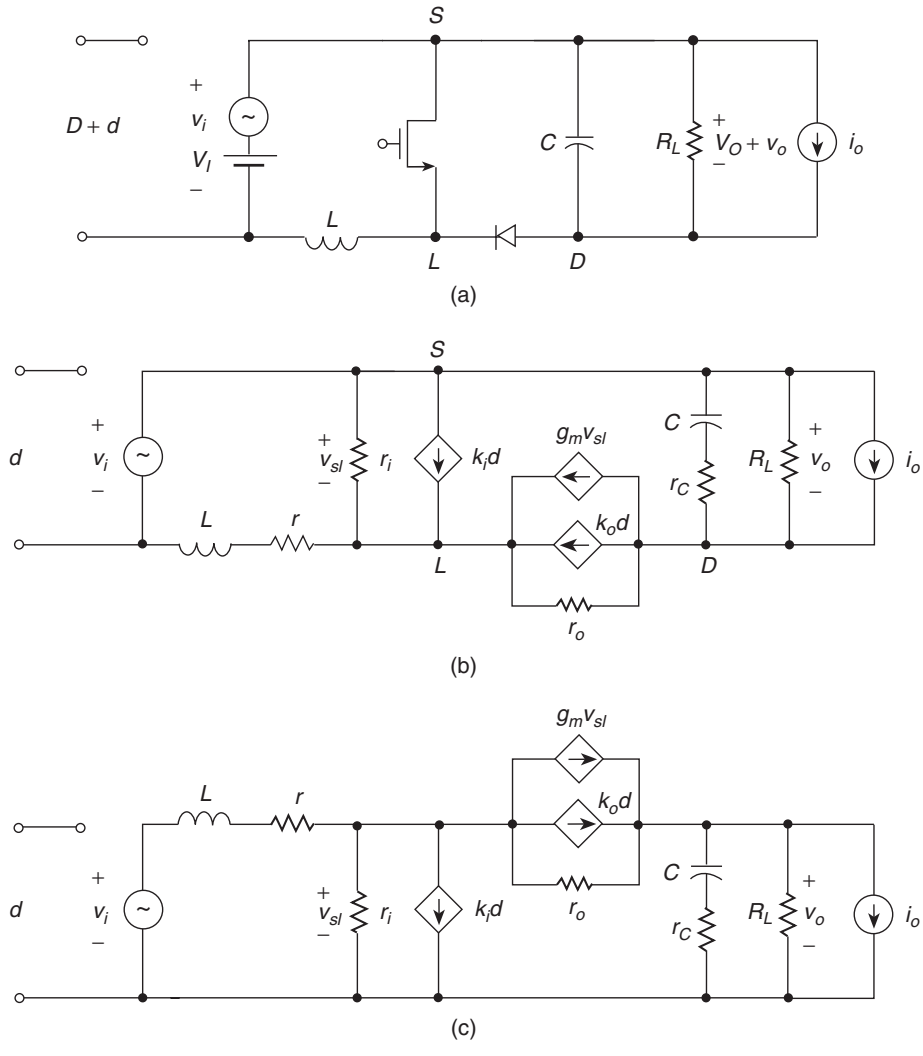


Figure 10.22 Small-signal model of PWM boost converter for DCM. (a) Boost converter. (b) Small-signal model for DCM. (c) Small-signal model for boost converter with some components moved to the upper branches.

10.13 Summary

- An ideal MOSFET can be modeled for dc components using an ideal dc current-dependent current source.
- An ideal diode can be modeled for dc components using an ideal dc voltage-dependent voltage source.
- An ideal switching network can be modeled for dc components using an ideal dc current-dependent current source and an ideal dc voltage-dependent voltage source.
- The MOSFET on-resistance r_{DS} and the diode forward resistance R_F can be averaged using the law of conservation of energy.

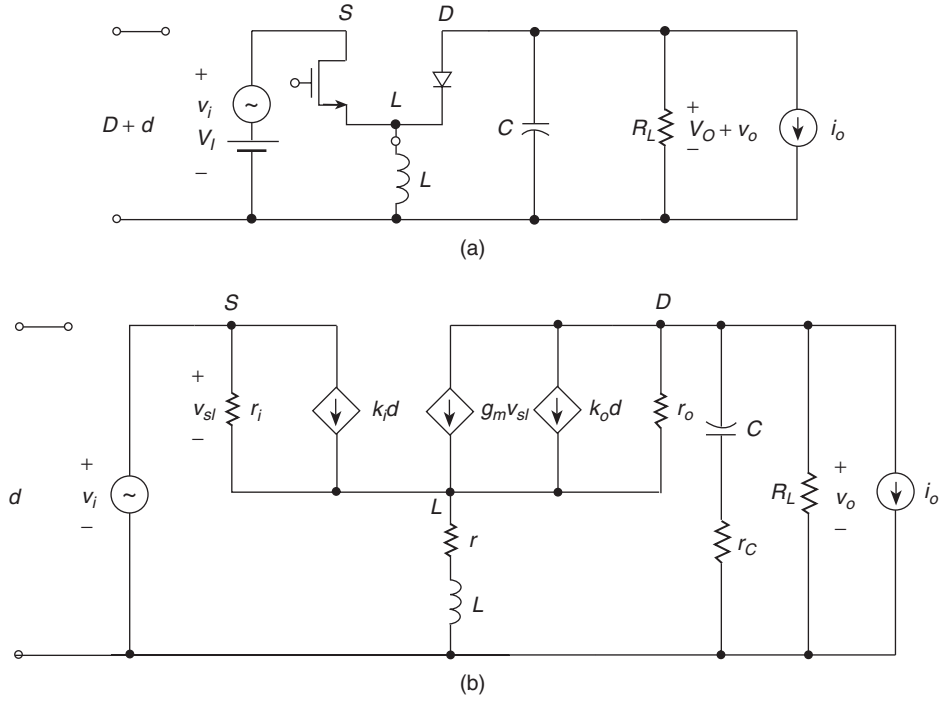


Figure 10.23 Small-signal model of PWM buck-boost converter for DCM. (a) Buck-boost converter. (b) Small-signal model for DCM.

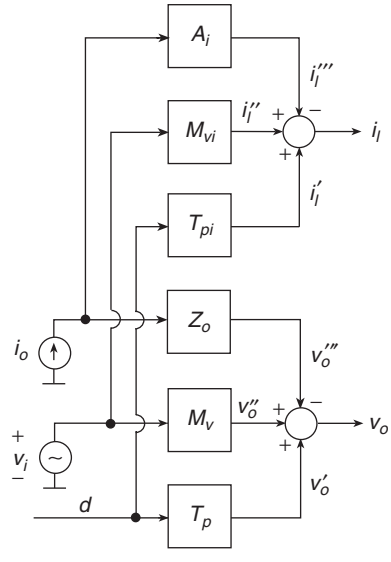


Figure 10.24 Block diagram of a small-signal model of dc–dc converters.

- The averaged transistor and diode resistances and the averaged offset voltage source can be moved to different branches using the reflection rules.
- The averaged model of the actual switching network for dc components can be converted to a large-signal model.
- The large-signal model can be transformed into a bilinear model for both dc and small-signal ac components.
- The bilinear model can be simplified to a linear model for both dc and small-signal components. Since this model is linear, it can be split into a linear small-signal circuit model and a linear dc circuit model.
- The small-signal model of PWM converters is valid only at low frequencies ranging from dc to the Nyquist frequency $f_s/2$.
- The dc circuit model can be used to study the open- and closed-loop converter behavior at dc.
- The small-signal circuit model can be used to study the open- and closed-loop dynamic performance of a PWM converter.

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10.15 Review Questions

10.1. Draw an ideal switching network of single-ended PWM converters.

10.2. Draw an actual switching network of single-ended PWM converters.

10.3. Draw an averaged large-signal model of an ideal switch for CCM.

10.4. Draw an averaged large-signal model of an ideal diode for CCM.

10.5. Draw an averaged large-signal model of an ideal switching network for CCM.

10.6. Draw an averaged large-signal model of an actual switch for CCM.

10.7. Draw an averaged large-signal model of an actual diode for CCM.

10.8. Draw an averaged large-signal model of an actual switching network with all the components in original branches for CCM.

10.9. Draw a simplified averaged large-signal model of an actual switching network for CCM.

10.10. Draw a nonlinear (bilinear) model of an actual switching network for CCM.

10.11. Draw a small-signal model of an actual switching network for CCM.

10.12. Draw a dc model of an actual switching network for CCM.

10.13. What is the frequency range in which the averaged small-signal model of the switching network is valid?

10.14. Draw a PWM small-signal switch model for CCM.

10.15. Draw a dc model of the actual switching network for DCM.

10.16. Draw a small-signal model of the actual switching network for DCM.

10.16 Problems

10.1. A single-ended transformerless PWM converter is operated under steady-state conditions in CCM. The duty cycle is $D = 0.4$. Find the components of an averaged model of the ideal switching network.

10.2. The parasitic components of a single-ended transformerless PWM converter operated under steady-state conditions in CCM are $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and the duty cycle is $D = 0.4$. Find the values of the averaged parasitic components in the original branches.

10.3. The parasitic components of a single-ended transformerless PWM converter operated under steady-state conditions in CCM are $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and the duty cycle is $D = 0.4$. Find the values of the averaged parasitic components in the inductor branch.

10.4. The parasitic components of a single-ended transformerless PWM converter operated under steady-state conditions in CCM are $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and the duty cycle is $D = 0.4$. Find the values of the averaged parasitic components in the switch branch.

10.5. The parasitic components of a single-ended transformerless PWM converter operated under steady-state conditions in CCM are $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and the duty cycle is $D = 0.4$. Find the values of the averaged parasitic components in the diode branch.

10.6. The parasitic components of a single-ended transformerless PWM converter operated under steady-state conditions in CCM are $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, $r_L = 0.2\,\Omega$, and the duty cycle is $D = 0.4$. Find the total averaged parasitic resistance in the inductor branch.

10.7. The duty cycle of a single-ended transformerless PWM converter operated under steady-state conditions in CCM is $D = 0.4$ and the ESR of the inductor is $r_L = 0.2\,\Omega$. Find the resistance of the inductor ESR in (a) the switch branch and (b) the diode branch.

10.8. A single-ended transformerless PWM converter operated under steady-state conditions in CCM has $D = 0.4$, $V_{SD} = 24\,\text{V}$, $I_L = 1.8\,\text{A}$, $r_{DS} = 1\,\Omega$, $R_F = 24\,\text{m}\Omega$, $V_F = 0.7\,\text{V}$, and $r_L = 0.2\,\Omega$. Find the components of the small-signal model of the actual switching network with all parasitic elements in the inductor branch.

10.9. In a buck PWM converter with no parasitic components, the dc input voltage is turned on at $t = 0$. The inductance is high enough to operate the converter in CCM for steady state. Find the transient waveform of the inductor current without a switching-frequency component and its harmonics.

11

Open-loop Small-signal Characteristics of Boost Converter for CCM

11.1 Introduction

The aims of this chapter are: (1) to introduce dc and small-signal linear circuit models of the PWM boost dc–dc converter, taking into account parasitic resistances of reactive components and power switches and also the offset voltage of the power diode; (2) to derive and illustrate the dc voltage transfer function and the efficiency using the dc model; and (3) to derive and illustrate the small-signal open-loop control-to-output transfer function, input-to-output transfer function, input impedance, and output impedance using the small-signal model. Responses of the output voltage to step changes in the duty cycle, input voltage, and load current are also given. The dynamics of the PWM bost converter has been studied in [1]–[17].

11.2 DC Characteristics

A dc model of the boost converter is shown in Figure 11.1. This model can be derived by replacing switching devices in the boost converter with the dc model of the actual switching network, the inductance L with a short circuit, and the capacitance C with an open circuit. The equivalent resistance in the inductor branch is

$$r = Dr_{DS} + (1 - D)R_F + r_L. \tag{11.1}$$

Since the battery representing the diode offset voltage V_F is moved to the inductor branch,

$$V_{SD} = V_O. \tag{11.2}$$

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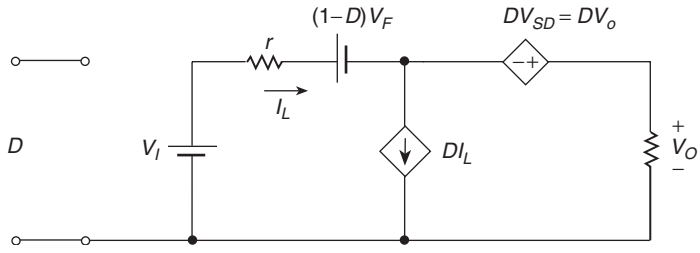


Figure 11.1 DC model of the PWM boost converter.

In addition,

$$I_I = I_L. \tag{11.3}$$

Using Kirchhoff's current law,

$$I_I - DI_I - I_O = 0, \tag{11.4}$$

which gives the dc current transfer function,

$$M_{IDC} \equiv \frac{I_O}{I_I} = 1 - D. \tag{11.5}$$

Since $I_O = V_O/R_L$,

$$I_I = I_L = \frac{I_O}{1-D} = \frac{V_O}{(1-D)R_L}. \tag{11.6}$$

By Kirchhoff's voltage law,

$$V_I - V_F(1-D) - rI_L + DV_O - V_O = 0, \tag{11.7}$$

which yields

$$V_O = \frac{V_I}{(1-D)\left[1 + \dfrac{V_F}{V_O} + \dfrac{r}{(1-D)^2 R_L}\right]}. \tag{11.8}$$

Hence, one obtains the dc input-to-output voltage transfer function

$$M_{VDC} \equiv \frac{V_O}{V_I} = \frac{1}{1-D}\,\frac{1}{1 + \dfrac{V_F}{V_O} + \dfrac{r}{(1-D)^2 R_L}} \tag{11.9}$$

and the dc control-to-output transfer function

$$T_{PDC} \equiv \frac{V_O}{D} = \frac{V_I}{D(1-D)\left[1 + \dfrac{V_F}{V_O} + \dfrac{r}{(1-D)^2 R_L}\right]}. \tag{11.10}$$

From (11.5) and (11.9), the efficiency of the converter is

$$\eta \equiv \frac{I_O V_O}{I_I V_I} = M_{IDC} M_{VDC} = (1-D)M_{VDC} = \frac{1}{1 + \dfrac{V_F}{V_O} + \dfrac{r}{R_L(1-D)^2}}. \tag{11.11}$$

Switching losses are neglected in this equation. Figures 11.2 and 11.3 show the dc voltage transfer function M_{VDC} and the efficiency η as a function of D at $R_L = 40\,\Omega$, $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $V_F = 0.3\,\text{V}$, $R_F = 72\,\text{m}\Omega$, and $r_L = 0.19\,\Omega$.

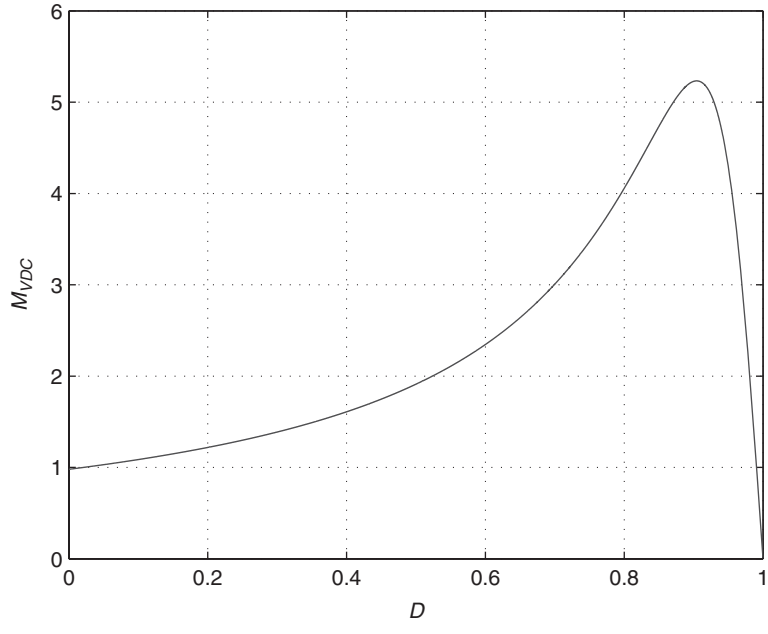


Figure 11.2 DC voltage transfer function M_{VDC} as a function of the duty cycle D at $R_L = 40\,\Omega$, $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $V_F = 0.3\,\text{V}$, $R_F = 72\,\text{m}\Omega$, and $r_L = 0.19\,\Omega$.

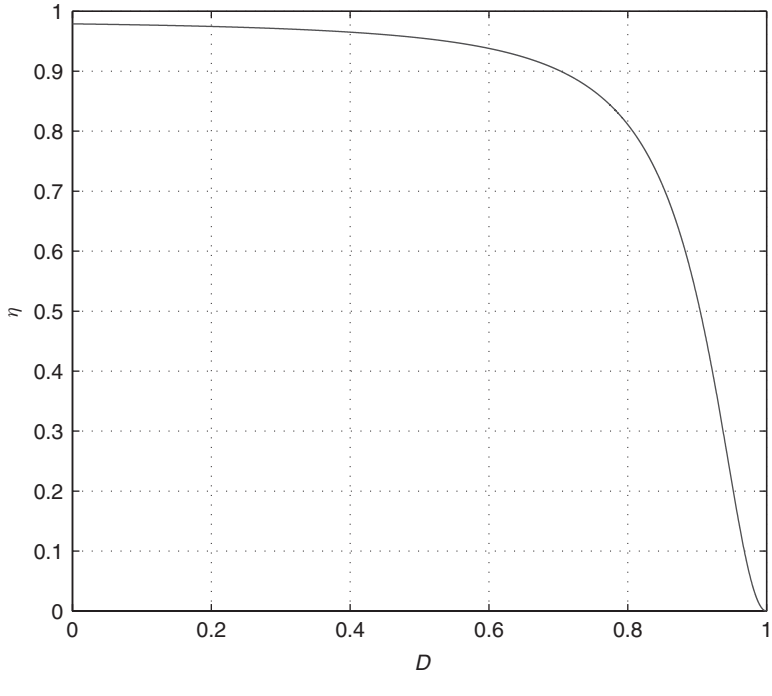


Figure 11.3 Efficiency η as a function of the duty cycle D at $R_L = 40\,\Omega$, $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $V_F = 0.3\,\text{V}$, $R_F = 72\,\text{m}\Omega$, and $r_L = 0.19\,\Omega$.

11.3 Open-loop Control-to-output Transfer Function

A small-signal model of the PWM boost converter for CCM operation is shown in Figure 11.4(a). This model is obtained by replacing the switching network in the boost converter with a small-signal model. Figure 11.4(b) shows a block diagram of the open-loop boost converter. Setting $v_i = 0$ and $i_o = 0$ in Figure 11.4(a), one obtains a small-signal model of the boost converter for determining the control-to-output transfer function shown in Figure 11.5. Note that

$$v_{sd} = v_o. \tag{11.12}$$

The current through the parallel combination of the load resistance and the filter capacitance is

$$i_{Z_2} = \frac{v_o}{Z_2}, \tag{11.13}$$

and the current through the inductor is

$$i_l = Di_l + I_L d + i_{Z_2} = Di_l + I_L d + \frac{v_o}{Z_2} \tag{11.14}$$

which, from (11.6), produces

$$i_l = \frac{I_L d}{1 - D} + \frac{v_o}{(1 - D)Z_2} = \frac{V_O d}{(1 - D)^2 R_L} + \frac{v_o}{(1 - D)Z_2}. \tag{11.15}$$

Using Kirchhoff's voltage law,

$$-i_l Z_1 + Dv_o + V_O d - v_o = 0. \tag{11.16}$$

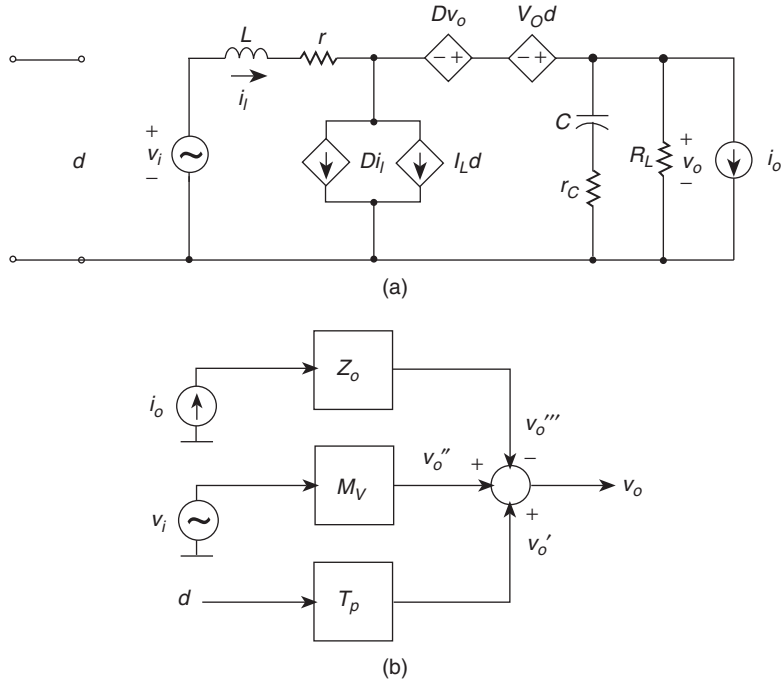


Figure 11.4 Small-signal model and block diagram of the PWM boost converter for CCM. (a) Small-signal model. (b) Block diagram.

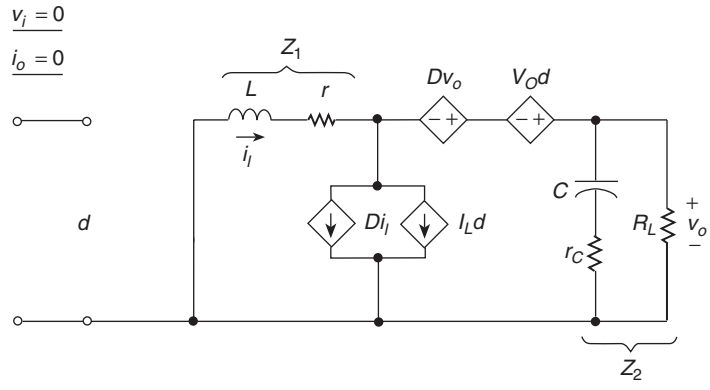


Figure 11.5 Small-signal model of the PWM boost converter for determining the control-to-output transfer function T_p.

Substituting (11.15) into (11.16) yields

$$-\frac{V_O d Z_1}{(1-D)^2 R_L} - \frac{v_o Z_1}{(1-D)Z_2} + V_O d = v_o(1-D), \tag{11.17}$$

which becomes

$$v_o(1-D)\left[1 + \frac{Z_1}{(1-D)^2 Z_2}\right] = dV_O\left[1 - \frac{Z_1}{(1-D)^2 R_L}\right]. \tag{11.18}$$

Hence, using (11.6), one obtains the control-to-output transfer function

$$T_p(s) \equiv \left.\frac{v_o(s)}{d(s)}\right|_{v_i = i_o = 0} = \frac{V_O}{1-D}\,\frac{1 - \dfrac{Z_1}{(1-D)^2 R_L}}{1 + \dfrac{Z_1}{(1-D)^2 Z_2}}. \tag{11.19}$$

The impedances Z_1 and Z_2 are

$$Z_1 = r + sL \tag{11.20}$$

and

$$Z_2 = \frac{R_L\left(r_C + \dfrac{1}{sC}\right)}{R_L + r_C + \dfrac{1}{sC}}. \tag{11.21}$$

Substitution of (11.20) and (11.21) into (11.19) gives the *control-to-output transfer function* (or the *duty ratio-to-output transfer function*) in the s-domain,

$$T_p(s) \equiv \left.\frac{v_o(s)}{d(s)}\right|_{v_i = i_o = 0}$$

$$= -\frac{V_O r_C}{(1-D)(R_L + r_C)}\,\frac{\left(s + \dfrac{1}{Cr_C}\right)\left\{s - \dfrac{1}{L}[R_L(1-D)^2 - r]\right\}}{s^2 + s\dfrac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{r + (1-D)^2 R_L}{LC(R_L + r_C)}}$$

$$= T_{px}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2} = T_{px}\frac{(s-z_n)(s-z_p)}{(s-p_1)(s-p_2)}$$

$$= \frac{V_O r_C \omega_{zn}\omega_{zp}}{(1-D)(R_L+r_C)\omega_0^2}\,\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{1+\dfrac{2\xi}{\omega_0}s+\left(\dfrac{s}{\omega_0}\right)^2} = T_{po}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{1+\dfrac{s}{Q\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2}, \tag{11.22}$$

where the magnitude of T_p at high frequencies is

$$T_{px} = T_p(\infty) = -\frac{V_O}{1-D}\,\frac{r_C}{R_L+r_C}, \tag{11.23}$$

the magnitude of T_p at $f = 0$ is

$$T_{po} = T_p(0) = \frac{V_O r_C \omega_{zn}\omega_{zp}}{(1-D)(R_L+r_C)\omega_0^2} = \frac{V_O}{1-D}\,\frac{R_L(1-D)^2-r}{R_L(1-D)^2+r} \approx \frac{V_O}{1-D}, \tag{11.24}$$

the angular *corner frequency* or the angular *undamped natural frequency* is

$$\omega_0 = \sqrt{\frac{(1-D)^2R_L+r}{LC(R_L+r_C)}} = \frac{1}{\sqrt{\tau_C\tau_L}} = p_1p_2, \tag{11.25}$$

the time constants are

$$\tau_C = C(R_L+r_C), \tag{11.26}$$

$$\tau_L = \frac{L/(1-D)^2}{R_L+r/(1-D)^2}, \tag{11.27}$$

the *damping ratio* is

$$\xi = \frac{L+C[r(R_L+r_C)+(1-D)^2R_Lr_C]}{2\sqrt{LC(R_L+r_C)[(1-D)^2R_L+r]}}, \tag{11.28}$$

the *quality factor* is

$$Q = \frac{1}{2\xi}, \tag{11.29}$$

the ESR zero, which is a left-half plane (LHP) or negative zero, is given by

$$z_n = -\frac{1}{Cr_C}, \tag{11.30}$$

the angular frequency of the ESR zero is

$$\omega_{zn} = -z_n = \frac{1}{Cr_C}, \tag{11.31}$$

the right-half plane (RHP) or positive zero and its angular frequency are

$$z_p = \omega_{zp} = \frac{R_L(1-D)^2-r}{L}, \tag{11.32}$$

and the poles are

$$p_1, p_2 = -\xi\omega_0 \pm \omega_0\sqrt{\xi^2-1} = -\xi\omega_0 \pm j\omega_0\sqrt{1-\xi^2} = -\sigma \pm j\omega_d. \tag{11.33}$$

The control-to-output transfer function T_p is a second-order low-pass function, which has two LHP poles, one LHP zero, and one RHP zero. The boost converter is a *non-minimum phase system* because it has an RHP zero. The LHP zero z_n is independent of D, whereas

the poles and the RHP zero depend on D. As D is increased from 0 to 1, the RHP zero z_p decreases from a maximum value of $(R_L - r)/L$, crosses zero, becomes negative, and reaches a minimum value of $-r/L$. In other words, z_p is moving from a location in the RHP to the origin, and then enters the LHP at $D = 1$. When D is increased from 0 to 1, the corner frequency f_0 decreases and the damping factor ξ increases. For $D = 0$, $r = R_F + r_L$ and

$$\omega_{0max} = \sqrt{\frac{R_L + r_L + R_F}{LC(R_L + r_C)}} \approx \frac{1}{LC}, \tag{11.34}$$

and for $D = 1$, $r = r_{DS} + r_L$ and

$$\omega_{0min} = \sqrt{\frac{r_{DS} + r_L}{LC(R_L + r_C)}} \approx 0. \tag{11.35}$$

Hence,

$$\frac{\omega_{0max}}{\omega_{0min}} = \sqrt{\frac{R_L + r_L + R_F}{r_{DS} + r_L}}. \tag{11.36}$$

Using the reflection rule, the resistance r can be moved from the inductor branch to the diode branch. This equivalent resistance is given by

$$r_e = \frac{r}{(1-D)^2} = \frac{Dr_{DS} + (1-D)R_F + r_L}{(1-D)^2}. \tag{11.37}$$

As D is increased from 0 to 1, r_e increases from $r_L + R_F$ to ∞. The equivalent inductance connected in series with the $C - r_C - R_L$ circuit is

$$L_e = \frac{L}{(1-D)^2}. \tag{11.38}$$

Another method for deriving the equivalent inductance L_e is based on the principle of energy conservation. The average inductor and diode currents are related by

$$i_L = \frac{i_D}{1-D}. \tag{11.39}$$

The energy stored in the inductance L located in its original branch is

$$W_L = \frac{1}{2}Li_L^2 = \frac{1}{2}L\frac{i_D^2}{(1-D)^2}, \tag{11.40}$$

and the energy stored in the equivalent inductance L_e located in the diode branch is

$$W_{Le} = \tfrac{1}{2}L_e i_D^2. \tag{11.41}$$

Hence, $L_e = L/(1-D)^2$.

Example 11.1

A boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$. Calculate r, z_n, f_{zn}, z_p, f_{zp}, f_0, ξ, Q, p_1, p_2, and f_d at $R_{Lmin} = 40\,\Omega$. Plot r, f_{zp}, f_0, and ξ versus D.

Solution. The total parasitic resistance in series with the inductor at $D_{nom} = 0.5$ is

$$\begin{aligned} r &= D_{nom}r_{DS} + (1 - D_{nom})R_F + r_L \\ &= 0.5 \times 0.18 + (1 - 0.5) \times 0.072 + 0.19 = 0.09 + 0.036 + 0.19 = 0.316\,\Omega. \end{aligned} \tag{11.42}$$

Figure 11.6 shows a plot of r versus D for $r_{DS} = 0.18\,\Omega$, $R_F = 72\,\text{m}\Omega$, and $r_L = 0.19\,\Omega$.

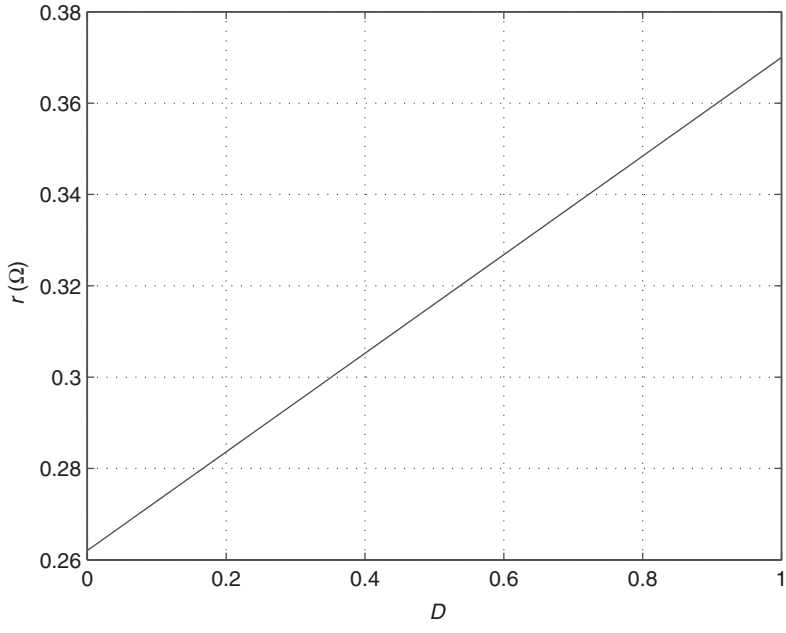


Figure 11.6 Total parasitic resistance r as a function of D for $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, and $r_L = 0.19\,\Omega$.

The LHP zero is

$$z_n = -\frac{1}{Cr_C} = -\frac{1}{68 \times 10^{-6} \times 0.111} = -132.49 \times 10^3 \text{ rad/s}, \tag{11.43}$$

and the frequency of the LHP zero is

$$f_{zn} = \frac{1}{2\pi Cr_C} = \frac{1}{2 \times \pi \times 68 \times 10^{-6} \times 0.111} = 21.09 \text{ kHz}. \tag{11.44}$$

The RHP zero is

$$z_p = \omega_{zp} = \frac{R_{Lmin}(1 - D_{nom})^2 - r}{L} = \frac{40 \times (1 - 0.5)^2 - 0.316}{156 \times 10^{-6}} = 62.08 \times 10^3 \text{ rad/s}, \tag{11.45}$$

and the frequency of the RHP zero is

$$f_{zp} = \frac{R_{Lmin}(1 - D_{nom})^2 - r}{2\pi L} = \frac{40 \times (1 - 0.5)^2 - 0.316}{2 \times \pi \times 156 \times 10^{-6}} = 9.88 \text{ kHz}. \tag{11.46}$$

Figure 11.7 shows a plot of f_0 versus D for $r_{DS} = 0.18\,\Omega$, $R_F = 72\,\text{m}\Omega$, $r_L = 0.19\,\Omega$, $r_C = 111\,\text{m}\Omega$, and $R_L = 40\,\Omega$.

The corner frequency is

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{(1 - D_{nom})^2 R_{Lmin} + r}{LC(R_{Lmin} + r_C)}} = \frac{1}{2\pi}\sqrt{\frac{(1 - 0.5)^2 \times 40 + 0.316}{156 \times 10^{-6} \times 68 \times 10^{-6} \times (40 + 0.111)}}$$
$$= 783.66 \text{ Hz}. \tag{11.47}$$

Figure 11.8 shows a plot of f_{zp} versus D for $r_{DS} = 0.18\,\Omega$, $R_F = 72\,\text{m}\Omega$, $r_L = 0.19\,\Omega$, $r_C = 111\,\text{m}\Omega$, and $R_L = 40\,\Omega$.

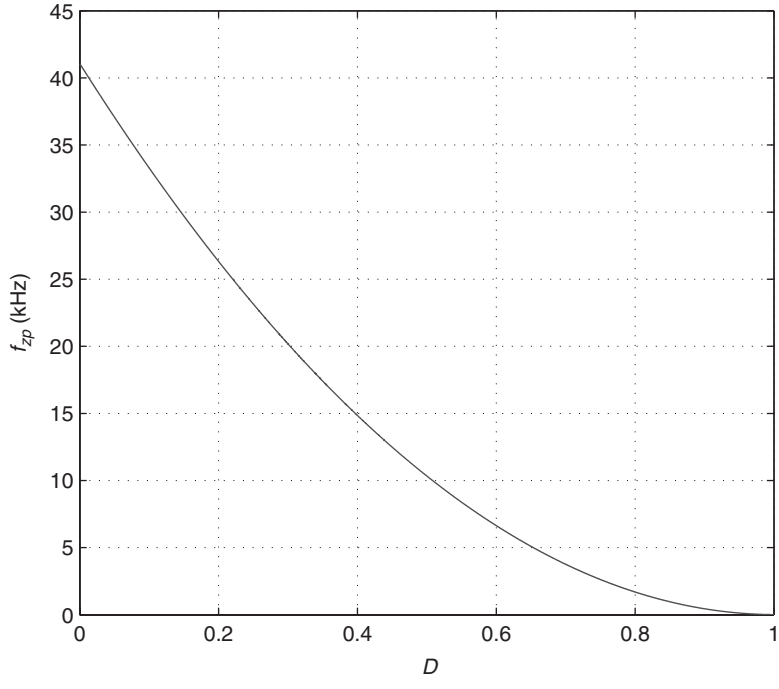


Figure 11.7 Frequency of the RHP zero f_{zp} as a function of D for the boost converter at $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$ for $R_L = 40\,\Omega$.

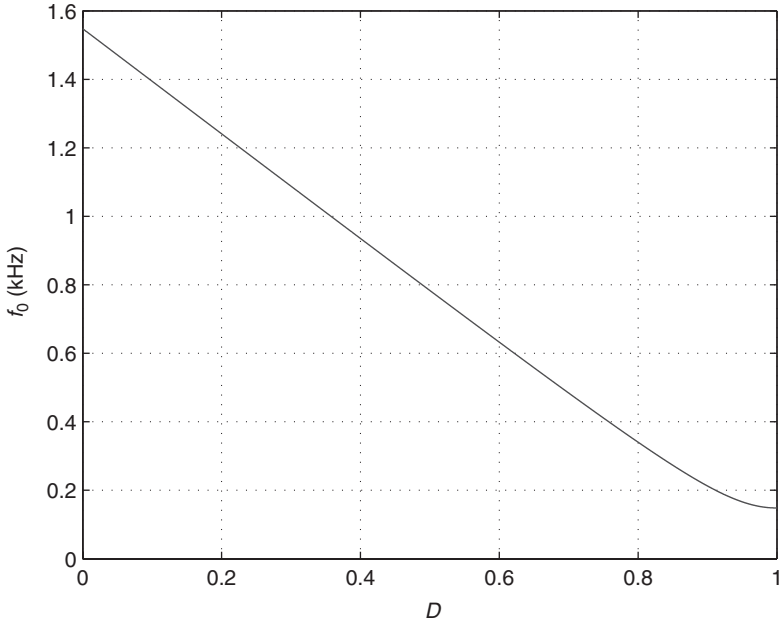


Figure 11.8 Corner frequency f_0 as a function of D for the boost converter at $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$ for $R_L = 40\,\Omega$.

The damping ratio is

$$\xi = \frac{C[r(R_{Lmin} + r_C) + (1 - D_{nom})^2 R_{Lmin} r_C] + L}{2\sqrt{LC(R_{Lmin} + r_C)[r + (1 - D_{nom})^2 R_{Lmin}]}}$$
$$= \frac{68 \times 10^{-6}[0.316 \times (40 + 0.111) + (1 - 0.5)^2 \times 40 \times 0.111] + 156 \times 10^{-6}}{2\sqrt{156 \times 10^{-6} \times 68 \times 10^{-6} \times (40 + 0.111)[0.316 + (1 - 0.5)^2 \times 40]}}$$
$$= \frac{1093.385 \times 10^{-6}}{4190.194 \times 10^{-6}} = 0.261, \tag{11.48}$$

and the quality factor is

$$Q = \frac{1}{2\xi} = \frac{1}{2 \times 0.261} = 1.916. \tag{11.49}$$

Figure 11.9 shows a plot of ξ versus D for $r_{DS} = 0.18\,\Omega$, $R_F = 72\,\text{m}\Omega$, $r_L = 0.19\,\Omega$, $r_C = 111\,\text{m}\Omega$, and $R_L = 40$, 80, and $200\,\Omega$.

The poles are

$$p_1, p_2 = -\sigma \pm j\omega_d = -\xi\omega_0 \pm j\omega_0\sqrt{1 - \xi^2}$$
$$= -0.261 \times 2 \times \pi \times 783.66 \pm j2 \times \pi \times 783.66\sqrt{1 - 0.261^2}$$
$$= -1285 \pm j4753\,(\text{rad/s}), \tag{11.50}$$

and the damped frequency is

$$f_d = f_0\sqrt{1 - \xi^2} = 783.66\sqrt{1 - 0.261^2} = 756.5\,\text{Hz}. \tag{11.51}$$

At $r = r_C = 0$, the approximate equations give $f_{zp} \approx R_{Lmin}(1 - D_{nom})^2/(2\pi L) = 20.4\,\text{kHz}$, $f_0 \approx (1/2\pi)\sqrt{(1 - D_{nom})^2/LC} = 772.6\,\text{Hz}$, $\xi \approx \sqrt{L/C}/[2R_{Lmin}(1 - D_{nom})] = 0.03787$,

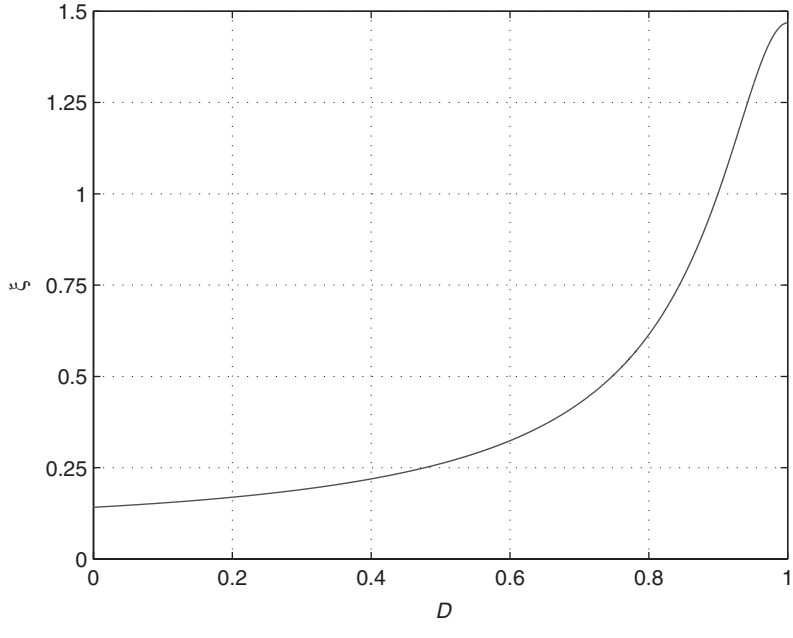


Figure 11.9 Damping ratio ξ as a function of D for $R_L = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$.

$Q = 1/2\xi \approx 13.2$, $p_1, p_2 \approx -184 \pm j4848.44$ rad/s, and $f_d \approx 771.49$ Hz. Note that $\xi_{lossy}/\xi_{lossless} = 0.261/0.03787 = 6.89$. Therefore, the parasitic components cannot be neglected.

Substitution of $s = j\omega$ into (11.22) yields

$$T_p(j\omega) = T_{po}\frac{\left(1 + j\dfrac{\omega}{\omega_{zn}}\right)\left(1 - j\dfrac{\omega}{\omega_{zp}}\right)}{1 - \left(\dfrac{\omega}{\omega_0}\right)^2 + j2\xi\left(\dfrac{\omega}{\omega_0}\right)} = |T_p|e^{j\phi_{Tp}}, \tag{11.52}$$

where

$$|T_p| = T_{po}\sqrt{\frac{\left[1 + \left(\dfrac{\omega}{\omega_{zn}}\right)^2\right]\left[1 + \left(\dfrac{\omega}{\omega_{zp}}\right)^2\right]}{\left[1 - \left(\dfrac{\omega}{\omega_0}\right)^2\right]^2 + 4\xi^2\left(\dfrac{\omega}{\omega_0}\right)^2}} \tag{11.53}$$

and

$$\phi_{Tp} = \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left(\frac{\omega}{\omega_{zp}}\right) - \arctan\left[\frac{2\xi\left(\dfrac{\omega}{\omega_0}\right)}{1 - \left(\dfrac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} \le 1, \tag{11.54}$$

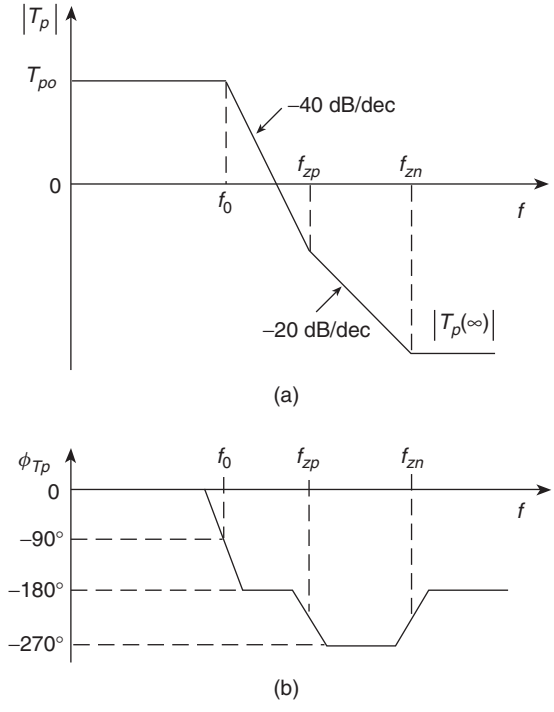


Figure 11.10 Idealized Bode plots of the open-loop control-to-output transfer function T_p for the boost converter (without the delay). (a) $|T_p|$ versus f. (b) ϕ_{Tp} versus f.

or

$$\phi_{Tp} = -180^\circ + \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left(\frac{\omega}{\omega_{zp}}\right) - \arctan\left[\frac{2\xi\left(\dfrac{\omega}{\omega_0}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} > 1. \tag{11.55}$$

Figure 11.10 shows idealized Bode plots of the open-loop control-to-output transfer function T_p for the boost converter.

11.4 Delay in Open-loop Control-to-output Transfer Function

The delay t_d introduced by a power transistors driver and pulse-width modulator can be described by the function $T_d = e^{-st_d}$. This function can be approximated by a first-order Padé rational function for frequencies from dc to $f_s/2$,

$$T_d(s) = e^{-st_d} \approx \frac{1-\dfrac{st_d}{2}}{1+\dfrac{st_d}{2}} = \frac{s-\dfrac{2}{t_d}}{s+\dfrac{2}{t_d}} = -\frac{s-\omega_{zd}}{s+\omega_{pd}}, \tag{11.56}$$

where $\omega_{zd} = \omega_{pd} = 2/t_d$. Hence, the control-to-output transfer function with the delay is

$$T_p(s) = -T_{px}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2}\frac{s-\omega_{zd}}{s+\omega_{pd}}. \tag{11.57}$$

Example 11.2

For the boost converter with $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $r = 0.316\,\Omega$, calculate T_{po} and $T_p(\infty)$ at $R_{Lmin} = 40\,\Omega$. Draw the Bode plots of T_p for $D = 0.5$ at $t_d = 0$ and $t_d = 1\,\mu\text{s}$.

Solution. From (11.24),

$$T_{po} = T_p(0) = \frac{V_O}{1-D_{nom}}\,\frac{R_{Lmin}(1-D_{nom})^2 - r}{R_{Lmin}(1-D_{nom})^2 + r} = \frac{20}{1-0.5}\,\frac{40\times(1-0.5)^2-0.316}{40\times(1-0.5)^2+0.316}$$
$$= 37.55\,\text{V} = 31.49\,\text{dBV}. \tag{11.58}$$

The approximate equation gives $T_{po} \approx V_O/(1-D_{nom}) = 20/(1-0.5) = 40\,\text{V} = 32\,\text{dBV}$. From (11.23),

$$T_{px} = T_p(\infty) = -\frac{V_O}{1-D_{nom}}\,\frac{r_C}{R_{Lmin}+r_C} = -\frac{20}{1-0.5}\,\frac{0.111}{40+0.111} = -0.1106\,\text{V}, \tag{11.59}$$

which gives $|T_{px}| = |T_p(\infty)| = -19\,\text{dBV}$. Figures 11.11 and 11.12 show Bode plots of T_p for the boost converter with and without the delay. The $-3\,\text{dB}$ bandwidth at $D = 0.5$ is $BW = 1\,\text{kHz}$.

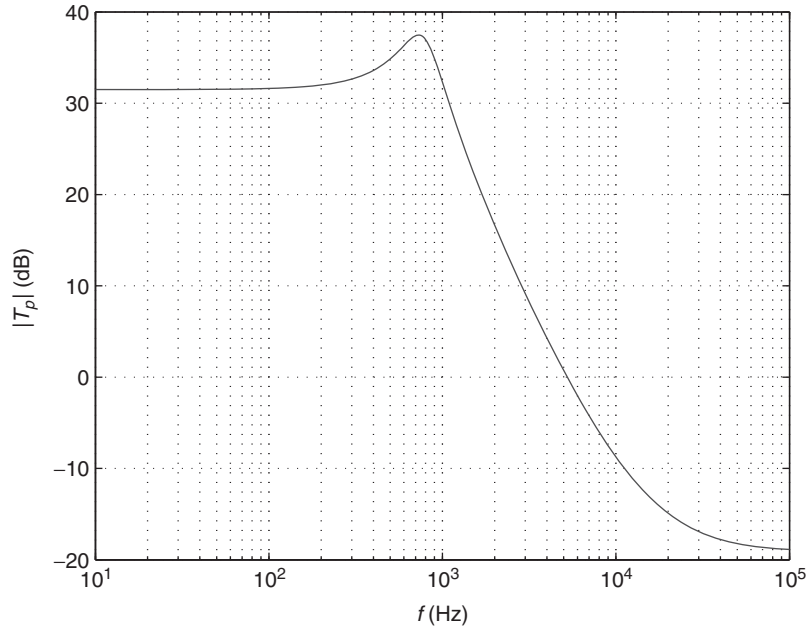


Figure 11.11 Bode plot of the magnitude of the open-loop control-to-output transfer function T_p with and without the delay $t_d = 1\,\mu s$ for the boost converter.

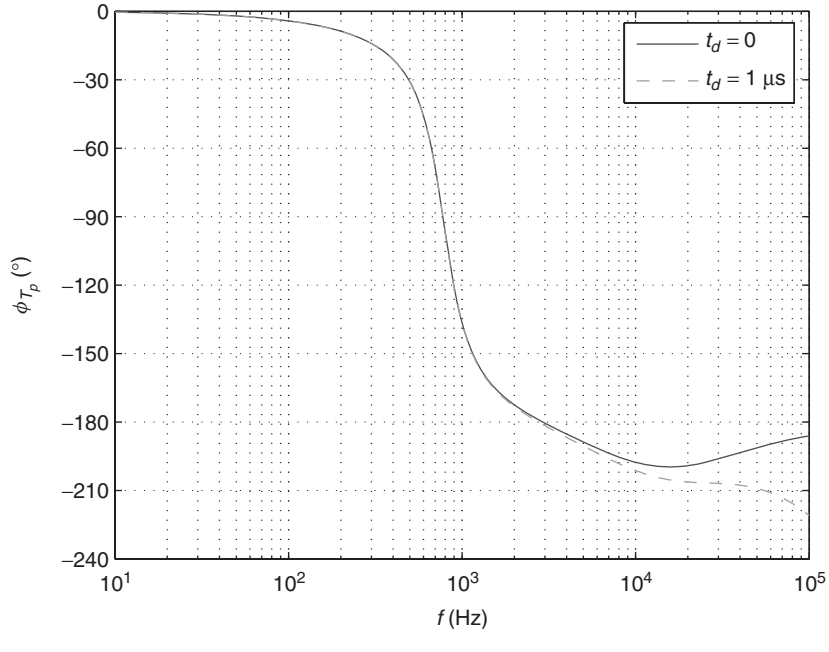


Figure 11.12 Bode plot of the phase of the open-loop control-to-output transfer function T_p for the boost converter with and without the delay $t_d = 1\,\mu s$.

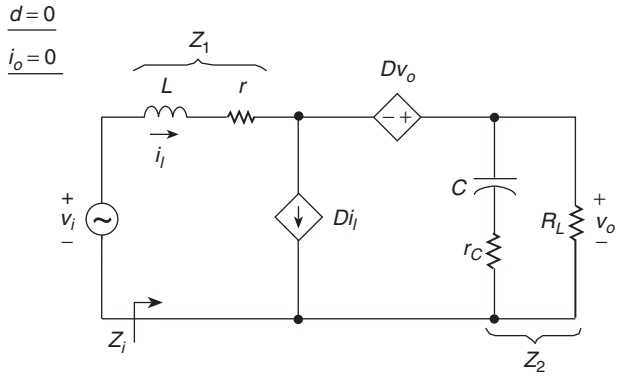


Figure 11.13 Small-signal model of the PWM boost converter for determining the input-to-output transfer function M_v.

11.5 Open-loop Audio Susceptibility

Setting $d = 0$ and $i_o = 0$ in the small-signal model of the boost converter of Figure 11.4 gives a small-signal model, shown in Figure 11.13, that can be used to derive the input-to-output voltage transfer function M_v. By Kirchhoff's current law,

$$i_l = Di_l + i_{Z_2} = Di_l + \frac{v_o}{Z_2}, \tag{11.60}$$

which can be rearranged into the form

$$i_l = \frac{i_{Z_2}}{1-D} = \frac{v_o}{(1-D)Z_2}. \tag{11.61}$$

By Kirchhoff's voltage law,

$$v_i - i_l Z_1 + Dv_o - v_o = 0. \tag{11.62}$$

Substitution of (11.61) into (11.62) gives

$$v_i = v_o(1-D)\left[1 + \frac{Z_1}{(1-D)^2 Z_2}\right]. \tag{11.63}$$

Thus, the open-loop input-to-output transfer function

$$M_v(s) \equiv \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{1}{1-D}\,\frac{Z_2}{Z_2 + \dfrac{Z_1}{(1-D)^2}} \tag{11.64}$$

is obtained. Substituting (11.20) and (11.21) into (11.64), one obtains the *input-to-output voltage transfer function* (also called the *line-to-output voltage transfer function* or the *audio susceptibility*)

$$M_v(s) \equiv \left.\frac{v_o(s)}{v_i(s)}\right|_{d=i_o=0}$$

$$= \frac{(1-D)R_L r_C}{L(R_L + r_C)}\,\frac{s + \dfrac{1}{Cr_C}}{s^2 + s\dfrac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{r + (1-D)^2 R_L}{LC(R_L + r_C)}}$$

$$= \frac{(1-D)R_L r_C}{L(R_L+r_C)} \frac{s+\omega_{zn}}{s^2+2\xi\omega_0 s+\omega_0^2} = M_{vx}\frac{s+\omega_{zn}}{s^2+2\xi\omega_0 s+\omega_0^2}$$

$$= \frac{(1-D)R_L r_C \omega_{zn}}{(R_L+r_C)L\omega_0^2} \frac{1+\dfrac{s}{\omega_{zn}}}{1+\dfrac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2} = M_{vo}\frac{1+\dfrac{s}{\omega_{zn}}}{1+\frac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2}. \tag{11.65}$$

Hence,

$$M_{vo} = M_v(0) = \frac{(1-D)R_L r_C \omega_{zn}}{(R_L+r_C)L\omega_0^2} = \frac{(1-D)R_L}{(1-D)^2+r} = \frac{1}{1-D}\ \frac{1}{1+\frac{r}{(1-D)^2R_L}}, \tag{11.66}$$

$$M_{vx} = \frac{(1-D)R_L r_C}{L(R_L+r_C)}, \tag{11.67}$$

and

$$M_v(\infty) = 0. \tag{11.68}$$

Notice that $M_{vo} \approx 1/(1-D)$ for $r/(1-D)^2 \ll R_L$ and is the same as the dc voltage transfer function M_{VDC} for the lossless boost converter.

For $s = j\omega$,

$$M_v(j\omega) = M_{vo}\frac{\left(1+j\dfrac{\omega}{\omega_{zn}}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2+j2\xi\left(\dfrac{\omega}{\omega_0}\right)} = |M_v|e^{j\phi_{Mv}}, \tag{11.69}$$

which gives

$$|M_v| = M_{vo}\sqrt{\frac{\left[1+\left(\dfrac{\omega}{\omega_{zn}}\right)^2\right]}{\left[1-\left(\dfrac{\omega}{\omega_0}\right)^2\right]^2+4\xi^2\left(\dfrac{\omega}{\omega_0}\right)^2}}. \tag{11.70}$$

Figure 11.14 shows idealized Bode plots of the open-loop input-to-output transfer function M_v for the boost converter. The slope pf the phase plot is $(-90^\circ/\xi)$/decade.

Example 11.3

A boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $r = 0.316\,\Omega$. Calculate M_{vo} at $R_{Lmin} = 40\,\Omega$ and draw the Bode plot of $|M_v|$ at $D = 0.5$.

Solution. From (11.66),

$$M_{vo} = M_v(0) = \frac{1}{1-D_{nom}}\ \frac{1}{1+\dfrac{r}{(1-D_{nom})^2R_{Lmin}}} = \frac{1}{1-0.5}\ \frac{1}{1+\dfrac{0.316}{(1-0.5)^2\times 40}}$$

$$= 1.939 = 5.75\,\text{dB}. \tag{11.71}$$

Figures 11.15 and 11.16 show the Bode plots of M_v. M_{vo} increases with increasing duty cycle D. In addition, $|M_v|$ decreases with increasing frequency above $f_0 = 783.66\,\text{Hz}$ at a

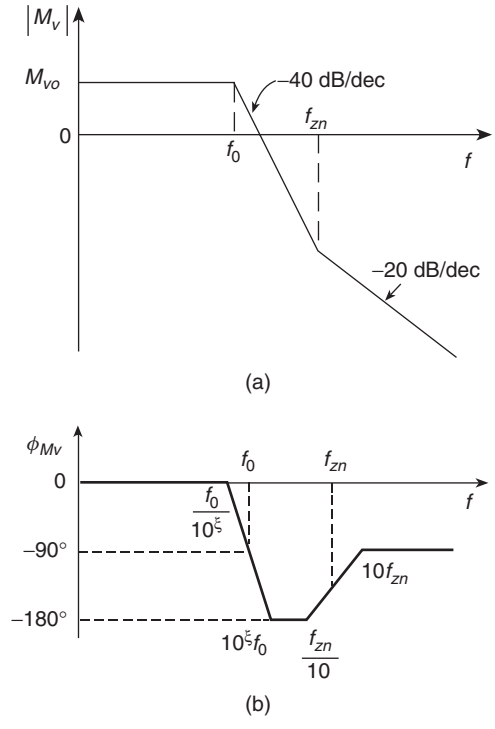


Figure 11.14 Idealized Bode plots of the open-loop input-to-output transfer function M_v for the boost converter in CCM. (a) $|M_v|$ versus f. (b) ϕ_{Mv} versus f.

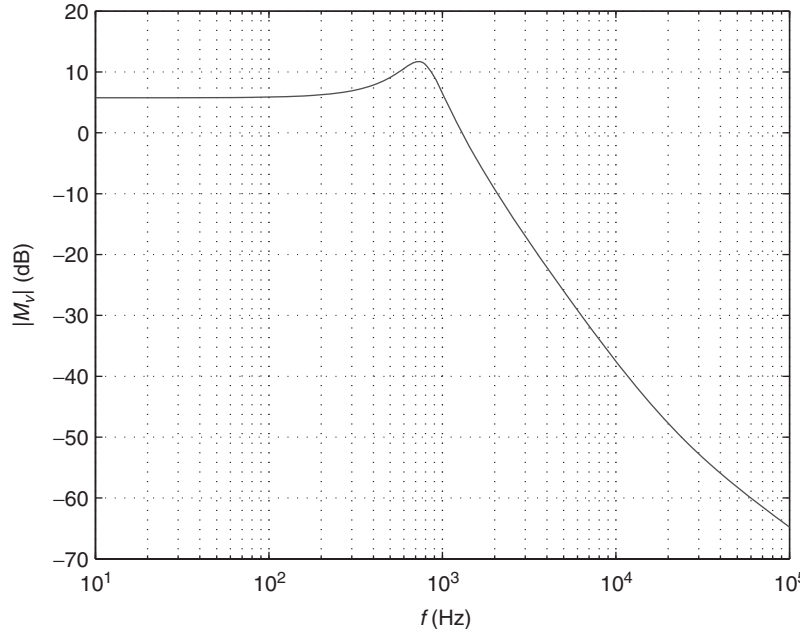


Figure 11.15 Bode plot of the magnitude of the open-loop input-to-output transfer function $|M_v|$ versus frequency for the boost converter.

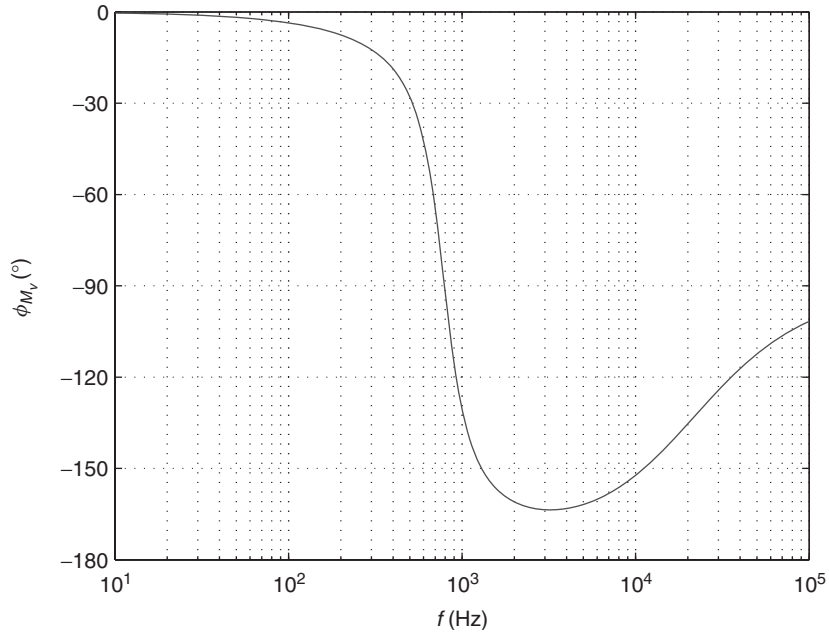


Figure 11.16 Bode plot of the phase of the open-loop input-to-output transfer function $|M_v|$ versus frequency for the boost converter.

rate of -40 dB/decade and above $f_{zn} = 21.09$ kHz at a rate of -20 dB/decade. The -3 dB bandwidth is $BW = 1$ kHz at $D = 0.5$.

11.6 Open-loop Input Impedance

The equivalent circuit of Figure 11.13 can be used to derive the open-loop small-signal input impedance of the boost converter. Note that $i_i = i_l$. Hence, by Kirchhoff's current law,

$$i_{Z_2} = i_i - Di_i = i_i(1 - D). \tag{11.72}$$

Therefore, the output voltage is

$$v_o = Z_2 i_{Z_2} = Z_2 i_i (1 - D). \tag{11.73}$$

Using Kirchhoff's voltage law,

$$v_i - i_i Z_1 + Dv_o - v_o = 0. \tag{11.74}$$

Substituting (11.73) into (11.74) yields

$$v_i = i_i[Z_1 + (1 - D)^2 Z_2]. \tag{11.75}$$

This yields the *open-loop input impedance*

$$Z_i(s) \equiv \left.\frac{v_i(s)}{i_i(s)}\right|_{d=i_o=0} = Z_1 + (1 - D)^2 Z_2 = (r + sL) + \frac{(1 - D)^2 R_L \left(r_C + \dfrac{1}{sC}\right)}{R_L + r_C + \dfrac{1}{sC}}. \tag{11.76}$$

Rearrangement of this equation produces

$$Z_i(s) = \frac{L\left\{s^2 + s\dfrac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{(1-D)^2 R_L + r}{LC(R_L + r_C)}\right\}}{s + \dfrac{1}{C(R_L + r_C)}}$$

$$= \frac{L(s^2 + 2\xi\omega_0 s + \omega_0^2)}{s + \omega_{rc}}, \tag{11.77}$$

where

$$\omega_{rc} = \frac{1}{C(R_L + r_C)}. \tag{11.78}$$

From (11.77),

$$R_i(0) = Z_i(0) = (1-D)^2 R_L + r \tag{11.79}$$

and

$$Z_i(\infty) = \infty. \tag{11.80}$$

Example 11.4

For the boost converter with $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$, and $r = 0.316\,\Omega$, calculate f_{rc} and $R_i(0)$ at $R_{Lmin} = 40\,\Omega$. Draw the plots of Z_i at $D = 0.5$.

Solution. Using (11.78),

$$f_{rc} = \frac{1}{2\pi C(R_{Lmin} + r_C)} = \frac{1}{2 \times \pi \times 68 \times 10^{-6} \times (40 + 0.111)} = 58.38\,\text{Hz}. \tag{11.81}$$

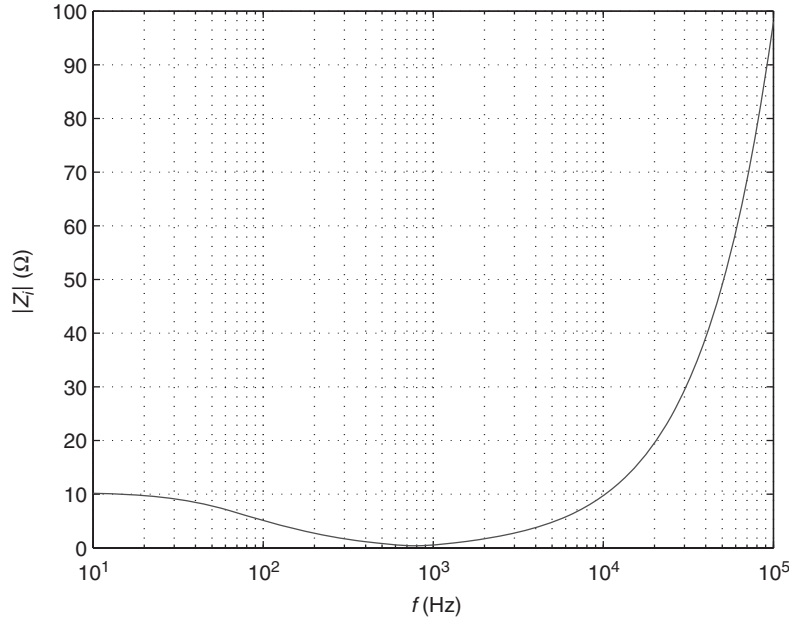


Figure 11.17 The magnitude of the open-loop input impedance Z_i for the boost converter.

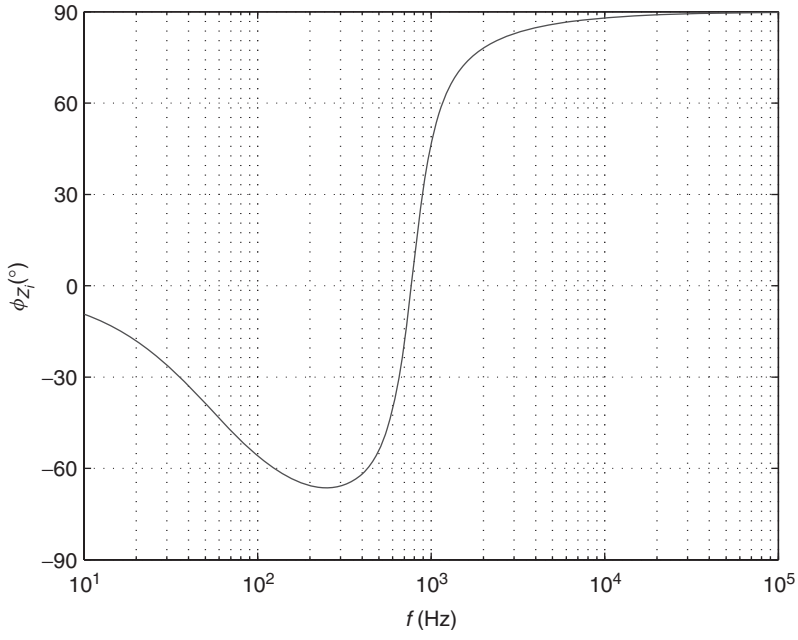


Figure 11.18 The phase of the open-loop input impedance Z_i for the boost converter.

From (11.79),

$$R_i(0) = Z_i(0) = (1 - D_{nom})^2 R_{Lmin} + r = (1 - 0.5)^2 \times 40 + 0.316 = 10.316\,\Omega. \quad (11.82)$$

Figures 11.17 and 11.18 show the plots of Z_i versus frequency. These plots are similar to those of a series resonant circuit. It can be seen that $|Z_i|$ decreases with increasing D and rapidly increases with frequency above 1 kHz.

11.7 Open-loop Output Impedance

A small-signal model of the boost converter for deriving the open-loop output impedance is shown in Figure 11.19. This model is obtained by reducing d, v_i, and i_o to zero and applying an independent voltage source v_t at the output of the model. The voltage source v_t will force a current i_t. The open-loop output impedance is equal to the ratio of the voltage v and the current i_t. By Kirchhoff's voltage law,

$$v_t - Dv_t - i_l Z_1 = 0, \quad (11.83)$$

which gives

$$i_l = -\frac{v_t(1 - D)}{Z_1}. \quad (11.84)$$

By Kirchhoff's current law,

$$i_b = Di_l - i_l = -i_l(1 - D) = \frac{(1 - D)^2 v_t}{Z_1} \quad (11.85)$$

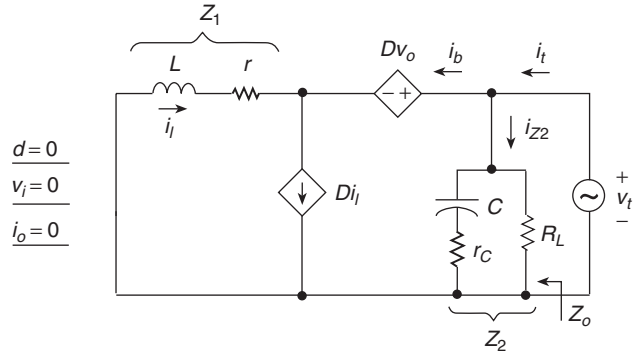


Figure 11.19 Small-signal model of the PWM boost converter for determining the output impedance Z_o.

and

$$i_t = i_{Z_2} + i_b = \frac{v}{Z_2} + \frac{(1-D)^2 v_t}{Z_1} = v_t \left[\frac{1}{Z_2} + \frac{(1-D)^2}{Z_1} \right]. \tag{11.86}$$

Hence, the *open-loop output impedance* (including the load resistance R_L) is

$$\begin{aligned} Z_o(s) \equiv \left. \frac{v_t(s)}{i_t(s)} \right|_{d=v_i=i_o=0} &= \frac{1}{\dfrac{1}{Z_2} + \dfrac{(1-D)^2}{Z_1}} = \frac{Z_1}{(1-D)^2} \parallel Z_2 \\ &= \frac{r + sL}{(1-D)^2} \parallel \frac{R_L \left(r_C + \dfrac{1}{sC} \right)}{R_L + r_C + \dfrac{1}{sC}}. \end{aligned} \tag{11.87}$$

Thus,

$$\begin{aligned} Z_o(s) &= \frac{R_L r_C}{R_L + r_C} \, \frac{\left(s + \dfrac{1}{Cr_C} \right) \left(s + \dfrac{r}{L} \right)}{s^2 + s \dfrac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{r + (1-D)^2 R_L}{LC(R_L + r_C)}} \\ &= \frac{R_L r_C}{R_L + r_C} \, \frac{(s + \omega_{zn})(s + \omega_{rl})}{s^2 + 2\xi\omega_0 s + \omega_0^2}, \end{aligned} \tag{11.88}$$

where

$$\omega_{rl} = \frac{r}{L}. \tag{11.89}$$

From (11.88),

$$R_o(0) = Z_o(0) = R_L \parallel \frac{r}{(1-D)^2} = \frac{rR_L}{r + (1-D)^2 R_L} \tag{11.90}$$

and

$$Z_o(\infty) = \frac{R_L r_C}{R_L + r_C} \approx r_C, \qquad \text{for } r_C \ll R_L. \tag{11.91}$$

Example 11.5

For the boost converter with $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $r = 0.316\,\Omega$, calculate f_{rl} and $Z_o(0)$ at $R_{Lmin} = 40\,\Omega$. Draw the plots of Z_o at $D = 0.5$.

Solution. From (11.89),

$$f_{rl} = \frac{r}{2\pi L} = \frac{0.316}{2 \times \pi \times 156 \times 10^{-6}} = 322.55\,\text{Hz}. \tag{11.92}$$

From (11.90),

$$Z_{oo} = R_o(0) = Z_o(0) = \frac{rR_{Lmin}}{r + (1 - D_{nom})^2 R_{Lmin}} = \frac{0.316 \times 40}{0.316 + (1 - 0.5)^2 \times 40} = 1.225\,\Omega. \tag{11.93}$$

Figures 11.20 and 11.21 show the plots of the output impedance Z_o versus frequency. These plots of Z_o are similar to those of a parallel resonant circuit. $|Z_o|$ increases with increasing f at low frequencies, assumes a maximum value of about $6.2\,\Omega$ (at $f_0 = 783.66\,\text{Hz}$), and then decreases with increasing f. The magnitude $|Z_o|$ increases with D at low frequencies because $r/(1 - D)^2$ increases with D.

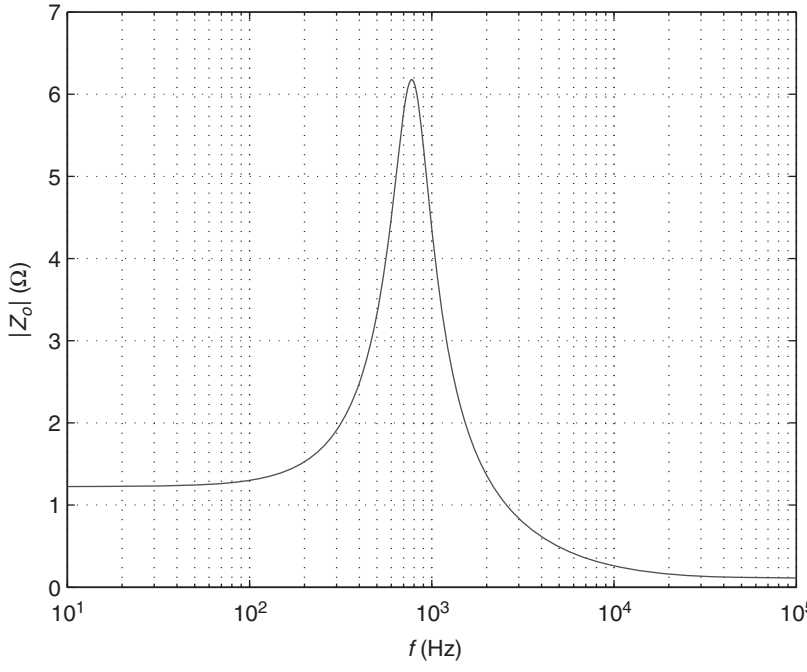


Figure 11.20 The magnitude of the open-loop output impedance Z_o for the boost converter.

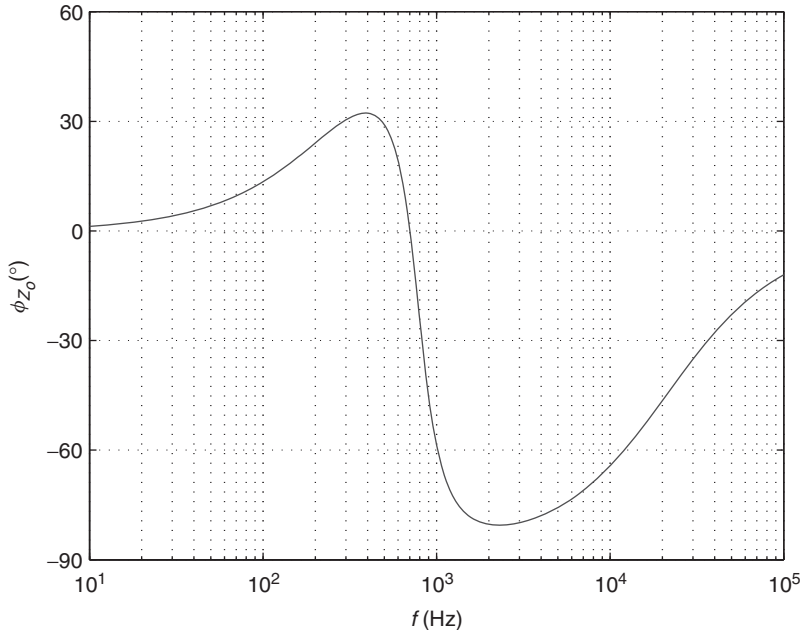


Figure 11.21 The phase of the open-loop output impedance Z_o for the boost converter.

11.8 Open-loop Step Responses

11.8.1 Open-loop Response of Output Voltage to Step Change in Input Voltage

Let us consider a step change in the input voltage of magnitude ΔV_I at time $t = 0$. The total input voltage is given by

$$v_I(t) = V_I(0^-) + \Delta V_I u(t), \tag{11.94}$$

where $u(t)$ is the unit step function and $V_I(0^-)$ is the steady-state input voltage before the step change. The step change of the input voltage in the time domain is expressed by

$$v_i(t) = v_I(t) - V_I(0^-) = \Delta V_I u(t), \tag{11.95}$$

which gives the step change of the input voltage in the s-domain,

$$v_i(s) = \frac{\Delta V_I}{s}. \tag{11.96}$$

Hence, from (11.65) and (11.96), the transient component of the output voltage of the open-loop boost converter in the s-domain is given by

$$v_o(s) = M_v(s)v_i(s) = \frac{\Delta V_I M_v(s)}{s} = \Delta V_I M_{vo} \frac{\omega_0^2}{\omega_{zn}} \frac{s + \omega_{zn}}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}. \tag{11.97}$$

This produces the transient component of the output voltage of the open-loop boost converter in the time domain,

$$v_o(t) = \mathcal{L}^{-1}\{v_o(s)\} = \Delta V_I M_{vo}\left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zn}} + \left(\frac{\omega_0}{\omega_{zn}}\right)^2}\,\frac{e^{-\xi\omega_0 t}}{\sqrt{1-\xi^2}}\sin(\omega_d t + \phi)\right], \tag{11.98}$$

where

$$\phi = \pi + \arctan\left[\frac{\sqrt{1-\xi^2}}{\left(\frac{\omega_{zn}}{\omega_0} - \xi\right)}\right] + \arctan\left(\frac{\sqrt{1-\xi^2}}{\xi}\right), \quad \text{for } \frac{\omega_{zn}}{\omega_0} \geq \xi, \tag{11.99}$$

or

$$\phi = 2\pi + \arctan\left[\frac{\sqrt{1-\xi^2}}{\left(\frac{\omega_{zn}}{\omega_0} - \xi\right)}\right] + \arctan\left(\frac{\sqrt{1-\xi^2}}{\xi}\right), \quad \text{for } \frac{\omega_{zn}}{\omega_0} < \xi. \tag{11.100}$$

Hence, the total output voltage is

$$v_O(t) = V_O(0^-) + v_o(t), \qquad \text{for } t \geq 0, \tag{11.101}$$

where $V_O(0^-)$ is the output voltage at time $t = 0^-$.

Setting the derivative of (11.98) to zero, one obtains the time instants at which the maximum and minimum values of v_o occur,

$$\omega_0 t_m = \frac{n\pi}{\sqrt{1-\xi^2}}, \tag{11.102}$$

where n is an integer. The first maximum value of v_o is the highest one and occurs for $n = 1$. The highest maximum value of v_o is given by

$$v_{omax} = \Delta V_I M_{vo}\left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zn}} + \left(\frac{\omega_0}{\omega_{zn}}\right)^2}\,e^{-\pi\xi/\sqrt{1-\xi^2}}\right], \tag{11.103}$$

resulting in the *maximum overshoot* of the transient component of the output voltage v_o,

$$\begin{aligned} S_{max} &\equiv \frac{v_{omax} - v_o(\infty)}{v_o(\infty)} = \frac{v_{omax}}{v_o(\infty)} - 1 = \frac{v_{omax}}{\Delta V_I M_{vo}} - 1 \\ &= \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zn}} + \left(\frac{\omega_0}{\omega_{zn}}\right)^2}\,e^{-\pi\xi/\sqrt{1-\xi^2}}, \end{aligned} \tag{11.104}$$

where $v_o(\infty) = \Delta V_I M_{vo}$ is the steady-state value of the transient component of the output voltage v_o after the transition.

The *maximum relative transient ripple* of the total output voltage is defined as

$$\delta_{max} \equiv \frac{v_{omax} - v_o(\infty)}{v_O(\infty)} = \frac{v_{Omax} - v_O(\infty)}{v_O(\infty)}, \tag{11.105}$$

where $v_O(\infty) = V_O(0^-) + v_o(\infty)$ is the steady-state value of the total output voltage after the transition.

Example 11.6

For the open-loop boost converter specified in Example 11.1, draw the waveform of the output voltage v_O that is a response to the step change in the input voltage from 12 to 13 V. Calculate (a) the maximum overshoot of the transient component of the output voltage, (b) the steady-state values of the transient component and the total output voltage, (c) the maximum relative transient ripple of the total output voltage.

Solution. Figure 11.22 shows the step response of the transient component of the output voltage v_o to a step change in the input voltage v_I from 12 to 13 V, which corresponds to a step change in v_i from 0 to 1 V, for the boost converter without feedback at $D_{nom} = 0.5$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$. The output voltage increases from 20 V to its peak value of 22.738 V and then reaches its steady-state value of $v_O = 21.939$ V after approximately 3 ms.

From Examples 11.1 and 11.3, $\xi = 0.261$, $f_{zn} = 21.09$ kHz, $f_0 = 783.66$ Hz, and $M_{vo} = 1.939$. The steady-state value of the transient component of the output voltage is

$$v_o(\infty) = M_{vo}\Delta V_I = 1.939 \times 1 = 1.939\,\text{V}. \tag{11.106}$$

Using (11.104), one can compute the maximum overshoot of the transient component of the output voltage v_o,

$$S_{max} = \sqrt{1 - \frac{2\xi f_0}{f_{zn}} + \left(\frac{f_0}{f_{zn}}\right)^2} e^{-\pi\xi/\sqrt{1-\xi^2}}$$

$$= \sqrt{1 - \frac{2 \times 0.261 \times 0.784}{21.09} + \left(\frac{0.784}{21.09}\right)^2} e^{-\pi \times 0.261/\sqrt{1-0.261^2}} = 42.39\,\%. \tag{11.107}$$

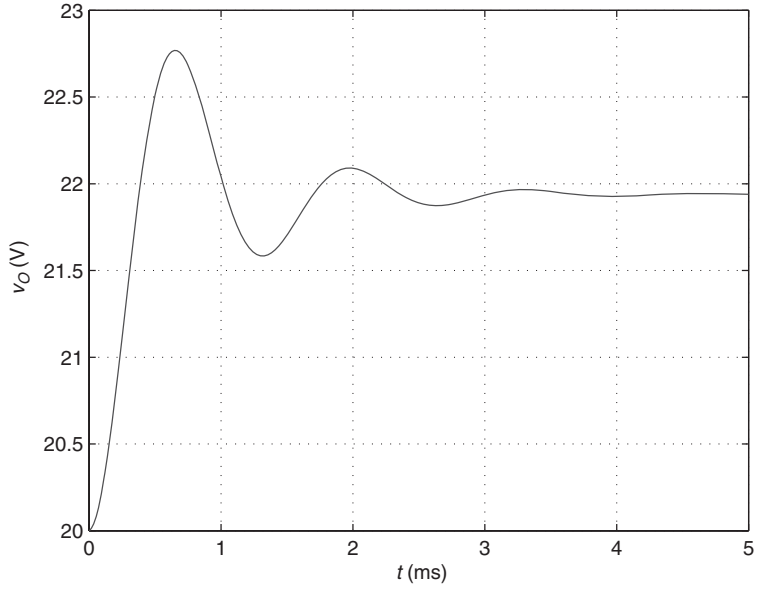


Figure 11.22 Response of the output voltage v_O to a step change in v_I from 12 to 13 V for the boost converter without feedback for $D_{nom} = 0.5$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$.

Hence, the maximum value of the transient component of the output voltage is

$$v_{omax} = (1 + S_{max})v_o(\infty) = (1 + 0.4239) \times 1.939 = 2.761\,\text{V}. \tag{11.108}$$

The steady-state value of the total output voltage is

$$v_O(\infty) = V_O(0^-) + v_o(\infty) = 20 + 1.939 = 21.939\,\text{V}. \tag{11.109}$$

Thus, the maximum relative transient ripple of the output voltage is

$$\delta_{max} = \frac{v_{omax} - v_o(\infty)}{v_O(\infty)} = \frac{2.761 - 1.939}{21.939} = \frac{0.822}{21.939} = 3.75\,\%. \tag{11.110}$$

11.8.2 Open-loop Response of Output Voltage to Step Change in Duty Cycle

Assume a step change in the duty cycle Δd_T at time $t = 0$. The total duty cycle is

$$d_T(t) = D + \Delta d_T u(t). \tag{11.111}$$

The step change in the duty cycle in the time domain is given by

$$d(t) = d_T(t) - D = \Delta d_T u(t), \tag{11.112}$$

which results in

$$d(s) = \frac{\Delta d_T}{s}. \tag{11.113}$$

Hence, using (11.22), the transient component of the output voltage of the open-loop boost converter in the s-domain is

$$v_o(s) = T_p(s)d(s) = \frac{\Delta d_T T_p(s)}{s} = -\Delta d_T T_{po} \frac{\omega_0^2}{\omega_{zn}\omega_{zp}} \frac{(s + \omega_{zn})(s - \omega_{zp})}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}. \tag{11.114}$$

The inverse Laplace transform of the output voltage of the open-loop boost converter in the time domain can be found using MATLAB.

Example 11.7

For the open-loop boost converter specified in Example 11.1, draw the waveform of the output voltage v_O that is the response to a step change in the duty cycle d_T from 0.5 to 0.6. Calculate the output voltage for the steady state after the transition and the maximum relative transient ripple.

Solution. Figure 11.23 shows the response of the transient component of the output voltage v_o to a step change in the control input d_T from 0.5 to 0.6 for $d = 0.1$ for the boost converter without feedback at $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$. The output voltage v_O increases from 20 V to a peak value of 25.35 V and then reaches a steady-state value of approximately 23.755 V after 3 ms.

From Example 11.2, the transient component of the output voltage is

$$v_o(\infty) = T_{po}\Delta d_T = 37.55 \times 0.1 = 3.755\,\text{V}. \tag{11.115}$$

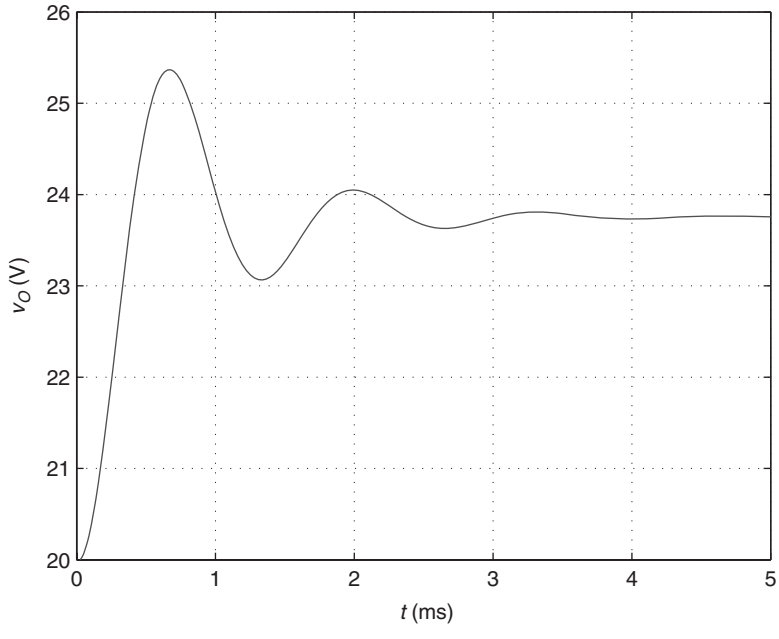


Figure 11.23 Response of the output voltage v_O to a step change in the duty cycle d_T from 0.4 to 0.5 for the boost converter without feedback for $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.4\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$.

Referring to Figure 11.23, $v_{omax} = 5.35\,\text{V}$ and the maximum overshoot is

$$S_{max} \equiv \frac{v_{omax} - v_o(\infty)}{v_o(\infty)} = \frac{5.35 - 3.755}{3.755} = 42.48\,\%. \tag{11.116}$$

The total output voltage is

$$v_O(\infty) = V_O(0^-) + v_o(\infty) = 20 + 3.755 = 23.755\,\text{V}. \tag{11.117}$$

Hence, the maximum relative transient ripple of the output voltage is

$$\delta_{max} = \frac{v_{Omax} - v_O(\infty)}{v_O(\infty)} = \frac{25.35 - 23.755}{23.755} = 6.71\,\%. \tag{11.118}$$

11.8.3 Open-loop Response of Output Voltage to Step Change in Load Current

Let us assume a step change in the load current ΔI_O at time $t = 0$ for fixed input voltage V_I and duty cycle D. The total load current is given by

$$i_O(t) = I_O(0^-) + \Delta I_O u(t), \tag{11.119}$$

resulting in the step change in the load current in the time domain,

$$i_o(t) = i_O(t) - I_O(0^-) = \Delta I_O u(t), \tag{11.120}$$

and in the s-domain,

$$i_o(s) = \frac{\Delta I_O}{s}. \tag{11.121}$$

This leads to the transient component of the output voltage in the s-domain,

$$v_o(s) = -Z_o(s) i_o(s) = -\frac{\Delta I_O R_L r_C}{R_L + r_C} \frac{(s + \omega_{zn})}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}, \tag{11.122}$$

and in the time domain,

$$v_o(t) = \mathcal{L}^{-1}\{v_o(s)\}. \tag{11.123}$$

The total output voltage is $v_O = V(0^-) + v_O(t)$.

Example 11.8

For the open-loop boost converter given in Example 11.1, draw the waveform of the output voltage v_O that is the response to the step change in the load current i_O from 0.5 to 0.6 A. Find the output voltage for the steady state after the transition and the maximum relative transient ripple.

Solution. Figure 11.24 shows the step response of the output voltage v_O to a step change in the load current i_O from 0.5 to 0.6 A for the buck converter without feedback at $V_I = 28\,\text{V}$, $D = 0.5$, $L = 156\,\mu\text{H}$, $C = 68\,\mu\text{F}$, $R_{Lmin} = 40\,\Omega$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$.

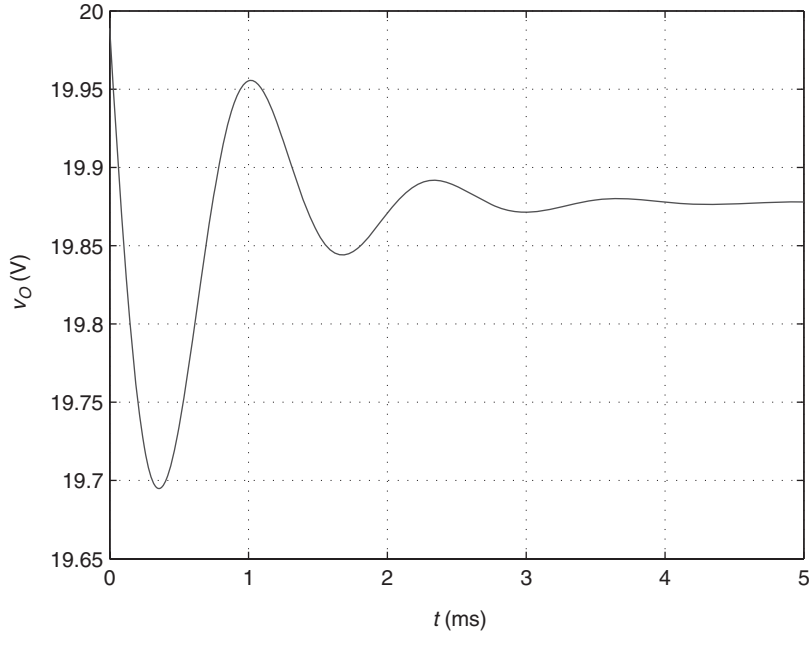


Figure 11.24 Step response of v_O to a step change in the load current I_O from 0.5 to 0.6 A for the boost converter without feedback for $V_{Inom} = 12\,\text{V}$, $D = 0.5$, $L = 156\,\mu\text{H}$, $C = 68\,\mu\text{F}$, $R_{Lmin} = 40\,\Omega$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$.

The output voltage v_O decreases from 20 V to a minimum value of 19.69 V and then reaches a steady-state value of approximately 19.9 V after 3 ms. The dc output resistance is $Z_o(0) = R_o(0) = R_{Lmin}r/[(1 - D_{nom})^2 R_{Lmin} + r] = 1.225\,\Omega$. The change in the steady-state output voltage is

$$v_o(\infty) = \Delta V_O = -Z_o(0)\Delta I_O = -1.225 \times 0.1 = -0.1225\,\text{V}. \tag{11.124}$$

Hence, the output voltage after the transition is

$$v_O(\infty) = V_O(0^-) + v_o(\infty) = 20 - 0.1225 = 19.8775\,\text{V}. \tag{11.125}$$

From Figure 11.24, $v_{omin} = -0.3051$ V, yielding the maximum undershoot of the output voltage

$$S_{max} = \frac{|v_{omin}| - |v_o(\infty)|}{|v_o(\infty)|} = \frac{0.3051 - 0.1221}{0.1221} = 150\,\%, \tag{11.126}$$

and the maximum relative transient ripple of the output voltage,

$$\delta_{max} = \frac{|v_{omin}| - |v_o(\infty)|}{v_O(\infty)} = \frac{0.3051 - 0.1221}{19.8775} = 0.92\,\%. \tag{11.127}$$

11.9 Summary

- The small-signal model of the boost converter has two inputs: the small-signal duty cycle d and the small-signal input voltage v_i. The small-signal duty cycle d is a control variable and the small-signal input voltage v_i is a disturbance.
- The small-signal model of the boost converter has one output, which is the small-signal component of the output voltage v_o.
- The open-loop control-to-output transfer function of the boost converter is a second-order low-pass function with two poles and two zeros.
- The two poles and one zero are located in the left-half plane and one zero is located in the right-half plane for most values of the dc duty cycle D. As D is increased from 0 to 1, the zero moves from the right-half plane to the origin and enters the left-half plane as D approaches 1.
- The open-loop input-to-output transfer function of the boost converter is a second-order low-pass transfer function.
- The open-loop input-to-output transfer function of the boost converter has two simple or complex poles and one simple zero.
- Both poles and the zero of the open-loop input-to-output transfer function of the boost converter are located in the left-half plane.
- The plots of the open-loop input impedance of the boost converter are similar to those of the series resonant circuit composed of a series combination of $L/(1 - D)^2$ and $r/(1 - D)^2$ in series with the $C - r_C - R_L$ circuit.
- The plots of the open-loop output impedance of the boost converter are similar to those of the parallel resonant circuit composed of a series combination of $L/(1 - D)^2$ and $r/(1 - D)^2$ in parallel with the $C - r_C - R_L$ circuit.

- The magnitude of the output impedance $|Z_o|$ increases with increasing D at low frequencies.

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11.11 Review Questions

11.1 Draw a dc model for a boost converter for CCM.

11.2 Draw a small-signal model for a boost converter for CCM.

11.3 Draw a small-signal model to derive the control-to-output transfer function of a boost converter for CCM.

11.4 What is the order of the control-to-output transfer function of the boost converter?

11.5 Where are the poles and zeros of the control-to-output transfer function of the boost converter located in the s-plane?

11.6 How does the location of the poles and zeros of the control-to-output transfer function change with increasing dc duty cycle D?

11.7 What is a nonminimal phase system?

11.8 Is the control-to-output transfer function of the boost converter minimal or nonminimal phase?

11.9 Sketch Bode plots for the control-to-output transfer function of the boost converter.

11.10 Draw a small-signal model for deriving the input-to-output transfer function of a boost converter.

11.11 Sketch the magnitude of the input-to-output transfer function for the boost converter.

11.12 Where are the poles and the zero of the input-to-output transfer function of the boost converter located in the s-plane?

11.13 Draw a small-signal model to derive the input impedance of a boost converter.

11.14 Sketch the magnitude and phase of input impedance for the boost converter.

11.15 Draw a small-signal model to derive the output impedance of a boost converter.

11.16 Sketch the magnitude and phase of the output impedance for the boost converter.

11.12 Problems

11.1 The boost converter designed in Chapter 3 has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $V_F = 1.4\,\text{V}$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, and $r_C = 1\,\Omega$. Determine M_{VDC} and η.

11.2 The boost converter has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Calculate z_n, f_{zn}, z_p, f_{zp}, f_0, ξ, Q, p_1, p_2, and f_d.

11.3 The boost converter has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine T_{po} and $T_p(\infty)$.

11.4 The boost converter has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine M_{vo}.

11.5 The boost converter has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\mu\text{H}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine $Z_i(0)$.

11.6 The boost converter has $V_{Inom} = 28\,\text{V}$, $V_O = -12\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine $Z_o(0)$ and $Z_o(\infty)$.

11.7 The boost converter has $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine $Z_o(0)$ for $D = 0.1$, 0.5, 0.8, and 0.9.

11.8 The boost converter has $\xi_{lossy} = 0.162$, $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, $r = 2.756\,\Omega$, and $r_C = 1\,\Omega$. Determine ξ and Q at all parasitic resistances equal to zero. Calculate the ratio of the actual to approximate values of ξ.

12

Voltage-mode Control of Boost Converter

12.1 Introduction

The objective of this chapter is to present a small-signal analysis of a closed-loop voltage-mode-controlled PWM boost dc–dc converter with an integral-lead controller, also called an integral-double-lead controller. The circuit of the controller is analyzed. Its design procedure is developed. Loop gain, closed-loop transfer functions, and input and output impedances are found. In addition, step responses are computed for changes in the input voltage and the reference voltage. A design example is given. The closed-loop boost converter has been studied in [1]–[13].

12.2 Circuit of Boost Converter with Voltage-mode Control

A boost converter and a single-loop control circuit is shown in Figure 12.1. This circuit has a series-shunt negative feedback topology. The duty cycle is directly controlled by a voltage derived from the reference voltage V_R and the feedback voltage v_F. This method of control is called voltage-mode control.

The feedback network can be represented by h-parameters as shown in Figure 12.2. The resistances $h_{11} = R_A R_B/(R_A + R_B)$ and $1/h_{22} = R_A + R_B$ can be moved from the feedback network to the A-circuit [13] as shown in Figure 12.3. Since usually $1/h_{22} \gg R_L$, it can be neglected.

Figure 12.4(a) shows a small-signal model of the boost converter and various stages related to the control of the output voltage. A block diagram of a closed-loop voltage-mode-controlled boost converter is shown in Figure 12.4(b). In this figure, T_p is the small-signal control-to-output transfer function of the power stage of the boost converter, M_v is the

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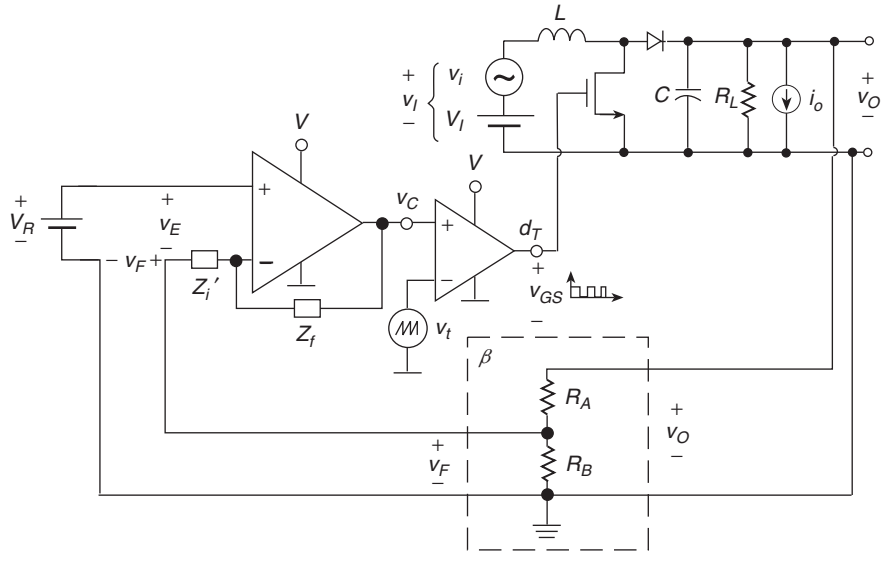


Figure 12.1 Boost PWM converter with voltage-mode control.

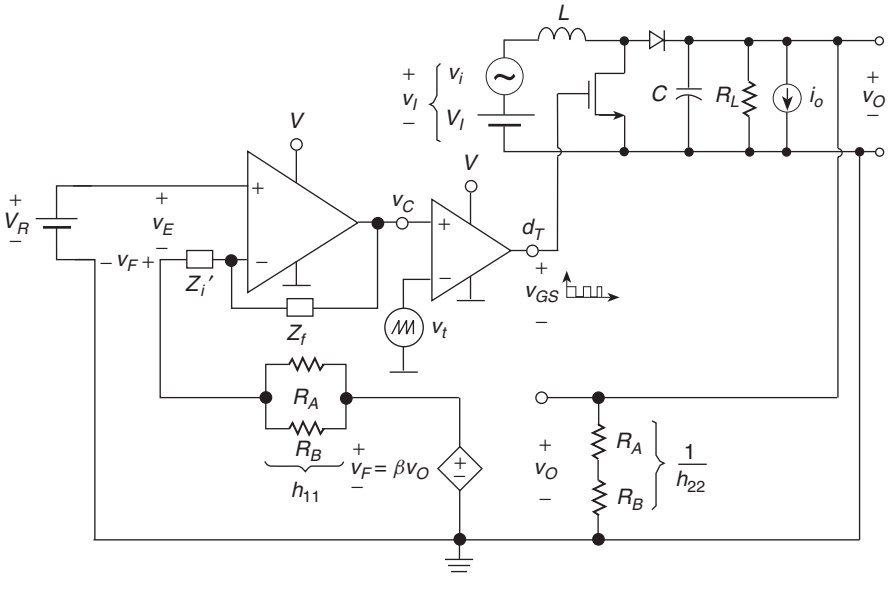


Figure 12.2 Closed-loop boost PWM converter with a feedback network β represented by h-parameters.

input-to-output voltage transfer function, Z_o is the open-loop output impedance, T_m is the transfer function of the pulse-width modulator, T_c is the voltage transfer function of the controller, β is the transfer function of the feedback network, v_f is the ac component of the feedback voltage, v_c is the ac component of the output voltage of the controller, v_e is the ac component of the error voltage, and v_r is the ac component of the reference voltage. The control block diagram is a three-input and single-output system driven by

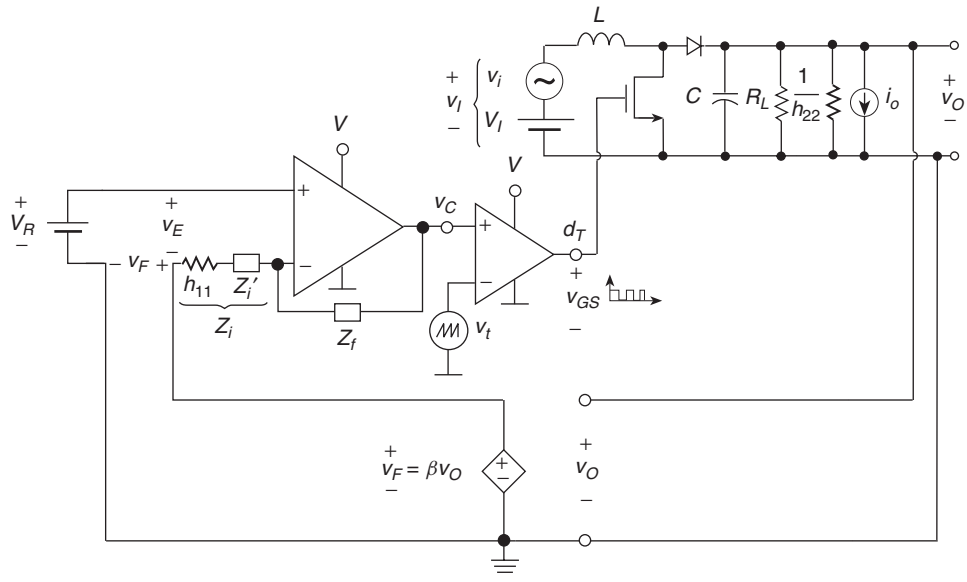


Figure 12.3 Closed-loop boost PWM converter with resistances h_{11} and $1/h_{22}$ moved to the A-network.

three independent sources, v_r, v_i, and i_o. The ac component of the input voltage v_i can be viewed as a disturbance caused by a low-frequency ripple voltage and/or variations of the line voltage. For a constant dc output voltage, $v_r = 0$. The voltage gain of the forward path for the ac components is

$$A \equiv \frac{v_o}{v_e} = T_c T_m T_p, \tag{12.1}$$

and the loop gain is

$$T \equiv \frac{v_o}{v_f} = \beta A = \beta T_c T_m T_p. \tag{12.2}$$

The ac component of the output voltage is given by

$$v_o = \frac{A}{1+T}\, v_r + \frac{M_v}{1+T}\, v_i - \frac{Z_o}{1+T} = T_{cl} v_r + M_{vcl} v_i - Z_{ocl} i_o. \tag{12.3}$$

Using this equation, the block diagram of Figure 12.4(b) can be simplified to the form shown in Figure 12.4(c).

12.3 Pulse-width Modulator

A circuit of a pulse-width modulator is shown in Figure 12.5(a). It is an inverting comparator based on an open-loop op-amp. The control voltage is applied to the noninverting input, and the ramp voltage v_t is applied to the inverting input. Waveforms of the control voltage v_C and the ramp voltage v_t in the pulse-width modulator are shown in Figure 12.6. As the control voltage is increased from V_C to $V_C + v_c$, the duty cycle is increased from D to $D + d$, causing an increase in the converter output voltage. From Figure 12.6, the slope of the ramp voltage waveform v_t can be expressed in terms of the dc components of the

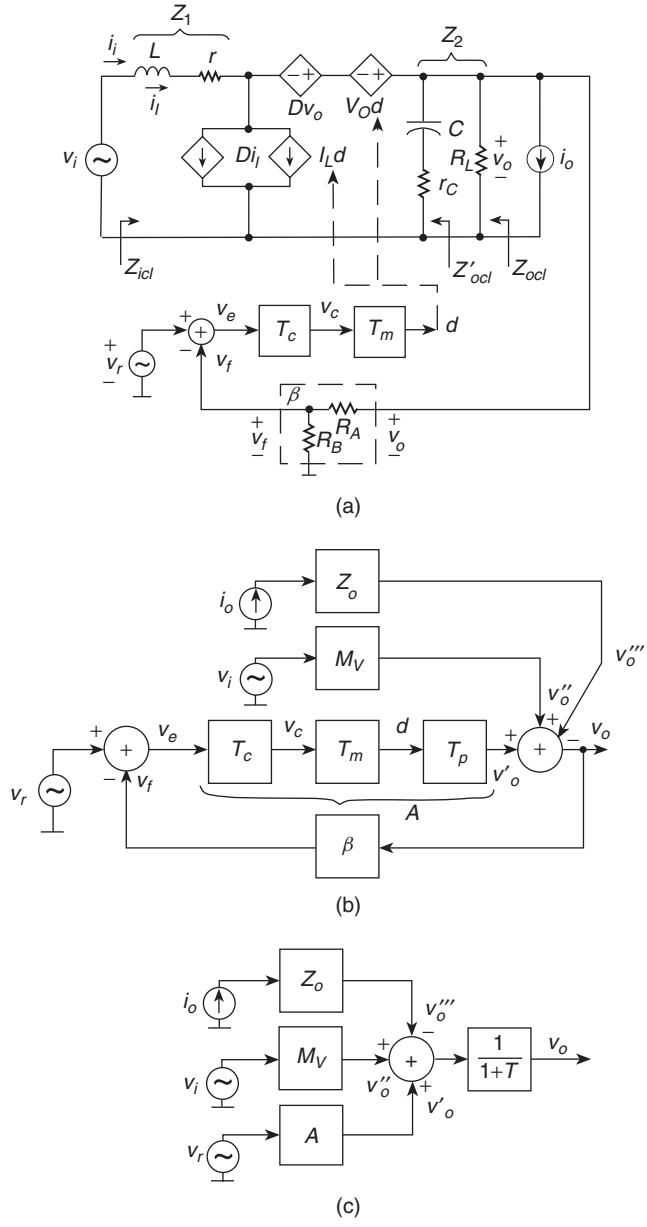


Figure 12.4 Closed-loop small-signal low-frequency model of the boost converter. (a) Small-signal model. (b) Block diagram. (c) Simplified block diagram.

control voltage V_C and the duty cycle D,

$$M = \tan\gamma = \frac{V_C}{DT_s} = \frac{V_{Tm}}{T_s}. \tag{12.4}$$

Hence, the *dc control voltage-to-duty cycle transfer function* of the pulse-width modulator is

$$T_{m(dc)} \equiv \frac{D}{V_C} = \frac{1}{V_{Tm}} = \frac{1}{MT_s} = \frac{f_s}{M}. \tag{12.5}$$

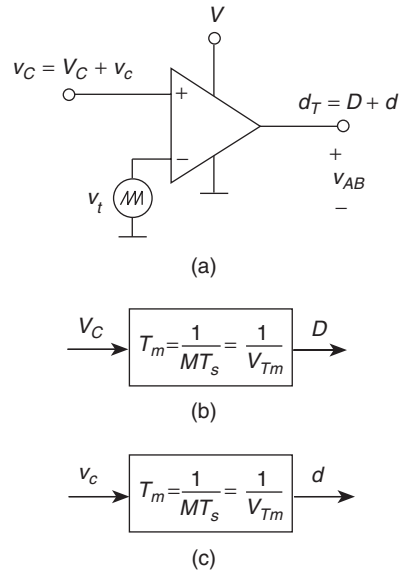


Figure 12.5 Pulse-width modulator. (a) Circuit. (b) DC block diagram. (c) AC small-signal block diagram.

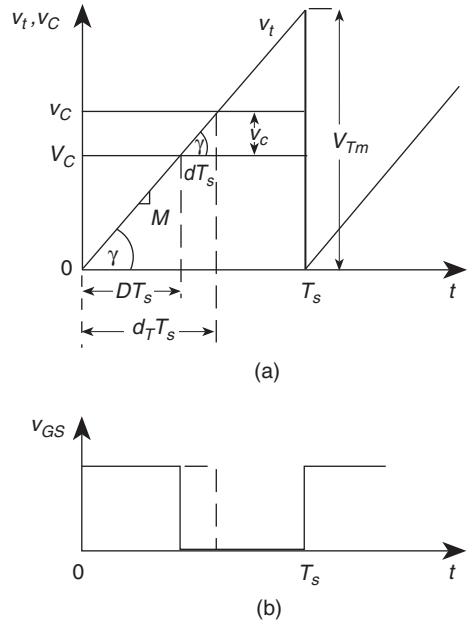


Figure 12.6 Waveforms in the pulse-width modulator. (a) Waveforms of the sawtooth voltage v_t and the control voltage v_C. (b) Waveforms of the gate-to-source voltage v_{GS}.

Using Figure 12.6(a), the slope of the ramp voltage v_t can be described in terms of the small-signal components of the control voltage v_c and the duty cycle d,

$$M = \tan\gamma = \frac{v_c}{dT_s} = \frac{V_{Tm}}{T_s}. \tag{12.6}$$

Rearrangement of this equation leads to the *ac control voltage-to-duty cycle transfer function* of the pulse-width modulator,

$$T_{m(ac)} \equiv \frac{d}{v_c} = \frac{1}{V_{Tm}} = \frac{1}{MT_s} = \frac{f_s}{M}. \tag{12.7}$$

Note that $T_{m(dc)} = T_{m(ac)} = T_m$.

12.4 Transfer Function of Modulator, Boost Converter Power Stage, and Feedback Network

The transfer function of the pulse-width modulator and the boost converter power stage is

$$\begin{aligned}
T_{mp}(s) &\equiv \frac{v_o(s)}{v_c(s)}|_{v_i=i_o=0} = T_m T_p(s) = \frac{T_p(s)}{V_{Tm}} \\
&= -\frac{V_O r_C}{V_{Tm}(1-D)(R_L+r_C)} \frac{\left(s+\dfrac{1}{Cr_C}\right)\left\{s-\dfrac{1}{L}[(1-D)^2R_L-r]\right\}}{s^2+s\dfrac{C[r(R_L+r_C)+(1-D)^2R_Lr_C]+L}{LC(R_L+r_C)} + \dfrac{r+(1-D)^2R_L}{LC(R_L+r_C)}} \\
&= -\frac{V_O r_C}{V_{Tm}(1-D)(R_L+r_C)} \frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2} \\
&= \frac{V_O r_C \omega_{zn}\omega_{zp}}{V_{Tm}(1-D)(R_L+r_C)\omega_0^2} \frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{1+\dfrac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2} \\
&= T_{mpo}\frac{\left(1+\dfrac{s}{\omega_{zn}}\right)\left(1-\dfrac{s}{\omega_{zp}}\right)}{1+\dfrac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2},
\end{aligned} \tag{12.8}$$

where

$$T_{mpo} = T_{mp}(0) = \frac{V_O r_C \omega_{zn}\omega_{zp}}{V_{Tm}(1-D)(R_L+r_C)\omega_0^2} = \frac{V_O}{V_{Tm}(1-D)} \frac{(1-D)^2R_L-r}{(1-D)^2R_L+r}. \tag{12.9}$$

Example 12.1

A boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $V_{Tm} = 5\,\text{V}$. Calculate T_{mpo} and draw Bode plots of T_{mp} for $D = 0.5$.

Solution. The transfer function of the pulse-width modulator is

$$T_m = \frac{1}{V_{Tm}} = \frac{1}{5}\,\frac{1}{\text{V}} = -14\,\frac{\text{dB}}{\text{V}}. \tag{12.10}$$

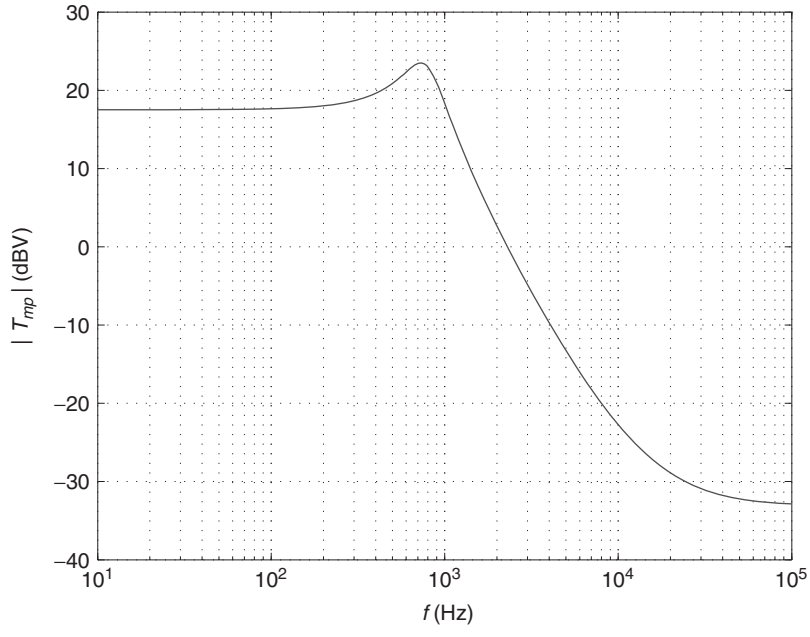


Figure 12.7 Bode plot of the magnitude of the modulator and the control-to-output transfer function $T_{mp} = T_m T_p$ for the boost converter.

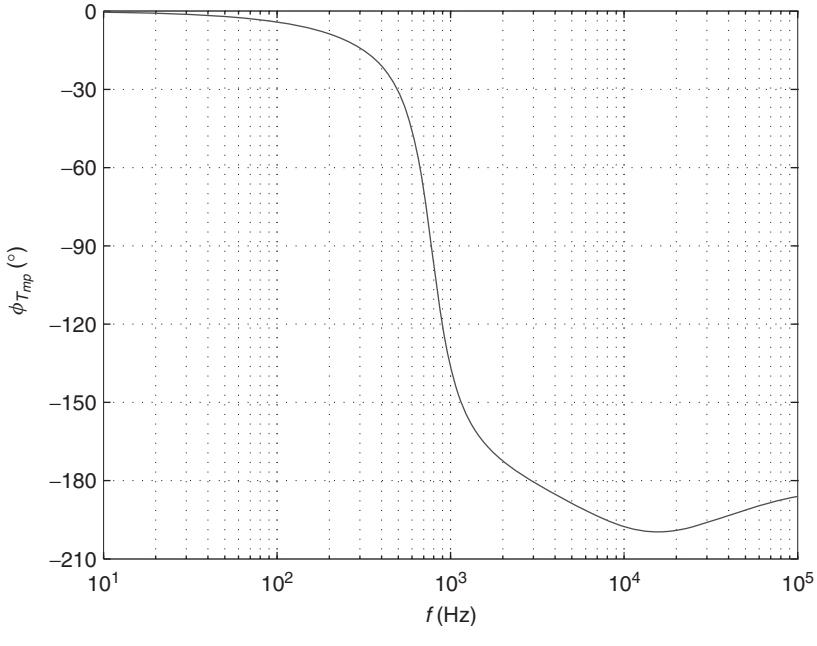


Figure 12.8 Bode plot of the phase of the modulator and the control-to-output transfer function $T_{mp} = T_m T_p$ for the boost converter.

The frequency of the LHP zero is $f_{zn} = 21.09\,\text{kHz}$. At R_{Lmin}, $T_{po} = 37.55\,\text{V}$, $\xi = 0.261$, $f_0 = 783.66\,\text{Hz}$, and $f_{zp} = 9.88\,\text{kHz}$. The transfer function of the pulse-width modulator and the boost converter at $f = 0$ is

$$T_{mpo} = T_m T_{po} = 0.2 \times 37.55 = 7.51 = 17.52\,\text{dB}. \tag{12.11}$$

Figures 12.7 and 12.8 show Bode plots of $T_{mp} = T_m T_p$.

Since $D = V_C / V_{Tm}$ and $V_C \approx V_R$, the reference voltage can be found to be

$$V_R \approx V_C = D_{nom} V_{Tm}. \tag{12.12}$$

The voltage transfer function of the feedback network is

$$\beta = \frac{V_F}{V_O} = \frac{v_f}{v_o} = \frac{R_B}{R_A + R_B}. \tag{12.13}$$

The transfer function of the pulse-width modulator, the boost converter, and the feedback network is

$$\begin{aligned} T_k(s) &\equiv \frac{v_f(s)}{v_c(s)} = T_m T_p(s)\beta = \beta T_{mp}(s) \\ &= -\frac{\beta V_O r_C}{V_{Tm}(1-D)(R_L + r_C)} \frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ &= \frac{\beta V_O r_C \omega_{zn}\omega_{zp}}{V_{Tm}(1-D)(R_L + r_C)\omega_0^2} \frac{\left(1 + \dfrac{s}{\omega_{zn}}\right)\left(1 - \dfrac{s}{\omega_{zp}}\right)}{1 + \dfrac{2\xi s}{\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2} \\ &= T_{ko} \frac{\left(1 + \dfrac{s}{\omega_{zn}}\right)\left(1 - \dfrac{s}{\omega_{zp}}\right)}{1 + \dfrac{2\xi s}{\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2}, \end{aligned} \tag{12.14}$$

where

$$T_{ko} = \frac{\beta V_O r_C \omega_{zn}\omega_{zp}}{V_{Tm}(1-D)(R_L + r_C)\omega_0^2} = \frac{\beta V_O}{V_{Tm}(1-D)} \frac{(1-D)^2 R_L - r}{(1-D)^2 R_L + r}. \tag{12.15}$$

Substituting $s = j\omega$, we get

$$T_k(j\omega) = \beta T_{mp}(j\omega) = T_{ko} \frac{\left(1 + \dfrac{\omega}{\omega_{zn}}\right)\left(1 - \dfrac{\omega}{\omega_{zp}}\right)}{1 - \left(\dfrac{\omega}{\omega_0}\right)^2 + j\dfrac{2\xi\omega}{\omega_0}} = |\beta T_{mp}| e^{j\phi_T k}, \tag{12.16}$$

where

$$|T_k| = |\beta T_{mp}| = T_{ko} \frac{\sqrt{1 + \left(\dfrac{\omega}{\omega_{zn}}\right)^2}\sqrt{1 + \left(\dfrac{\omega}{\omega_{zp}}\right)^2}}{\sqrt{\left[1 - \left(\dfrac{\omega}{\omega_0}\right)^2\right]^2 + \left(\dfrac{2\xi\omega}{\omega_0}\right)^2}} \tag{12.17}$$

and

$$\phi_{T_k} = \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left(\frac{\omega}{\omega_{zp}}\right) - \arctan\left[\frac{\left(\frac{2\xi\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} \leq 1 \tag{12.18}$$

or

$$\phi_{T_k} = -180^\circ + \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left(\frac{\omega}{\omega_{zp}}\right) - \arctan\left[\frac{\left(\frac{2\xi\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} > 1. \tag{12.19}$$

Example 12.2

A boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $T_{mpo} = 7.51$. Calculate T_{ko}. Draw Bode plots of T_k for $D = 0.5$.

Solution. The dc reference voltage is

$$V_R \approx V_C = D_{nom} V_{Tm} = 0.5 \times 5 = 2.5\,\text{V}. \tag{12.20}$$

The voltage transfer function of the feedback network is

$$\beta = \frac{V_F}{V_O} \approx \frac{V_R}{V_O} = \frac{2.5}{20} = 0.125 = -18\,\text{dB}. \tag{12.21}$$

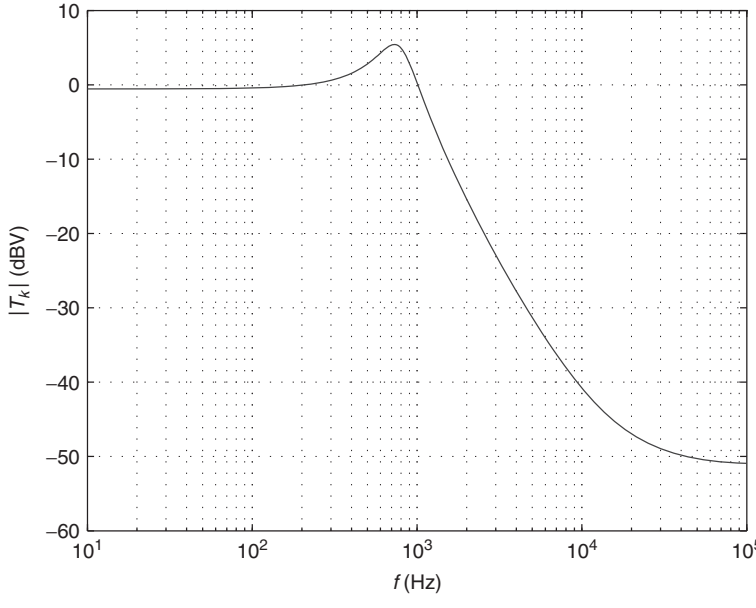


Figure 12.9 Bode plot of the magnitude of the modulator, the control-to-output transfer function, and the feedback network $T_k = \beta T_{mp} = \beta T_m T_p$ for the boost converter.

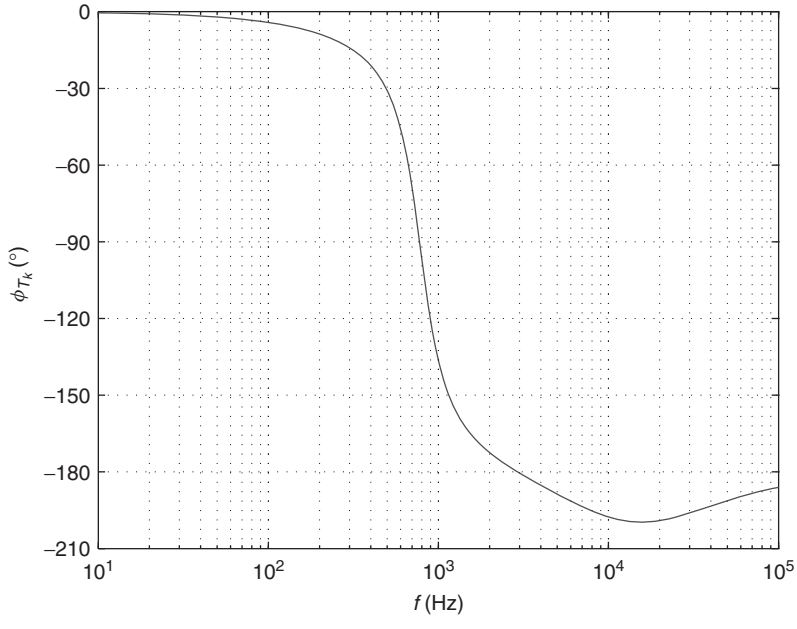


Figure 12.10 Bode plot of the phase of the modulator, the control-to-output transfer function, and the feedback network $T_k = \beta T_{mp} = \beta T_m T_p$ for the boost converter.

Thus,

$$T_{ko} = \beta T_{mpo} = 0.125 \times 7.51 = 0.9388 = -0.549\,\text{dB}. \tag{12.22}$$

Figures 12.9 and 12.10 show Bode plots of T_k. The phases of T_{mp} and T_k are the same as the phase of T_p.

12.5 Error Amplifier

A general circuit of an *error amplifier* and its control block diagram are shown in Figure 12.11. The error amplifier is also called a *controller* or a *compensator*. The feedback voltage consists of a dc component and an ac component,

$$v_F = V_F + v_f. \tag{12.23}$$

Hence, the error voltage is given by

$$v_E = V_E + v_e = V_R - v_F = V_R - V_F - v_f, \tag{12.24}$$

where the dc component of the error voltage is

$$V_E = V_R - V_F, \tag{12.25}$$

and the ac component of the error voltage is

$$v_e = -v_f. \tag{12.26}$$

The current through the impedances Z_i and Z_f is

$$i_{Z_i} = \frac{v_F - V_R}{Z_i} = \frac{V_R - v_C}{Z_f}. \tag{12.27}$$

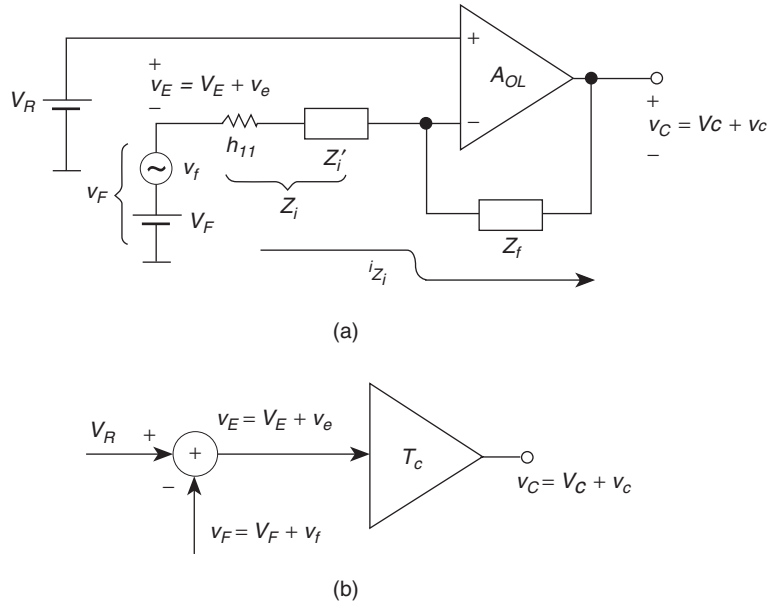


Figure 12.11 General circuit and control block diagram of an error amplifier. (a) General circuit. (b) Control block diagram.

Rearrangement of this equation gives the total control voltage

$$v_C = V_C + v_c = V_R + \frac{Z_f}{Z_i}(V_R - v_F) = V_R + \frac{Z_f}{Z_i}(V_R - V_F - v_f)$$

$$= V_R + \frac{Z_f}{Z_i}(V_R - V_F) - \frac{Z_f}{Z_i}v_f, \tag{12.28}$$

where the dc component of the control voltage is

$$V_C = V_R + \frac{Z_f(0)}{Z_i(0)}(V_R - V_F) = V_R + \frac{Z_f(0)}{Z_i(0)}V_E \approx V_R, \tag{12.29}$$

and the ac component of the control voltage is

$$v_c = -\frac{Z_f}{Z_i}v_f. \tag{12.30}$$

The dc gain of the controller at $V_R = 0$ is obtained from (12.29),

$$T_{C(DC)} \equiv \frac{V_C}{V_E} = \frac{V_C}{V_R - V_F} = \frac{Z_f(0)}{Z_i(0)}. \tag{12.31}$$

Substitution of (12.26) into (12.30) yields

$$v_c = \frac{Z_f}{Z_i}v_e, \tag{12.32}$$

which gives the ac voltage transfer function of the controller,

$$T_c(s) \equiv \frac{v_c(s)}{v_e(s)} = \frac{Z_f(s)}{Z_i(s)}. \tag{12.33}$$

The ac gain of the op-amp is

$$A_v(s) \equiv \frac{v_c(s)}{v_f(s)} = \frac{v_c(s)}{-v_e(s)} = -T_c(s) = -\frac{Z_f(s)}{Z_i(s)}. \tag{12.34}$$

12.6 Integral-single-lead Controller

A control circuit is required in dc–dc converters for the following reasons: to reduce the dc error, to reduce the sensitivity of the closed-loop gain T_{cl} to component values over a wide frequency range, to achieve a fast transient response to sudden changes in the input voltage V_I and/or the load resistance R_L, to reduce the input-to-output noise transmission $|M_{vcl}|$, to reduce the closed-loop output impedance Z_{ocl}, and to satisfy the sufficient degree of relative stability, that is, to ensure a sufficient gain margin GM of the order of -12 dB and phase margin PM of the order of $45–60^\circ$.

An integral-single-lead compensator, also called a second-order integral-lead controller or type II controller [3], is shown in Figure 12.12(a). The circuit has a pole at the origin and a single pole–zero pair. The pole at the origin forms the integral part of the controller and the pole–zero pair forms the lead part of the controller. The controller is an inverting op-amp with a dc reference voltage source V_R. Setting the dc reference voltage V_R to zero, one obtains an equivalent circuit for the ac component, as depicted in Figure 12.12(b). The capacitor C_2 and the resistance $R_1 + h_{11}$ form an integral part of the controller, which ideally introduces a pole at the origin. The capacitor C_1 and the resistor R_2 introduce a zero. The resistor R_2 and the series combination of C_1 and C_2 introduce a pole. The capacitance C_1 is usually much higher than the capacitance C_2, and therefore the frequency of the pole f_{pc} is much higher than the frequency of the zero f_{zc}.

The primary reason for using an integral controller is to obtain very high values of the gain at dc and low frequencies and therefore reduce the dc error, but this benefit typically comes at the expense of reduced stability. This is because the integral controller introduces a phase lag of -90° at all frequencies. The phase lag can partially be compensated (reduced)

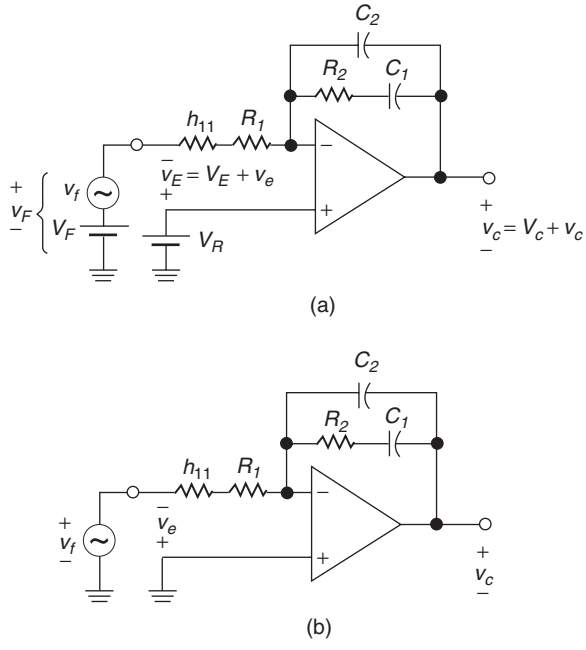


Figure 12.12 Second-order integral-single-lead controller (type II controller). (a) Circuit for both the dc and ac components. (b) Equivalent circuit for the ac component.

by means of a lead controller. The task for the lead controller is to reduce the phase lag and therefore achieve a high gain crossover frequency f_c, while maintaining a specified phase margin PM. The crossover frequency f_c is defined as the frequency at which the magnitude of the loop gain $|T|$ crosses 1 or 0 dB. A high gain crossover frequency f_c normally results in a wide bandwidth of the closed-loop system, yielding a fast response.

Let us assume that the operational amplifier is ideal, that is, its open-loop dc gain and bandwidth are infinite. The voltage transfer function of the amplifier shown in Figure 12.12(a) is given by

$$A_v(s) \equiv \frac{v_c(s)}{v_f(s)} = -\frac{Z_f(s)}{Z_i(s)} = -\frac{\frac{1}{sC_2}\left(R_2 + \frac{1}{sC_1}\right)}{(R_1 + h_{11})\left(R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}\right)}$$

$$= -\frac{1}{C_2(R_1 + h_{11})} \frac{s + \frac{1}{R_2C_1}}{s\left(s + \frac{C_1 + C_2}{R_2C_1C_2}\right)}. \tag{12.35}$$

Since $v_e = v_r - v_f = -v_f$ at $v_r = 0$, the voltage transfer function of the integral-single-lead controller is

$$T_c(s) \equiv \frac{v_c(s)}{v_e(s)} = -A_v(s) = \frac{B(s + \omega_{zc})}{s(s + \omega_{pc})} = \frac{B\omega_{zc}\left(1 + \frac{s}{\omega_{zp}}\right)}{\omega_{pc}s\left(1 + \frac{s}{\omega_{pc}}\right)} = \frac{B\left(1 + \frac{s}{\omega_{zc}}\right)}{K^2 s\left(1 + \frac{s}{\omega_{pc}}\right)}, \tag{12.36}$$

where

$$B = \frac{1}{C_2(R_1 + h_{11})}, \tag{12.37}$$

$$\omega_{zc} = \frac{1}{R_2C_1}, \tag{12.38}$$

$$\omega_{pc} = \frac{C_1 + C_2}{R_2C_1C_2} = \left(\frac{C_1}{C_2} + 1\right)\omega_{zc} = K^2\omega_{zc}, \tag{12.39}$$

and

$$K = \sqrt{\frac{\omega_{pc}}{\omega_{zc}}} = \sqrt{\frac{C_1}{C_2} + 1}. \tag{12.40}$$

It can be seen from (12.36) that the integral-single-lead controller introduces a pole at the origin in addition to a pole–zero pair. The pole at the origin provides a very high gain at low frequencies like an integral controller and the zero–pole pair provides a constant gain and a reduced phase shift between the zero frequency f_{zc} and the pole frequency f_{pc} like a lead controller. Therefore, the controller provides a very high gain at low frequencies as an integral controller and a reduced phase lag between the zero and pole frequencies.

Substitution of $s = j\omega$ into (12.36) yields the frequency response of the integral-single-lead controller

$$T_c(j\omega) = \frac{B\left(1 + j\frac{\omega}{\omega_{zc}}\right)}{K^2 j\omega\left(1 + j\frac{\omega}{\omega_{pc}}\right)} = |T_c|e^{j\phi_{Tc}}, \tag{12.41}$$

where

$$|T_c| = \frac{B}{\omega K^2}\sqrt{\frac{1+\left(\dfrac{\omega}{\omega_{zc}}\right)^2}{1+\left(\dfrac{\omega}{\omega_{pc}}\right)^2}} \tag{12.42}$$

and

$$\phi_{Tc} = -\frac{\pi}{2} + \arctan\left(\frac{\dfrac{\omega}{\omega_{zc}} - \dfrac{\omega}{\omega_{pc}}}{1+\dfrac{\omega^2}{\omega_{zc}\omega_{pc}}}\right). \tag{12.43}$$

The integral part of $|T_c|$ occurs for $f \ll f_{zc}$, which can be approximated by

$$|T_c| \approx \frac{B}{K^2\omega}. \tag{12.44}$$

This means that $|T_c|$ for an integral-single-lead controller is K^2 times lower than that for a standard integral controller at $f < f_{zc}$. Figure 12.13 shows the idealized Bode plots for the voltage transfer function of the integral-single-lead controller. The magnitude $|T_c|$ decreases with frequency at a rate of -20 dB/dec at low frequencies as for an integral controller, it is constant and equal to $|T_{cm}| = R_2/(h_{11} + R_1)$ at mid-frequencies as for a proportional controller, and decreases with frequency again at a rate of -20 dB/dec at high frequency as for a integral controller. This last part of $|T_c|$ is useful in switching power supply applications because it reduces the magnitudes of the switching frequency and its harmonics. The phase shift starts from -90° at low frequencies as for an integral controller, reaches its maximum value at frequency f_m as for a lead controller, and decreases back to -90° at high frequencies as for an integral controller.

Setting the derivative of the term in parentheses in (12.43) to zero and using (12.40), one obtains the frequency at which the phase shift ϕ_{Tc} reaches a maximum value,

$$\omega_m = \sqrt{\omega_{zc}\omega_{pc}} = \frac{\omega_{pc}}{K} = K\omega_{zc} = \frac{K}{R_2C_1}. \tag{12.45}$$

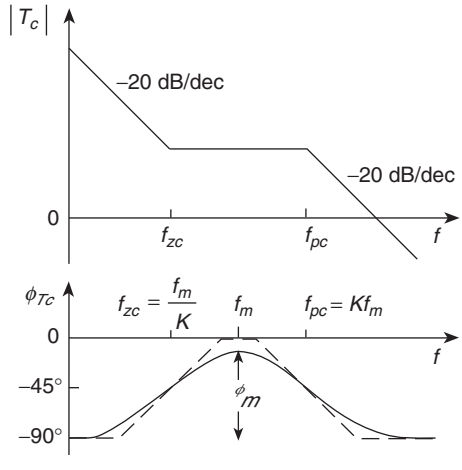


Figure 12.13 Idealized Bode plots for the integral-single-lead controller (type II controller).

Thus, the maximum value of the phase $\phi_{Tc(max)} = \phi_{Tc}(f_m)$ occurs at the geometric mean value of the zero and pole frequencies. Substitution of (12.45) into (12.43) gives

$$\phi_{Tc}(f_m) = -\frac{\pi}{2} + \arctan\left(\frac{\sqrt{\frac{f_{pc}}{f_{zc}}} - \sqrt{\frac{f_{zc}}{f_{pc}}}}{2}\right) = -\frac{\pi}{2} + \arctan\left(\frac{K^2-1}{2K}\right)$$

$$= -\frac{\pi}{2} + \arcsin\left(\frac{K^2-1}{K^2+1}\right). \tag{12.46}$$

Hence, the maximum amount of phase shift reduction, also called the *phase boost*, is

$$\phi_m = \phi_{Tc}(f_m) - \left(-\frac{\pi}{2}\right) = \phi_{Tc}(f_m) + \frac{\pi}{2} = \arctan\left(\frac{K^2-1}{2K}\right) = \arcsin\left(\frac{K^2-1}{K^2+1}\right), \tag{12.47}$$

from which

$$K = \tan\left(\frac{\phi_m}{2} + 45^\circ\right) = \cot\left[\frac{\phi_{Tc}(f_m)}{2}\right]. \tag{12.48}$$

Hence,

$$\phi_m = -\frac{\pi}{2} + 2\arctan\ K. \tag{12.49}$$

Figure 12.14 illustrates the relationship between ϕ_m and K. It can be seen that the phase boost ϕ_m increases from zero to 90° as K is increased from 0 to ∞. The required amount of phase boost ϕ_m can be achieved by adjusting the spread of the zero and pole frequencies $K^2 = f_{pc}/f_{zc}$.

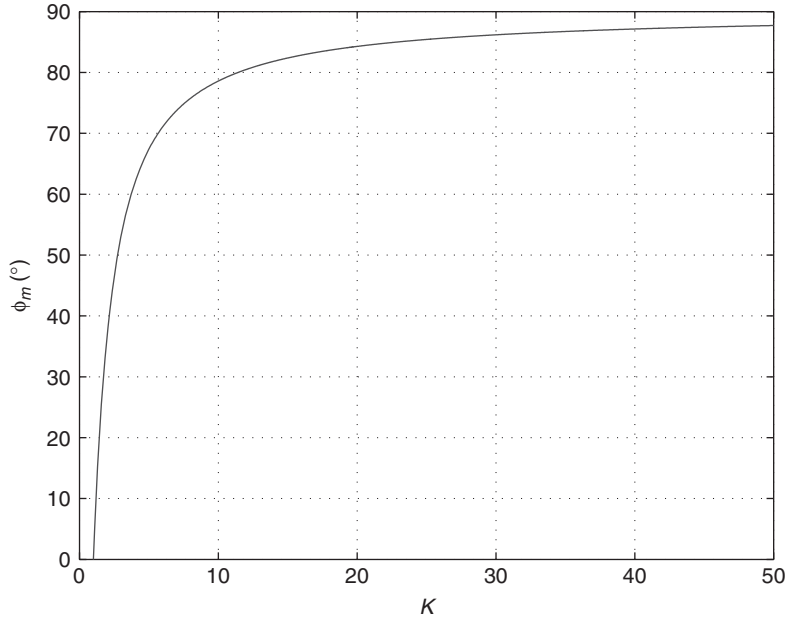


Figure 12.14 Plot of phase ϕ_m versus K for the integral-single-lead controller (type II controller).

Substitution (12.45) into (12.42) yields the magnitude of the controller voltage transfer function at the frequency f_m,

$$|T_c(f_m)| = \frac{B}{K\omega_m}. \tag{12.50}$$

Substituting (12.37) into (12.50) and using (12.39) and (12.45) produces

$$|T_c(f_m)| = \frac{1}{\omega_m KC_2(R_1 + h_{11})} = \frac{R_2}{R_1 + h_{11}}\left(1 - \frac{1}{K^2}\right). \tag{12.51}$$

The *gain crossover frequency* f_c is defined as the frequency at which the loop-gain magnitude $|T|$ is equal to unity,

$$|T(f_c)| = 1 = 0\,\text{dB}. \tag{12.52}$$

It indicates the frequency range in which negative feedback is effective in attenuating audio susceptibility and output impedance.

Relative stability of closed-loop linear systems is measured by two criteria: the gain margin *GM* and the phase margin *PM*. The *gain margin GM* is defined as the reciprocal of the loop-gain magnitude at the frequency f_{-180} at which the loop-gain phase angle reaches -180°:

$$GM \equiv \frac{1}{|T(f_{-180})|} = -20\log|T(f_{-180})|. \tag{12.53}$$

It indicates how many times the loop-gain magnitude can be increased before the system becomes unstable. Typical gain margins range from 6 to 12 dB.

The *phase margin PM* is defined as the amount of the loop-gain phase lag at the crossover frequency f_c that is required to bring the system to the verge of instability:

$$PM \equiv 180^\circ + \phi_T(f_c). \tag{12.54}$$

Typical phase margins range from 45° to 75°. A lower phase margin gives faster transient response and shorter settling time, but more peaking in the closed-loop transfer function and higher ringing and overshoot in transient responses.

The integral-lead controller is usually designed in such a way that the gain crossover frequency f_c is equal to the frequency f_m. The magnitude of the loop gain at the crossover frequency f_c is

$$|T(f_c)| = |T_c(f_c)||T_k(f_c)| = |T_c(f_c)||T_{mp}(f_c)|\beta = 1. \tag{12.55}$$

Hence, using (12.51), one obtains the required value of the controller transfer function magnitude at the crossover frequency f_c,

$$|T_c(f_c)| = \frac{1}{|T_k(f_c)|} = \frac{1}{\beta|T_{mp}(f_c)|} = \frac{1}{\omega_c KC_2(R_1 + h_{11})}. \tag{12.56}$$

Using (12.47), the phase of the loop gain at the crossover frequency f_c is given by

$$\phi_T(f_c) = \phi_{T_k}(f_c) + \phi_{Tc}(f_c) = \phi_{T_k}(f_c) - 90^\circ + \phi_m. \tag{12.57}$$

Hence, the phase margin can be expressed as

$$PM \equiv 180^\circ + \phi_T(f_c) = 180^\circ + \phi_{T_k}(f_c) + \phi_{Tc}(f_c) = 90^\circ + \phi_{T_k}(f_c) + \phi_m, \tag{12.58}$$

which leads to the required phase boost,

$$\phi_m = PM - \phi_{T_k}(f_c) - 90^\circ. \tag{12.59}$$

The phase boost ϕ_m of the integral-single-lead compensator is low. Therefore, this circuit can be used for compensating converters with low negative phase values such as buck converters.

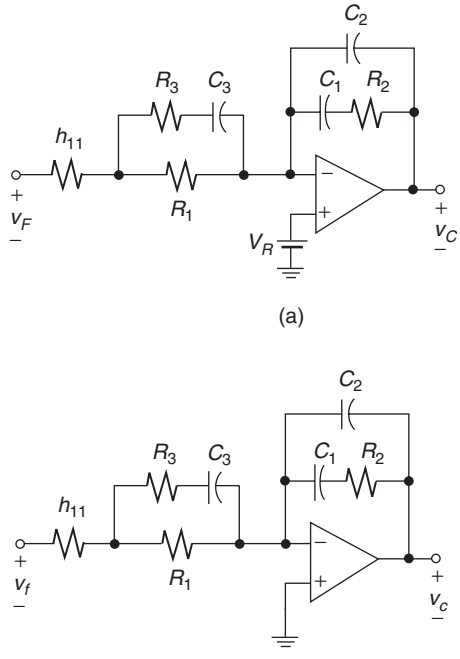


Figure 12.15 Third-order integral-double-lead controller with two zero–pole pairs (type III controller). (a) Circuit. (b) Equivalent circuit for the ac component.

12.7 Integral-double-lead Controller

12.7.1 Analysis of Integral-double-lead Controller

An integral-double-lead compensator, also called a third-order integral-lead controller or type III controller [3], is shown in Figure 12.15(a). The circuit is loaded by the feedback network in the form of $h_{11} = R_A||R_B$ [13]. The controller has a pole at the orign and two zero–pole pairs. An equivalent circuit of the controller for the ac component is depicted in Figure 12.15(b). The Miller integral part of this controller is used to achieve a large low-frequency gain and, therefore, to reduce both the dc error and the closed-loop output impedance at low frequencies. However, an integral controller introduces a phase lag of -90° at all frequencies. The phase lag can be reduced by means of a lead controller in a limited frequency range. This allows a wider closed-loop bandwidth and, therefore, a faster step response. The phase boost ϕ_m of this controller is theoretically 180° and in practice less than 160°. The task for the lead controller is to achieve a high crossover frequency f_c of the control-to-output gain, while maintaining a specified phase margin PM.

The impedances of the controller are

$$Z_f = \frac{\dfrac{1}{sC_2}\left(R_2 + \dfrac{1}{sC_1}\right)}{R_2 + \dfrac{1}{sC_1} + \dfrac{1}{sC_2}} = \frac{s + \dfrac{1}{R_2C_1}}{sC_2\left(s + \dfrac{C_1 + C_2}{R_2C_1C_2}\right)}, \tag{12.60}$$

$$Z_i = h_{11} + \frac{R_1\left(R_3 + \dfrac{1}{sC_3}\right)}{R_1 + R_3 + \dfrac{1}{sC_3}} = \left(h_{11} + \frac{R_1R_3}{R_1 + R_3}\right)\frac{s + \dfrac{R_1 + h_{11}}{C_3[R_3(R_1 + h_{11}) + h_{11}R_1]}}{s + \dfrac{1}{C_3(R_1 + R_3)}}, \quad (12.61)$$

where

$$h_{11} = \frac{R_AR_B}{R_A + R_B}. \quad (12.62)$$

Assume that the open-loop dc gain and the bandwidth of the operational amplifier are infinite. Hence, from (12.60) and (12.60), the voltage transfer function of the controller for the ac component is

$$A_v(s) \equiv \frac{v_c(s)}{v_f(s)} = -\frac{Z_f}{Z_i} = -\frac{R_1 + R_3}{C_2[R_1R_3 + h_{11}(R_1 + R_3)]} \times \frac{\left(s + \dfrac{1}{R_2C_1}\right)\left[s + \dfrac{1}{C_3(R_1 + R_3)}\right]}{s\left(s + \dfrac{C_1 + C_2}{R_2C_1C_2}\right)\left\{s + \dfrac{R_1 + h_{11}}{C_3[R_1R_3 + h_{11}(R_1 + R_3)]}\right\}}. \quad (12.63)$$

At $v_r = 0$, $v_e = -v_f$ and therefore the voltage transfer function of the integral-double-lead controller is

$$T_c(s) \equiv \frac{v_c(s)}{v_e(s)} = -\frac{v_c(s)}{v_f(s)} = -A_v(s) = \frac{B(s + \omega_{zc1})(s + \omega_{zc2})}{s(s + \omega_{pc1})(s + \omega_{pc2})}, \quad (12.64)$$

where

$$B = \frac{R_1 + R_3}{C_2[R_1R_3 + h_{11}(R_1 + R_3)]}, \quad (12.65)$$

$$\omega_{zc1} = \frac{1}{R_2C_1}, \quad (12.66)$$

$$\omega_{zc2} = \frac{1}{C_3(R_1 + R_3)}, \quad (12.67)$$

$$\omega_{pc1} = \frac{C_1 + C_2}{R_2C_1C_2} = \omega_{zc1}\left(\frac{C_1}{C_2} + 1\right), \quad (12.68)$$

and

$$\omega_{pc2} = \frac{R_1 + h_{11}}{C_3[R_1R_3 + h_{11}(R_1 + R_3)]}. \quad (12.69)$$

The voltage transfer function of the controller is $A_v(s) \equiv v_c(s)/v_e(s) = -T_c(s)$. Assuming that $\omega_{zc1} = \omega_{zc2} = \omega_{zc}$ and $\omega_{pc1} = \omega_{pc2} = \omega_{pc}$ and using (12.66) and (12.67),

$$K = \frac{\omega_{pc1}}{\omega_{zc1}} = \frac{\omega_{pc2}}{\omega_{zc2}} = \frac{\omega_{pc}}{\omega_{zc}} = \frac{C_1}{C_2} + 1 = \frac{(R_1 + h_{11})(R_1 + R_3)}{R_1R_3 + h_{11}(R_1 + R_3)}. \quad (12.70)$$

Hence, (12.64) becomes

$$T_c(s) \equiv \frac{v_c(s)}{v_e(s)} = \frac{B(s + \omega_{zc})^2}{s(s + \omega_{pc})^2} = \frac{B\omega_{zc}^2\left(1 + \dfrac{s}{\omega_{zc}}\right)^2}{\omega_{pc}^2 s\left(1 + \dfrac{s}{\omega_{pc}}\right)^2} = \frac{B\left(1 + \dfrac{s}{\omega_{zc}}\right)^2}{K^2 s\left(1 + \dfrac{s}{\omega_{pc}}\right)^2}. \quad (12.71)$$

For $s = j\omega$,

$$T_c(j\omega) = \frac{B\left(1 + j\dfrac{\omega}{\omega_{zc}}\right)^2}{K^2 j\omega\left(1 + j\dfrac{\omega}{\omega_{pc}}\right)^2} = |T_c(\omega)|e^{j\phi_{Tc}(\omega)}, \tag{12.72}$$

where the magnitude of T_c is

$$|T_c(\omega)| = \frac{B\left[1 + \left(\dfrac{\omega}{\omega_{zc}}\right)^2\right]}{\omega K^2\left[1 + \left(\dfrac{\omega}{\omega_{pc}}\right)^2\right]}, \tag{12.73}$$

and the phase shift of T_c is

$$\phi_{Tc}(\omega) = -\frac{\pi}{2} + 2\arctan\left(\frac{\dfrac{\omega}{\omega_{zc}} - \dfrac{\omega}{\omega_{pc}}}{1 + \dfrac{\omega^2}{\omega_{zc}\omega_{pc}}}\right). \tag{12.74}$$

The maximum value of phase ϕ_{Tc} occurs at the geometric mean value of the zero frequency and the pole frequency and, from (12.67), (12.69), and (12.70), is given by

$$\omega_m = \omega_c = \sqrt{\omega_{zc}\omega_{pc}} = \sqrt{K}\omega_{zc} = \frac{\sqrt{K}}{R_2C_1} = \frac{\omega_{pc}}{\sqrt{K}}$$
$$= \frac{R_1 + h_{11}}{C_3\sqrt{K}[R_1R_3 + h_{11}(R_1 + R_3)]}. \tag{12.75}$$

Substitution of (12.75) into (12.74) yields the phase shift at $f = f_m$,

$$\phi_{Tc}(f_m) = -\frac{\pi}{2} + 2\arctan\left(\frac{K-1}{2\sqrt{K}}\right) = -\frac{\pi}{2} + 2\arcsin\left(\frac{K-1}{K+1}\right). \tag{12.76}$$

Thus, the maximum amount of the phase shift reduction is

$$\phi_m = \phi_{Tc}(f_m) + \frac{\pi}{2} = 2\arctan\left(\frac{K-1}{2\sqrt{K}}\right) = 2\arcsin\left(\frac{K-1}{K+1}\right), \tag{12.77}$$

from which

$$K = \frac{1 + \sin\left(\dfrac{\phi_m}{2}\right)}{1 - \sin\left(\dfrac{\phi_m}{2}\right)} = \tan^2\left(\frac{\phi_m}{4} + \frac{\pi}{4}\right). \tag{12.78}$$

Hence,

$$\phi_m = -\pi + 4\arctan\sqrt{K}. \tag{12.79}$$

Figure 12.16 shows ϕ_m versus K. Note that ϕ_m increases from zero to about 160° as K is increased from nearly zero to 100.

Substituting (12.75) into (12.73) and using (12.65) and (12.70), one obtains the magnitude of the controller voltage transfer function at the frequency $f = f_m$,

$$|T_c(f_m)| = \frac{B}{\omega_m K} = \frac{R_1 + R_3}{\omega_m K C_2[R_1R_3 + h_{11}(R_1 + R_3)]} = \frac{1}{\omega_m C_2(R_1 + h_{11})}. \tag{12.80}$$

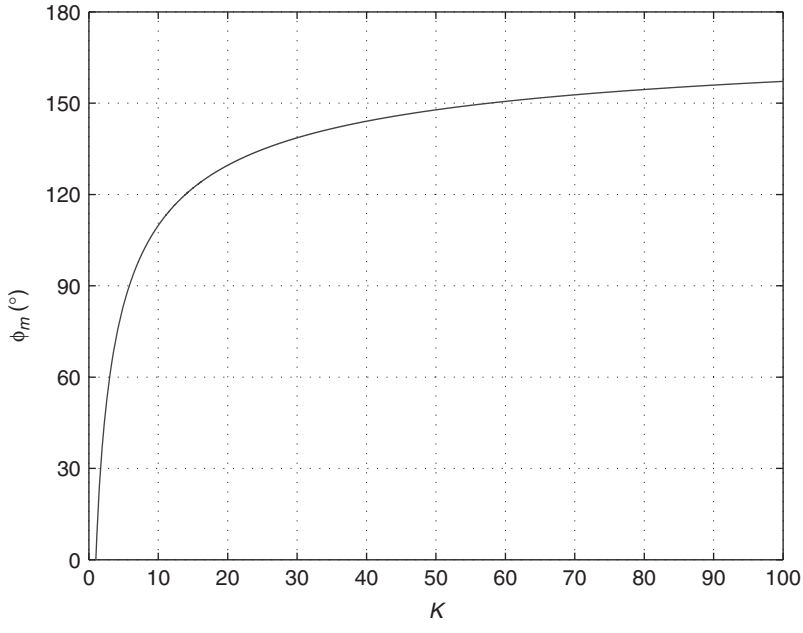


Figure 12.16 Maximum phase boost ϕ_m versus K for the integral-double-lead controller with two zero–pole pairs (type III controller).

The magnitude of the loop gain at the crossover frequency f_c is

$$|T(f_c)| = |T_c(f_c)||T_k(f_c)| = |T_c(f_c)||T_{mp}(f_c)|\beta = 1. \tag{12.81}$$

Assuming that $f_c = f_m$ and using (12.80) and (12.81), one arrives at

$$|T_c(f_c)| = \frac{1}{|T_k(f_c)|} = \frac{1}{\beta|T_{mp}(f_c)|} = \frac{1}{\omega_c C_2(R_1 + h_{11})}. \tag{12.82}$$

The phase shift of the loop gain at the crossover frequency f_c is

$$\phi_T(f_c) = \phi_{T_k}(f_c) + \phi_{Tc}(f_c). \tag{12.83}$$

Using (12.76), the phase margin is obtained as

$$PM = 180^\circ + \phi_T(f_c) = 180^\circ + \phi_{T_k}(f_c) + \phi_{T_c}(f_c) = 90^\circ + \phi_{Tmp}(f_c) + \phi_m. \tag{12.84}$$

12.7.2 Design of Integral-double-lead Controller

A boost PWM converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $V_R = 25\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $R_{Lmax} = 200\,\Omega$, $D_{nom} = 0.5$, $\xi = 0.261$, $f_0 = 783.66\,\text{Hz}$, $f_{zp} = 9.88\,\text{kHz}$, $f_{zn} = 21.09\,\text{kHz}$, $V_{Tm} = 5\,\text{V}$, and $T_{ko} = 0.9388$. Design a control circuit such that $PM = 60^\circ$.

Solution. The voltage transfer function of the feedback network is

$$\beta = \frac{V_F}{V_O} \approx \frac{V_R}{V_O} = \frac{R_B}{R_A + R_B} = \frac{2.5}{20} = 0.125 = -18.06\,\text{dB}. \tag{12.85}$$

Assuming $R_B = 620\,\Omega$, one obtains

$$R_A = R_B\left(\frac{1}{\beta} - 1\right) = 4.34\,\text{k}\Omega \tag{12.86}$$

and

$$h_{11} = \frac{R_A R_B}{R_A + R_B} = 542.5\,\Omega. \tag{12.87}$$

Note that $1/h_{22} = R_A + R_B = 0.62 + 4.34 = 4.96\,\text{k}\Omega \gg R_{Lmax} = 200\,\Omega$ and therefore $1/h_{22}||R_{Lmax} = 0.192\,\Omega$.

Assume that $f_c = f_m = 2\,\text{kHz}$. From (12.19),

$$\begin{aligned}\phi_{T_k}(f_c) &= -180^\circ + \arctan\left(\frac{f_c}{f_{zn}}\right) - \arctan\left(\frac{f_c}{f_{zp}}\right) - \arctan\left[\frac{\left(\frac{2\xi f_c}{f_0}\right)}{1-\left(\frac{f_c}{f_0}\right)^2}\right] \\ &= -180^\circ + \arctan\left(\frac{2}{21.09}\right) - \arctan\left(\frac{2}{9.88}\right) - \arctan\left[\frac{\left(\frac{2\times 0.261\times 2}{0.78366}\right)}{1-\left(\frac{2}{0.78366}\right)^2}\right] \\ &= -180^\circ + 5.42^\circ - 11.44^\circ + 13.59^\circ = -172.43^\circ.\end{aligned} \tag{12.88}$$

Since the phase margin $PM = 60^\circ$, one obtains the required phase boost

$$\phi_m = PM - \phi_{T_k}(f_c) - 90^\circ = 60^\circ + 172.43^\circ - 90^\circ = 142.43^\circ, \tag{12.89}$$

and the K factor

$$K = \tan^2\left(\frac{\phi_m}{4} + 45^\circ\right) = \tan^2\left(\frac{142.43^\circ}{4} + 45^\circ\right) = 36.547. \tag{12.90}$$

The frequencies of the poles and zeros of the controller are

$$f_{zc} = f_c/\sqrt{K} = 2000/\sqrt{36.547} = 330.851\,\text{Hz} \tag{12.91}$$

and

$$f_{pc} = f_c\sqrt{K} = 2000\sqrt{36.547} = 12.09\,\text{kHz}. \tag{12.92}$$

From (12.17),

$$\begin{aligned}|T_k(f_c)| = \beta|T_{mp}(f_c)| &= T_{ko}\frac{\sqrt{1+\left(\frac{\omega_c}{\omega_{zn}}\right)^2}\sqrt{1+\left(\frac{\omega_c}{\omega_{zp}}\right)^2}}{\sqrt{\left[1-\left(\frac{\omega_c}{\omega_0}\right)^2\right]^2 + \left(\frac{2\xi\omega_c}{\omega_0}\right)^2}} \\ &= 0.9388\frac{\sqrt{1+\left(\frac{2}{21.09}\right)^2}\sqrt{1+\left(\frac{2}{9.88}\right)^2}}{\sqrt{\left[1-\left(\frac{2}{0.78366}\right)^2\right]^2 + \left(\frac{2\times 0.261\times 2}{0.78366}\right)^2}} = 0.1696 = -15.4\,\text{dB}.\end{aligned} \tag{12.93}$$

Next,

$$|T_c(f_c)| = \frac{1}{|T_k(f_c)|} = \frac{1}{\beta|T_{mp}(f_c)|} = \frac{1}{0.1696} = 5.8955 = 15.4\,\text{dB} \tag{12.94}$$

and

$$B = \omega_c K|T_c(f_c)| = 2\pi \times 2000 \times 36.547 \times 5.8955 = 2.7076 \times 10^6\,(\text{rad/s}). \tag{12.95}$$

Bode plots of T_c of the controller are shown in Figures 12.17 and 12.18.

Assuming $R_1 = 100\,\text{k}\Omega$ and using (12.70), one obtains

$$R_3 = \frac{R_1[R_1 - h_{11}(K-1)]}{(K-1)(R_1 + h_{11})} = \frac{100[100 - (36.547-1)0.542]}{(36.547-1)(100+0.542)} = 2.259\,\text{k}\Omega. \tag{12.96}$$

Pick $R_3 = 2.2\,\text{k}\Omega$. Hence, from (12.82),

$$C_2 = \frac{\beta|T_{mp}(f_c)|}{\omega_c(R_1 + h_{11})} = \frac{0.1696}{2 \times \pi \times 2 \times 10^3 \times (100 + 0.542) \times 10^3} = 134\,\text{pF}. \tag{12.97}$$

Pick $C_2 = 150\,\text{pF}$. From (12.70),

$$C_1 = C_2(K-1) = 0.15 \times (36.547 - 1) = 5.33\,\text{nF}. \tag{12.98}$$

Pick $C_1 = 5\,\text{nF}$. Using (12.75),

$$R_2 = \frac{\sqrt{K}}{\omega_c C_1} = \frac{\sqrt{36.547}}{2 \times \pi \times 2 \times 10^3 \times 5 \times 10^{-9}} = 96.22\,\text{k}\Omega. \tag{12.99}$$

Pick $R_2 = 100\,\text{k}\Omega$. From (12.75),

$$\begin{aligned} C_3 &= \frac{R_1 + h_{11}}{\omega_c\sqrt{K}[R_1R_3 + h_{11}(R_1 + R_3)]} \\ &= \frac{(100 + 0.542) \times 10^3}{2 \times \pi \times 2 \times 10^3\sqrt{36.547}[100 \times 2.2 + 0.542(100 + 2.2)] \times 10^6} \\ &= 4.8\,\text{nF}. \end{aligned} \tag{12.100}$$

Pick $C_3 = 5\,\text{nF}$. From (12.65),

$$\begin{aligned} B &= \frac{R_1 + R_3}{C_2[R_1R_3 + h_{11}(R_1 + R_3)]} \\ &= \frac{(100 + 2.2) \times 10^3}{0.15 \times 10^{-9} \times [100 \times 2.2 + 0.542 \times (100 + 2.2)] \times 10^6} \\ &= 2.474 \times 10^6\,(\text{rad/sec}). \end{aligned} \tag{12.101}$$

The frequencies of the poles and zeros of the controller with standard resistors and capacitors are

$$f_{zc1} = \frac{1}{2\pi R_2 C_1} = \frac{1}{2 \times \pi \times 100 \times 10^3 \times 5 \times 10^{-9}} = 318.31\,\text{Hz}, \tag{12.102}$$

$$f_{zc2} = \frac{1}{2\pi C_3(R_1 + R_3)} = \frac{1}{2 \times \pi \times 5 \times 10^{-9}(100 + 2.2) \times 10^3} = 311.46\,\text{Hz}, \tag{12.103}$$

$$f_{pc1} = f_{zc1}\left(\frac{C_1}{C_2} + 1\right) = 318.31\left(\frac{5}{0.15} + 1\right) = 10.929\,\text{kHz}, \tag{12.104}$$

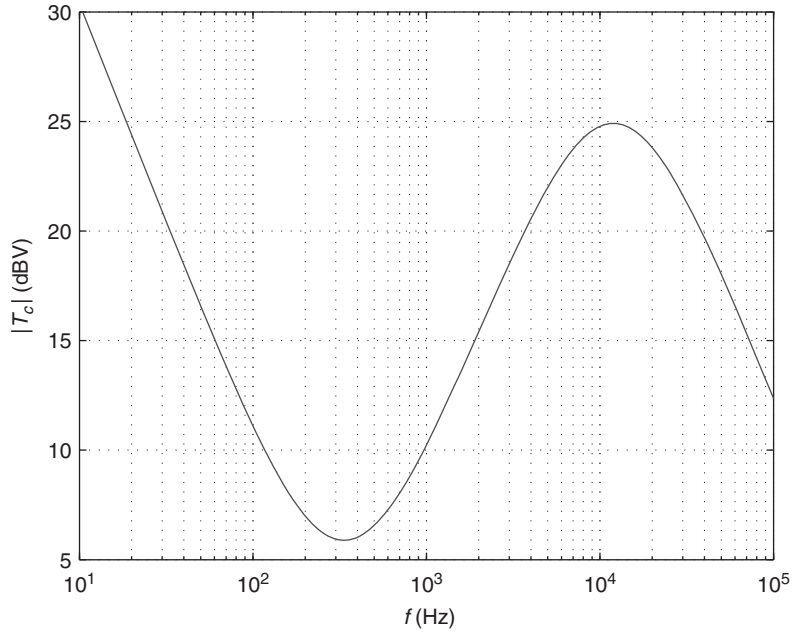


Figure 12.17 Bode plot of the magnitude of the voltage transfer function T_c for the designed integral-double-lead controller with two zero–pole pairs (type III converter).

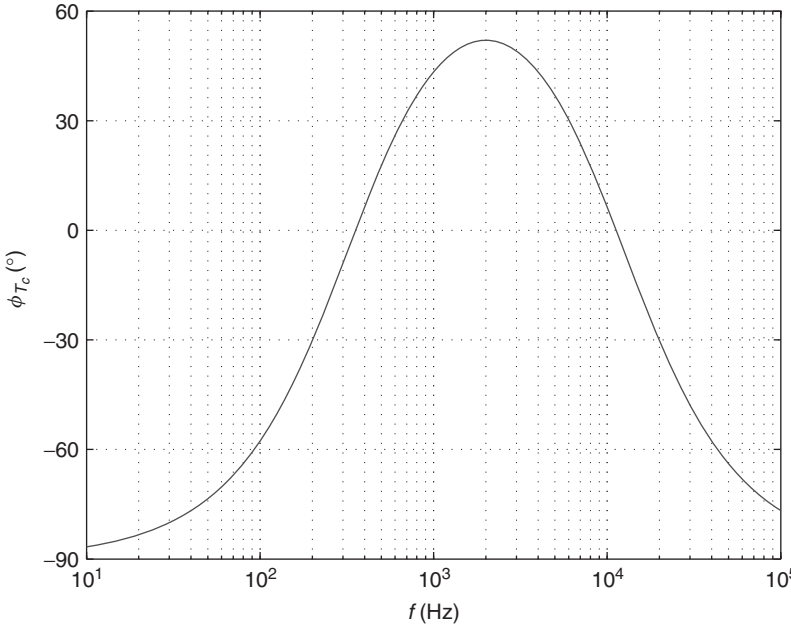


Figure 12.18 Bode plot of the phase of the voltage transfer function T_c for the designed integral-double-lead controller with two zero-pole pairs (Type III).

and

$$f_{pc2} = \frac{R_1 + h_{11}}{2\pi C_3[R_1R_3 + h_{11}(R_1 + R_3)]}$$
$$= \frac{(100 + 0.542)10^3}{2 \times \pi \times 5 \times 10^{-9}[100 \times 2.2 + 0.542(100 + 2.2)] \times 10^6}$$
$$= 11.621\,\text{kHz}. \tag{12.105}$$

12.8 Loop Gain

The loop gain of the converter is

$$T(s) \equiv \left.\frac{v_f(s)}{v_e(s)}\right|_{v_i=i_o=0} = T_c(s)T_{mp}(s)\beta = T_c(s)T_mT_p(s)\beta$$
$$= \frac{T_x(s + \omega_{zc})^2(s + \omega_{zn})(s - \omega_{zp})}{s(s + \omega_{pc})^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}, \tag{12.106}$$

where

$$T_x = -\frac{\beta B V_O r_C}{V_{Tm}(1 - D)(R_L + r_C)}. \tag{12.107}$$

Example 12.3

A boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $\beta = 0.125$, $T_m = 0.2\,\text{V}^{-1}$, $f_{zn} = 21.09\,\text{kHz}$, $f_{zp} = 9.88\,\text{kHz}$, $f_0 = 783.66\,\text{Hz}$, $\xi = 0.261$, $B = 2.7079 \times$

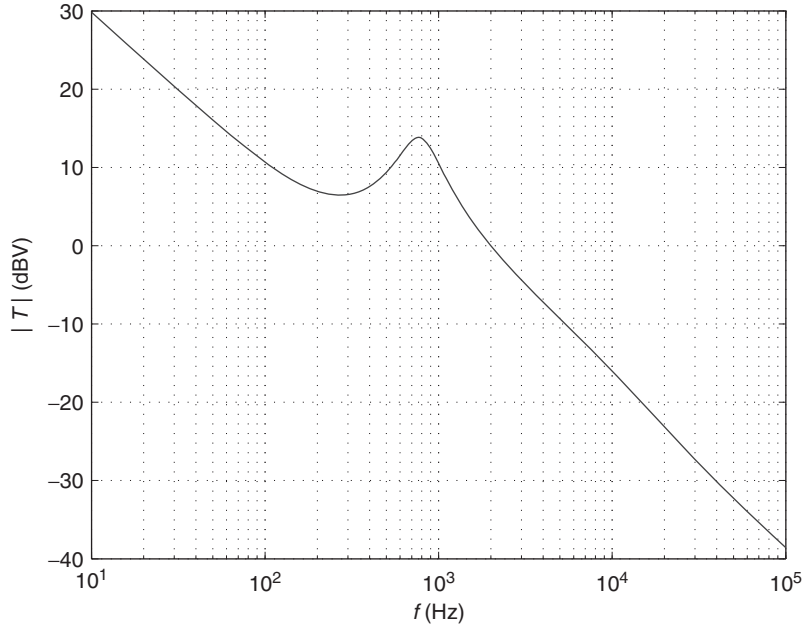


Figure 12.19 Bode plot of the magnitude of the loop gain T for the boost converter.

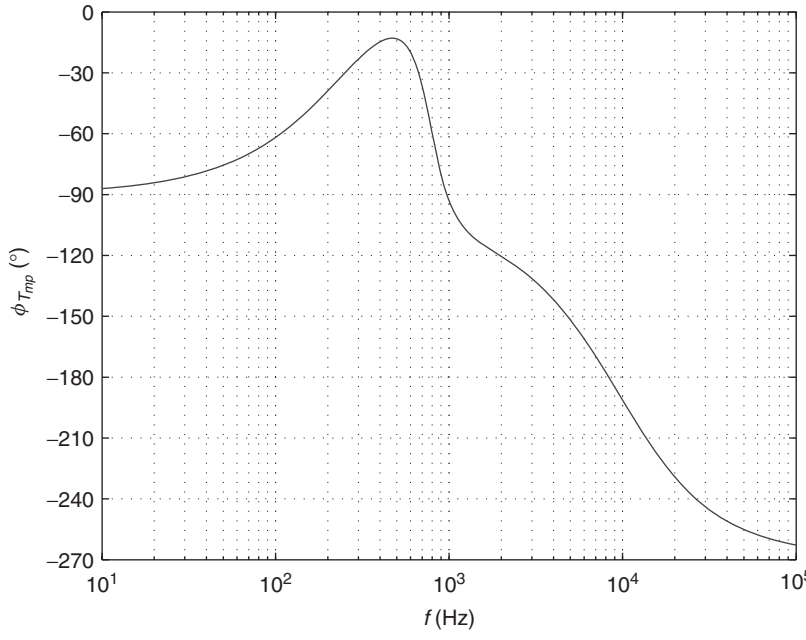


Figure 12.20 Bode plot of the phase of the loop gain T for the boost converter.

10^6 rad/s, $f_{zc} = 330.829$ Hz, and $f_{zp} = 12.009$ kHz. Draw Bode plots for the loop gain T of the boost converter for $D = 0.5$.

Solution. Figures 12.19 and 12.20 show Bode plots of the loop gain T for $D = 0.5$. The crossover frequency is $f_c = 2$ kHz at $D_{nom} = 0.5$. The phase margin is $PM = 60^\circ$. The phase crosses -180° at $f_{-180^\circ} = 8.5$ kHz and the gain margin is $GM = 14$ dB.

12.9 Closed-loop Control-to-output Voltage Transfer Function

The closed-loop control-to-output transfer function is found to be

$$T_{cl}(s) \equiv \left.\frac{v_o(s)}{v_r(s)}\right|_{v_i=i_o=0} = \frac{A(s)}{1+\beta A(s)} = \frac{T_c(s)T_mT_p(s)}{1+\beta T_c(s)T_mT_p(s)}$$
$$= \frac{T_x}{\beta}\ \frac{(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}{s(s+\omega_{pc})^2(s^2+2\xi\omega_0 s+\omega_0^2)+T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}. \quad (12.108)$$

Example 12.4

A boost converter has $\beta = 0.125$, $T_m = 0.2\,\mathrm{V}^{-1}$, $V_{Inom} = 12$ V, $V_O = 20$ V, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu$H, $r_L = 0.19\,\Omega$, $C = 68\,\mu$F, $r_C = 0.111\,\Omega$, $R_1 = 100\,\mathrm{k}\Omega$, $R_2 = 100\,\mathrm{k}\Omega$, $R_3 = 2.2\,\mathrm{k}\Omega$, $C_1 = 5$ nF, $C_2 = 0.15$ nF, and $C_3 =$

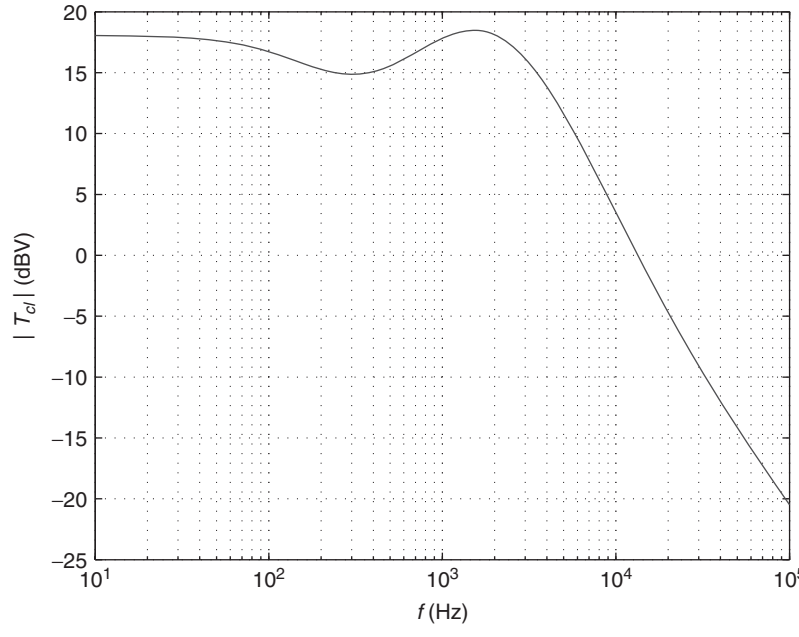


Figure 12.21 Bode plot of the magnitude of the closed-loop control-to-output transfer function T_{cl} for the boost converter.

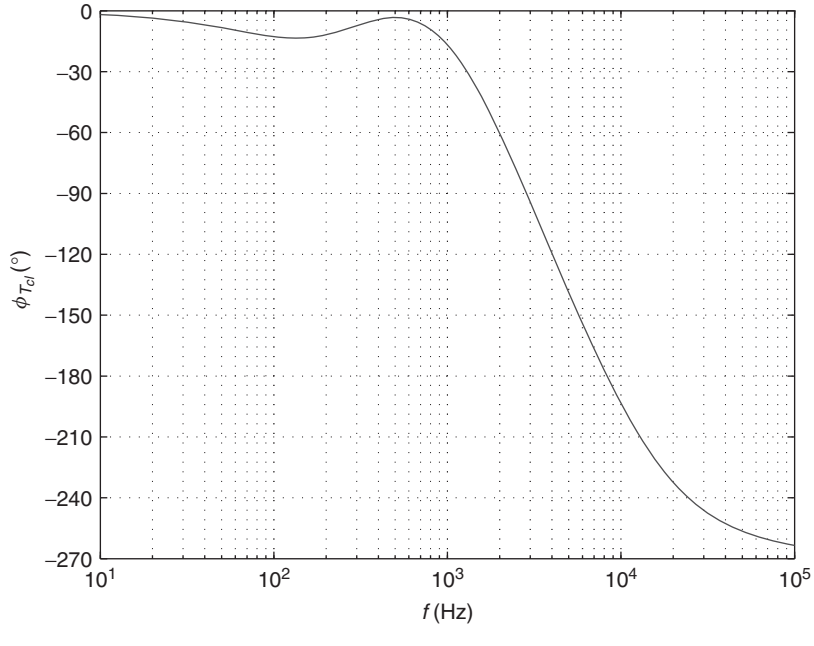


Figure 12.22 Bode plot of the phase of the closed-loop control-to-output transfer function T_{cl} for the boost converter.

5 nF. Calculate $T_{clo} = T_{cl}(0)$. Draw Bode plots for the closed-loop control-to-output transfer function T_{cl} of the boost converter for $D = 0.5$.

Solution. The closed-loop control-to-output transfer function at $f = 0$ is

$$T_{clo} = T_{cl}(0) \approx \frac{1}{\beta} = \frac{1}{0.125} = 8 = 18\,\text{dB}. \tag{12.109}$$

Figures 12.21 and 12.22 show Bode plots of T_{cl}. The bandwidth of the closed-loop control-to-output transfer function is $BW_f = 2\,\text{kHz}$ at $D = 0.5$.

12.10 Closed-loop Audio Susceptibility

The closed-loop input-to-output voltage transfer function, called the audio susceptibility, is given by

$$M_{vcl}(s) \equiv \left.\frac{v_o(s)}{v_i(s)}\right|_{v_r = i_o = 0} = \frac{M_v(s)}{1 + T(s)} = \frac{(1-D)R_L r_C}{L(R_L + r_C)} \times \frac{s(s+\omega_{pc})^2(s+\omega_{zn})}{s(s+\omega_{pc})^2(s^2 + 2\xi\omega_0 s + \omega_0^2) + T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}. \tag{12.110}$$

Example 12.5

A boost converter has $\beta = 0.125$, $V_{Tm} = 5\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C =$

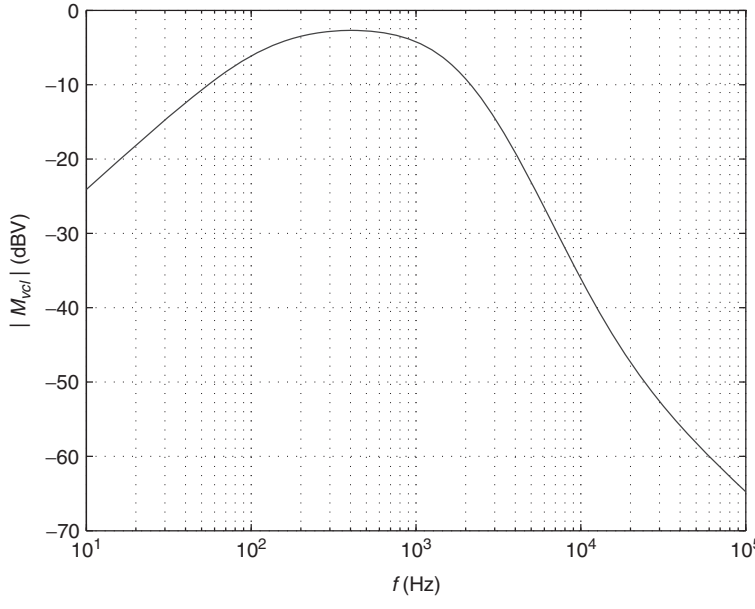


Figure 12.23 Bode plot of the magnitude of the closed-loop input-to-output transfer function M_{vcl} for the boost converter.

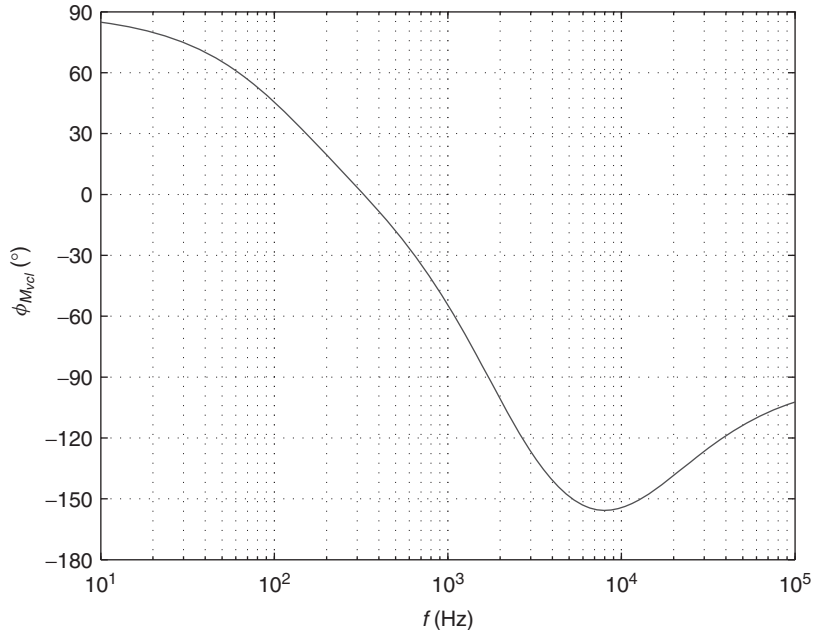


Figure 12.24 Bode plot of the phase of the closed-loop input-to-output transfer function M_{vcl} for the boost converter.

0.111 Ω, $R_1 = 100\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $R_3 = 2.2\,\text{k}\Omega$, $C_1 = 5\,\text{nF}$, $C_2 = 0.15\,\text{nF}$, and $C_3 = 5\,\text{nF}$. Draw Bode plots for the closed-loop input-to-output transfer function M_{vcl} of the boost converter for $D = 0.5$.

Solution. Figures 12.23 and 12.24 show Bode plots of M_{vcl}.

12.11 Closed-loop Input Impedance

Referring to the block diagram shown in Figure 12.4(a) and setting $v_r = 0$,

$$d = -\beta T_c T_m v_o. \tag{12.111}$$

Using Kirchhoff's curret law and assuming that $R_A + R_B \gg R_L$, one obtains

$$i_l = D i_l + I_L d + \frac{v_o}{Z_2}, \tag{12.112}$$

which gives

$$i_l = \frac{v_o}{Z_2(1-D)} + \frac{I_L d}{1-D}. \tag{12.113}$$

Substitution of (12.111) into (12.112) yields

$$i_l v_o \left[\frac{1}{Z_2(1-D)} - \frac{I_L \beta T_c T_m}{1-D}\right]. \tag{12.114}$$

A dc analysis of the boost converter leads to

$$I_L = \frac{I_O}{1-D}. \tag{12.115}$$

Substituting (12.115) into (12.113) gives

$$i_l = v_o \left[\frac{1}{Z_2(1-D)} - \frac{I_O \beta T_c T_m}{(1-D)^2} \right]. \tag{12.116}$$

Dividing both sides by v_i gives the closed-loop input admittance

$$Y_{icl}(s) \equiv \left. \frac{i_l}{v_i} \right|_{v_r(r)=0} = \left[\frac{1}{Z_2(1-D)} - \frac{I_O \beta T_c T_m}{(1-D)^2} \right] \frac{v_o}{v_i} \tag{12.117}$$

which, after substitution of (12.110), simplifies to

$$Y_{icl}(s) = \frac{1}{Z_2(1-D)} \frac{M_v}{1+T} - \frac{I_O \beta T_c T_m}{(1-D)^2} \frac{M_v}{1+T}. \tag{12.118}$$

Dividing M_v by T_p gives

$$M_v = -\frac{R_L(1-D)^2}{V_O L(s-\omega_{zp})} T_p. \tag{12.119}$$

Substitution of (12.119) into (12.118) produces

$$Y_{icl}(s) = \frac{1}{L(s-\omega_{zp})} \frac{\beta A(s)}{1+T} + \frac{1}{Z_2(1-D)} \frac{M_v}{1+T}. \tag{12.120}$$

The impedance Z_2 is given by

$$Z_2 = \frac{R_L \left(r_C + \dfrac{1}{sC} \right)}{R_L + r_C + \dfrac{1}{sC}} = \frac{R_L r_C}{R_L + r_C} \frac{s + \dfrac{1}{r_C C}}{s + \dfrac{1}{C(R_L + r_C)}} = \frac{R_L r_C}{R_L + r_C} \frac{s+\omega_{zn}}{s+\omega_{rc}}, \tag{12.121}$$

where

$$\omega_{zn} = \frac{1}{r_C C} \tag{12.122}$$

and

$$\omega_{rc} = \frac{1}{C(R_L + r_C)}. \tag{12.123}$$

Hence, one arrives at the closed-loop input admittance

$$Y_{icl}(s) = \frac{\beta T_{cl}}{L(s-\omega_{zp})} + \frac{M_{vcl}}{Z_2(1-D)} = \frac{\beta T_{cl}}{L(s-\omega_{zp})} + \frac{(R_L + r_C)(s+\omega_{rc}) M_{vcl}}{R_L r_C (1-D)(s+\omega_{zn})} \tag{12.124}$$

and the closed-loop input impedance

$$\begin{aligned} Z_{icl}(s) &= \frac{1}{Y_{icl}(s)} \\ &= \frac{L[s(s+\omega_{pc})^2(s^2 + 2\xi\omega_0 s + \omega_0^2) + T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})]}{s(s+\omega_{pc})^2(s+\omega_{rc}) + T_x(s+\omega_{zc})^2(s+\omega_{zn})}. \end{aligned} \tag{12.125}$$

At low frequencies, $|T| \gg 1$ and therefore $|T|/|1+T| \approx 1$, $|M_{vcl}| \ll 1$, and the low-frequency closed-loop input impedance can be approximated by

$$Z_{icl}(s) \approx L(s-\omega_{zp}) \tag{12.126}$$

and the dc closed-loop input resistance is

$$R_{icl}(0) = Z_{icl}(0) = -\omega_{zp} L = -[(1-D)^2 R_L - r]. \tag{12.127}$$

The dc closed-loop input resistance can be expressed in terms of the dc voltage transfer function $M_{V\,DC} = 1/(1-D)$ as

$$R_{icl}(0) \approx -(1-D)^2 R_L = -\frac{R_L}{1/(1-D)^2} = -\frac{R_L}{M_{V\,DC}^2}. \tag{12.128}$$

The closed-loop output impedance can also be represented as the closed-loop input resistance and the closed-loop reactance

$$Z_{icl} = |Z_{icl}| \cos\phi_{Zicl} + j\,|Z_{icl}| \sin\phi_{Zicl} = R_{icl} + jX_{icl} \tag{12.129}$$

where $R_{icl} = |Z_{icl}| \cos\phi_{Zicl}$ and $X_{icl} = |Z_{icl}| \sin\phi_{Zicl}$.

Example 12.6

A boost converter has $\beta = 0.125$, $V_{Tm} = 5\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $r = 0.316\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $R_{Lmin} = 40\,\Omega$, $R_1 = 100\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $R_3 = 2.2\,\text{k}\Omega$, $C_1 = 5\,\text{nF}$, $C_2 = 0.15\,\text{nF}$, and $C_3 = 5\,\text{nF}$. Calculate $R_{icl}(0)$. Draw the plots for the closed-loop input impedance Z_{icl} as the magnitude and phase and also as the real and imaginary parts for the boost converter.

Solution. The closed-loop input resistance is

$$R_{icl}(0) = -[(1-D_{nom})^2 R_{Lmin} - r] = -[(1-0.5)^2 \times 40 - 0.316] = -9.684\,\Omega. \tag{12.130}$$

Figures 12.25 and 12.26 show plots of $Z_{icl} = |Z_{icl}|e^{j\phi_{Zicl}}$ versus frequency. Note that the phase ϕ_{Zicl} is close to -180° at low frequencies. Figures 12.27 and 12.28 depict plots of

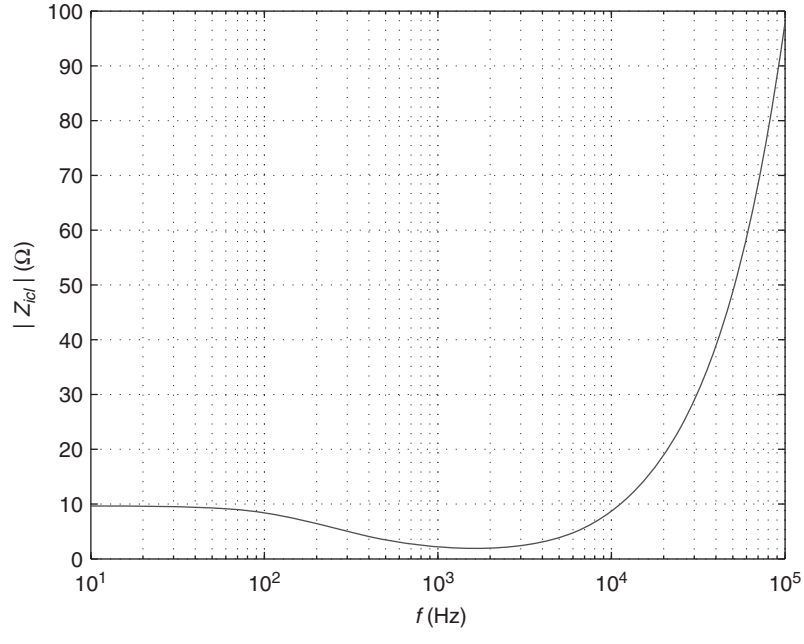


Figure 12.25 The magnitude of the closed-loop input impedance Z_{icl} versus frequency for the boost converter.

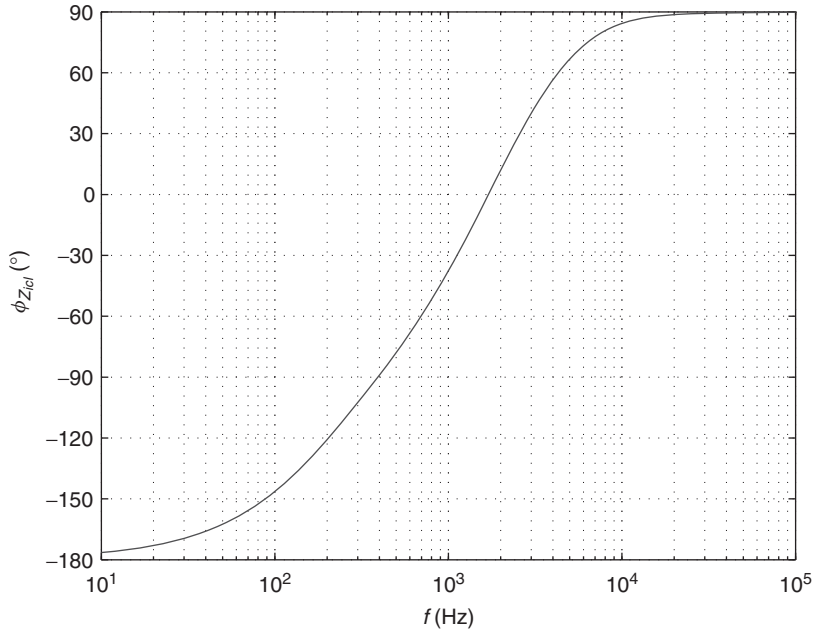


Figure 12.26 The phase of the closed-loop input impedance Z_{icl} versus frequency for the boost converter.

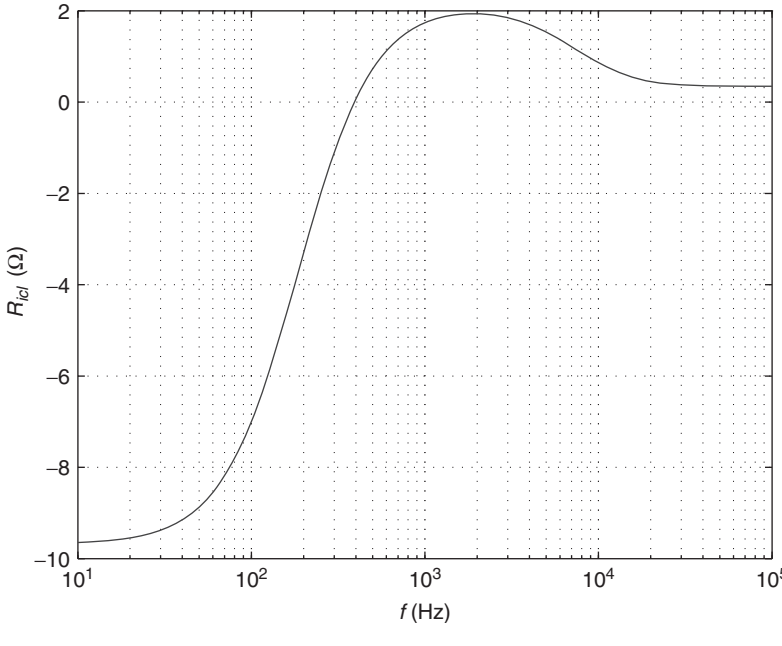


Figure 12.27 The input resistance of the closed-loop input impedance $Z_{icl} = R_{icl} + jX_{icl}$ versus frequency for the boost converter.

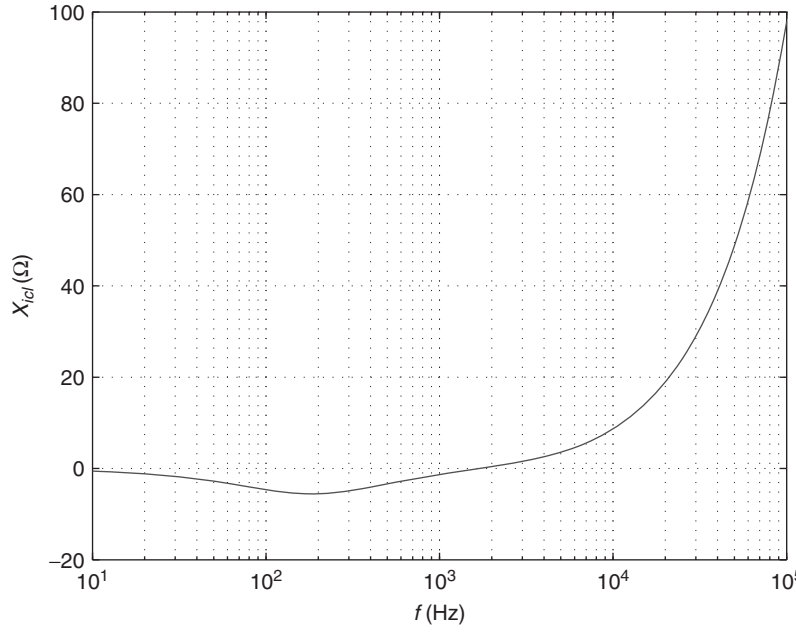


Figure 12.28 The input reactance of the closed-loop input impedance $Z_{icl} = R_{icl} + jX_{icl}$ versus frequency for the boost converter.

$Z_{icl} = R_{icl} + jX_{icl}$ versus frequency. The input resistance R_{icl} is negative at low frequencies. This may cause instablity.

12.12 Closed-loop Output Impedance

The closed-loop output impedance including the load resistance R_L is

$$Z_{ocl}(s) \equiv \left.\frac{v(s)}{i(s)}\right|_{v_r(s)=0 \text{ and } v_i(s)=0} = \frac{Z_o(s)}{1+T(s)} = \frac{R_L r_C}{R_L + r_C} \times \frac{s(s+\omega_{pc})^2(s+\omega_{zn})(s+\omega_{rl})}{s(s+\omega_{pc})^2(s^2+2\xi\omega_0 s+\omega_0^2)+T_x(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}, \quad (12.131)$$

where v and i are the test voltage and current, respectively.

The closed-loop output impedance excluding the load resistance R_L is given by

$$\frac{1}{Z'_{ocl}} = \frac{1}{Z_{ocl}} - \frac{1}{R_L}. \quad (12.132)$$

Since $|Z_{ocl}| \ll R_L$, $Z'_{ocl} \approx Z_{ocl}$. The magnitude of the output impedance $|Z'_{ocl}|$ of an ideal voltage source should be zero at all frequencies.

Example 12.7

A boost converter has $\beta = 0.125$, $V_{Tm} = 5\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C =$

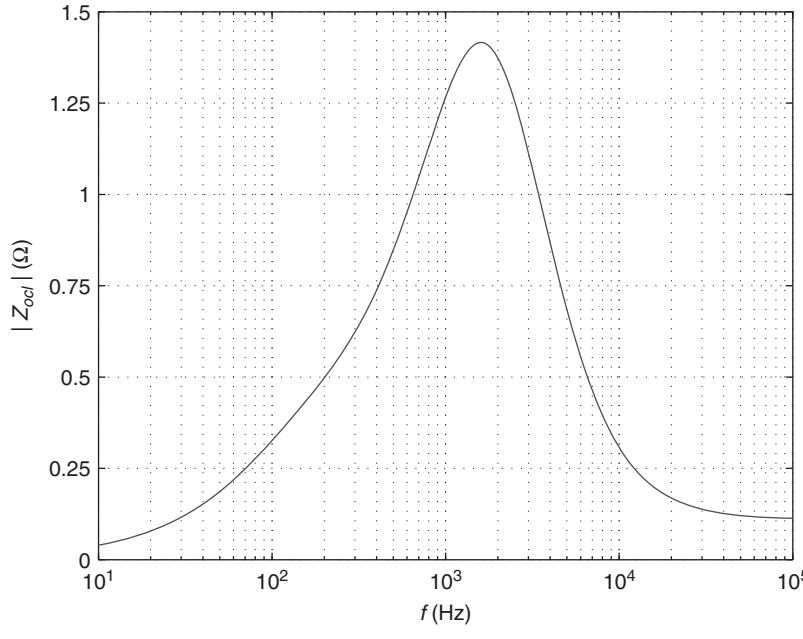


Figure 12.29 Plot of the phase of the closed-loop output impedance Z_{ocl} versus frequency for the boost converter.

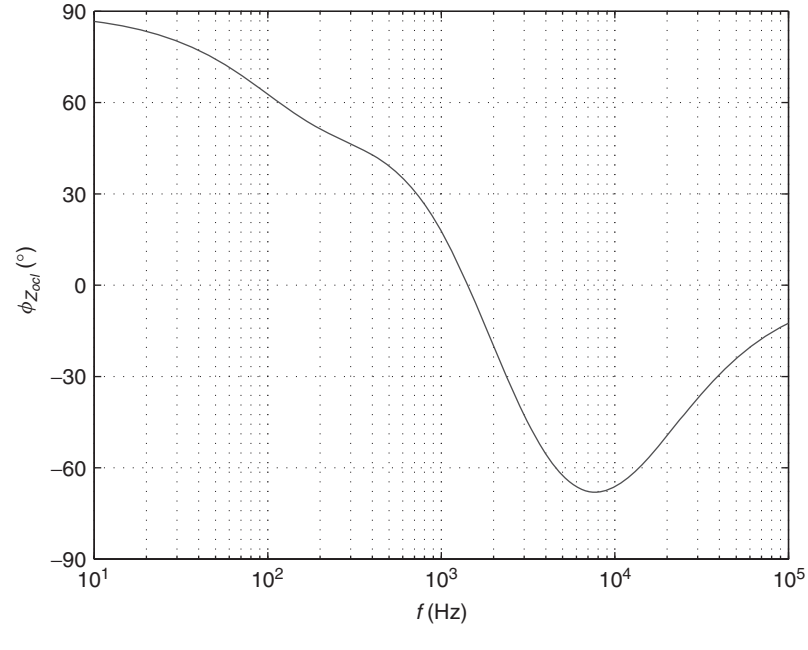


Figure 12.30 Plot of the phase of the closed-loop output impedance Z_{ocl} versus frequency for the boost converter.

0.111 Ω, $R_{Lmin} = 40\,\Omega$, $R_1 = 100\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $R_3 = 2.2\,\text{k}\Omega$, $C_1 = 5\,\text{nF}$, $C_2 = 0.15\,\text{nF}$, $C_3 = 5\,\text{nF}$. Calculate $R_{icl}(0)$. Draw the plots for the closed-loop output impedance Z_{ocl} versus frequency for the boost converter for $D = 0.4$, 0.5, and 0.6.

Solution. Figures 12.29 and 12.30 show the plots of Z_{ocl} for the boost converter.

12.13 Closed-loop Step Responses

12.13.1 Closed-loop Response to Step Change in Input Voltage

Assume that a step change in the input voltage is ΔV_I at time $t = 0$ and the steady-state input voltage before the step change is $V_I(0^-)$. Therefore, the total input voltage is given by

$$v_I(t) = V_I(0^-) + \Delta V_I u(t), \tag{12.133}$$

which results in a step change in the input voltage in the time domain,

$$v_i(t) = v_I(t) - V_I(0^-) = \Delta V_I u(t), \tag{12.134}$$

and in the s-domain,

$$v_i(s) = \frac{\Delta V_I}{s}. \tag{12.135}$$

Hence, one obtains the transient component of the output voltage in the s-domain,

$$v_o(s) = M_{vcl}(s)v_i(s) = \frac{\Delta V_I M_{vcl}(s)}{s} = \frac{\Delta V_I M_v(s)}{s[1 + T(s)]}, \tag{12.136}$$

the transient component of the output voltage,

$$v_o(t) = \mathcal{L}^{-1}\{v_o(s)\}, \tag{12.137}$$

and the total output voltage

$$v_O(t) = V_O(0^-) + v_o(t). \tag{12.138}$$

Example 12.8

Draw the waveform of the total output voltage $v_O(t)$ of the closed-loop boost converter of Example 12.1 as a response to the step change in the input voltage from 12 to 13 V. Find the maximum relative transient ripple of the total output voltage v_O.

Solution. Figure 12.31 shows a step response of the output voltage v_O to a step change in the input voltage v_I from 12 to 13 V for the boost converter with negative feedback at $\beta = 0.125$, $V_{Tm} = 5\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $R_{Lmin} = 40\,\Omega$, $R_1 = 100\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $C_1 = 5\,\text{nF}$, $C_2 = 0.15\,\text{nF}$, $C_3 = 5\,\text{nF}$, and $D = 0.5$. The output voltage increases from 20 to 20.63 V and then returns to $V_O = 20\,\text{V}$ after 6 ms. The maximum relative transient ripple of the output voltage is

$$\delta_{max} = \frac{v_{Omax} - v_O(\infty)}{v_O(\infty)} = \frac{20.63 - 20}{20} = \frac{0.63}{20} = 3.15\,\%. \tag{12.139}$$

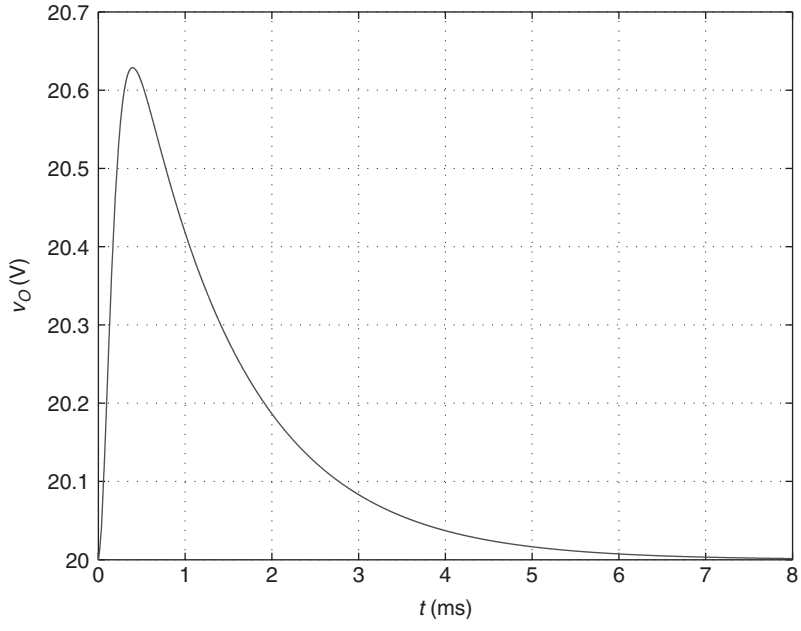


Figure 12.31 Response of v_O to the step change in input voltage v_I from 12 to 13 V for the boost converter with negative feedback.

12.13.2 Closed-loop Response to Step Change in Reference Voltage

Assume that a step change in the reference voltage is ΔV_R at time $t = 0$ and the reference voltage is $V_R(0^-)$. The total reference voltage can be described by

$$v_R(t) = V_R(0^-) + \Delta V_R u(t). \tag{12.140}$$

Hence, the ac component of the reference voltage in the time domain is

$$v_r(t) = v_R(t) - V_R(0^-) = \Delta V_R u(t), \tag{12.141}$$

and in the s-domain is

$$v_r(s) = \frac{\Delta V_R}{s}. \tag{12.142}$$

The transient component of the output voltage in the s-domain can be expressed as

$$v_o(s) = T_{pcl}(s)v_r(s) = \frac{\Delta V_R T_{cl}(s)}{s} = \frac{\Delta V_R A(s)}{s[1 + T(s)]}. \tag{12.143}$$

The inverse Laplace transform of $v_o(s)$ produces the transient component of the output voltage,

$$v_o(t) = \mathcal{L}^{-1}\{v_o(s)\}, \tag{12.144}$$

and the total output voltage

$$v_O(t) = V_O(0^-) + v_o(t). \tag{12.145}$$

Example 12.9

Draw the total output voltage $v_O(t)$ of the closed-loop boost converter of Example 12.1 as a response to the step change in the reference voltage v_R from 2.5 to 3 V. Find the maximum overshoot and the maximum transient ripple. Also, calculate the increase in the steady-state output voltage.

Solution. Figure 12.32 shows the step response of the output voltage v_O to the step change in the reference voltage v_R from 2.5 to 3 V, which corresponds to a step change in the ac component of the reference voltage v_r from 0 to 0.5 V at $D = 0.5$ for the boost converter with negative feedback. The total output voltage v_O initially decreases from 20 V to 19.8 V, then increases to 23.8 V, decreases again, and finally reaches a steady-state value of 24 V after 5 ms. Notice that output voltage initially decreases because of the presence of the RHP zero in the transfer function T_{cl}. The peak value of v_O is lower than the steady-state value. Therefore, the overshoot can be considered to be zero.

At the reference voltage $V_R = 2.5$ V and the output voltage $V_O = 20$ V, the closed-loop control-to-output voltage transfer function should be

$$T_{clo} = T_{cl}(0) = \frac{V_O}{V_R} = \frac{20}{2.5} = 8 = 18.062 \text{ dB}. \tag{12.146}$$

The increase of the reference voltage V_R from 2.5 to 3 V causes the output voltage V_O to increase to

$$V_O = T_{clo} V_R = 8 \times 3 = 24 \text{ V} \tag{12.147}$$

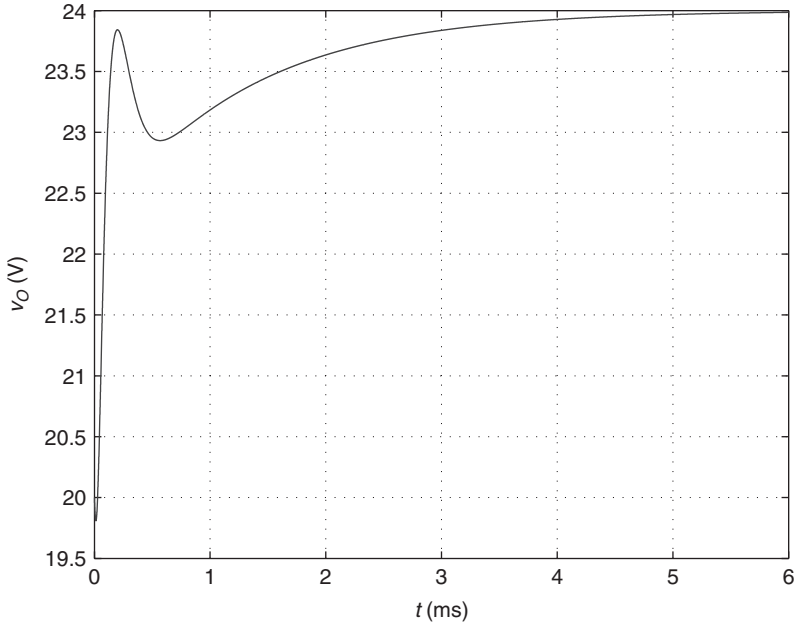


Figure 12.32 Response of v_O to the step change in reference voltage v_R from 2.5 to 3 V for the boost converter with negative feedback.

or

$$V_O = T_{clo} V_R \approx \frac{V_R}{\beta} = \frac{3}{0.125} = 24\,\text{V}. \tag{12.148}$$

Thus, the increase in the steady-state output voltage is

$$\Delta V_O = T_{clo} \Delta V_R = 8 \times 0.5 = 4\,\text{V}. \tag{12.149}$$

The dc output voltage V_O increases from 20 V to approximately 24 V.

12.13.3 Closed-loop Response to Step Change in Load Current

The load current contains a step change ΔI_O at $t = 0$ and is described by

$$i_O(t) = I_O(0^-) + \Delta I_O u(t). \tag{12.150}$$

Hence, the small-signal step change in the load current is

$$i_o(t) = i_O(t) - I_O(0^-) = \Delta I_O u(t), \tag{12.151}$$

which gives

$$i_o(s) = \frac{\Delta I_O}{s}. \tag{12.152}$$

Therefore, the transient component of the output voltage is given by

$$v_o(t) = -Z_{ocl}(s) i_o(s) = \frac{\Delta I_O R_L r_C}{R_L + r_C} \times \frac{s(s + \omega_{pc})^2 (s + \omega_{zn})(s + \omega_{rl})}{s^2 (s + \omega_{pc})^2 (s^2 + 2\xi\omega_0 s + \omega_0^2) + T_x s (s + \omega_{zc})^2 (s + \omega_{zn})(s - \omega_{zp})}. \tag{12.153}$$

Example 12.10

Draw the waveform of the total output voltage $v_O(t)$ of the closed-loop boost converter of Example 12.1 as a response to the step change in the load current i_O from 0.5 to 0.6 A. Find the maximum relative transient ripple of the total output voltage v_O.

Solution. Figure 12.33 shows a step response of the output voltage v_O to the step change in the load current i_O from 0.5 to 0.6 A for the boost converter with negative feedback at $\beta = 0.125$, $V_{Tm} = 5\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $R_{Lmin} = 40\,\Omega$, $R_1 = 100\,\text{k}\Omega$, $R_2 = 100\,\text{k}\Omega$, $C_1 = 5\,\text{nF}$, $C_2 = 0.15\,\text{nF}$, $C_3 = 5\,\text{nF}$, and $D = 0.5$. The output voltage decreases from 20 to 19.893 V and then returns to $V_O = 20\,\text{V}$ after 5 ms. The maximum relative transient ripple of the output voltage is

$$\delta_{max} = \frac{|v_{Omin} - v_O(\infty)|}{v_O(\infty)} = \frac{|19.893 - 20|}{20} = \frac{0.107}{20} = 0.535\,\%. \tag{12.154}$$

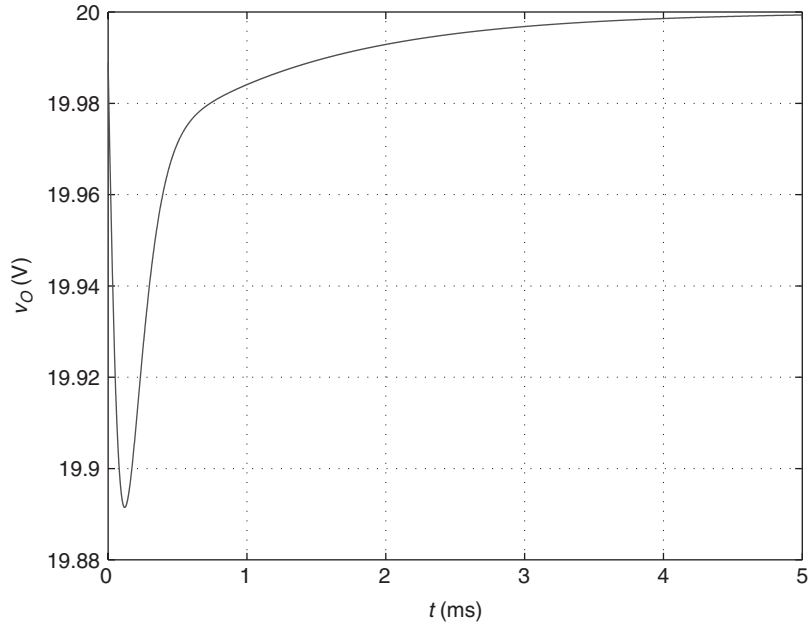


Figure 12.33 Response of v_O to the step change in load current i_O from 0.5 to 0.6 A for the boost converter with negative feedback.

12.14 Closed-loop DC Transfer Functions

The dc voltage transfer function of the forward path is

$$A_o = A(0) = \frac{V_O}{V_E} = T_{co}T_mT_{po}, \tag{12.155}$$

where $T_{co} = T_c(0)$ is the dc gain of the control circuit. The dc loop gain is expressed by

$$T_o = T(0) = \frac{V_F}{V_E} = \beta A_o = \beta T_{co}T_mT_{po}. \tag{12.156}$$

The dc closed-loop control-to-output voltage gain is

$$T_{clo} = T_{cl}(0) = \frac{V_O}{V_R} = \frac{A_o}{1 + \beta A_o}. \tag{12.157}$$

If $\beta A_o \gg 1$, then

$$T_{clo} = \frac{A_o}{1 + \beta A_o} \approx \frac{1}{\beta}, \tag{12.158}$$

and the dc output voltage is

$$V_O = T_{clo}V_R \approx \frac{V_R}{\beta}. \tag{12.159}$$

To ensure that the dc output voltage V_O remains constant and equal to a desired value, the loop gain βA_o must be very high and the feedback network voltage transfer function β and the reference voltage V_R must be accurate. An accurate value of β is achieved by using precision resistors (e.g., 1 %).

The dc closed-loop audio susceptibility is

$$M_{vclo} = \frac{M_{vo}}{1 + \beta A_o}, \tag{12.160}$$

and the dc closed-loop output resistance is

$$R_{oclo} = R_{ocl}(0) = \frac{R_o}{1 + \beta A_o}. \tag{12.161}$$

Example 12.11

For the boost converter given in Example 12.1, calculate T_{clo}, V_O, V_E, Z_{oclo}, and M_{vclo} if $T_{co} = 1000$, $T_{po} = 37.55$, $\beta = 1/8$, $V_{Tm} = 5\,\text{V}$, $M_{vo} = 1.939$, and $Z_{oo} = 1.225\,\Omega$.

Solution. The dc voltage transfer function of the forward path is

$$A_o = A(0) = T_{co}T_mT_{po} = 1000 \times \tfrac{1}{5} \times 37.55 = 7510. \tag{12.162}$$

The dc loop gain is

$$T_o = T(0) = \beta A_o = \tfrac{1}{8} \times 7510 = 938.75 = 59.45\,\text{dB}. \tag{12.163}$$

The dc closed-loop control-to-output gain is

$$T_{clo} = \frac{A_o}{1 + \beta A_o} = \frac{7510}{1 + 938.75} = 7.9915 = 18\,\text{dB}. \tag{12.164}$$

The dc output voltage is

$$V_O = T_{clo}V_R = 7.9915 \times 2.5 = 19.9787\,\text{V}, \tag{12.165}$$

the dc feedback voltage is

$$V_F = \beta V_O = 0.125 \times 19.9787 = 2.4973\,\text{V}, \tag{12.166}$$

and the dc error voltage is

$$V_E = V_R - V_F = 2.5 - 2.4973 = 2.7\,\text{mV}. \tag{12.167}$$

The dc closed-loop output impedance is

$$R_{oclo} = \frac{Z_{oo}}{1 + \beta A_o} = \frac{1.225}{1 + 938.75} = 1.3\,\text{m}\Omega. \tag{12.168}$$

The dc closed-loop input-to-output voltage transfer function is

$$M_{vclo} = \frac{M_{vo}}{1 + \beta A_o} = \frac{1.939}{1 + 938.75} = 2.0633 \times 10^{-3} = -53.7\,\text{dB}. \tag{12.169}$$

12.15 Summary

- The closed-loop boost converter consists of a feedback network, a control circuit, a pulse-width modulator, and a boost converter power stage.
- It is difficult to achieve good phase and gain margins of the boost converter because of the RHP zero.

- Negative feedback reduces the magnitude of the audio susceptibility by a factor of $|1 + T|$.
- The dc input resistance of the closed-loop boost converter is negative.
- Negative feedback reduces the magnitude of the output impedance by a factor of $|1 + T|$.

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12.17 Review Questions

12.1. Draw the boost converter along with other stages that form a single-loop negative feedback control circuit.

12.2. Draw a single-loop control circuit for the boost converter with the feedback network replaced by *h*-parameters.

12.3. Draw a single-loop control circuit for the boost converter with the resistances of the feedback network moved to the *A*-circuit.

12.4. Is it easy to ensure the stability of the boost converter?

12.5. What is the effect of negative feedback on the audio susceptibility?

12.6. What is the effect of negative feedback on the input impedance?

12.7. What is the effect of negative feedback on the output impedance?

12.18 Problems

12.1. A pulse-width modulator has a ramp output voltage with a peak value $V_{Tm} = 5\,\text{V}$. Find a transfer function of the modulator.

12.2. A boost PWM converter has $V_{Inom} = 156\,\text{V}$, $D_{nom} = 0.65$, and the pulse-width modulator $V_{Tm} = 5\,\text{V}$. Determine the dc reference voltage for a control circuit.

12.3. A boost PWM converter has $V_O = 400\,\text{V}$ and the reference voltage is $V_R = 3.25\,\text{V}$. Design a feedback network.

12.4. A boost PWM converter has $T_{po} = 1114.27\,\text{V}$, a feedback network has $\beta = 1/123$, and a pulse-width modulator has $T_m = 0.2\,\text{V}^{-1}$. Determine the overall voltage transfer function T_{ko} of the three stages at $f = 0$.

12.5. A boost PWM converter has $V_I = 156\,\text{V}$, $V_O = 400\,\text{V}$, $V_R = 3.25\,\text{V}$, $T_{ko} = 1.8118$, $\xi = 0.162$, $f_{zn} = 159\,\text{kHz}$, $f_{zp} = 1.17\,\text{kHz}$, and $f_0 = 322\,\text{Hz}$. Design a control circuit such that $PM \geq 55^\circ$.

12.6. The transfer function of the feedback network in a boost converter is $\beta = 1/123$. Find the value of the closed-loop control-to-input voltage transfer function at $f = 0$.

12.7. A closed-loop boost converter has $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $R_{Lmax} = 17.78\,\text{k}\Omega$, and $r = 2.756\,\Omega$. Find the values of the dc closed-loop input resistance at R_{Lmin} and R_{Lmax}.

13

Current-mode Control

13.1 Introduction

Voltage-mode control, also called duty-cycle control, contains a *single loop* and adjusts the duty cycle directly in response to output voltage changes. *Current-mode control* [1]–[56], also called *current-programmed mode* or *current-injected control*, is a *multiple-loop* control method that contains two loops: an *inner current loop* and an *outer voltage loop*. The current loop controls the inductor peak current, while the voltage loop controls the output voltage. The technique is called current-mode control because the inductor current is directly controlled, whereas the output voltage is controlled only indirectly by the current loop. The inductor peak current is close to the inductor average current. The inductor average current is related to the load current. In buck and buck-derived converters, the load current is equal to the average current. In the boost converter (often used as a power-factor corrector), the average input current is equal to the average inductor current. The inner current loop initially adjusts the duty cycle in response to the changes in inductor current, and the outer voltage loop produces a reference voltage for the current loop in response to the changes in the converter output voltage. The duty cycle is determined by the time instants at which the inductor or switch current reaches a threshold level determined by a control signal. This threshold level becomes the input to the inner loop. The key feature of current-mode control is that the inner loop changes the inductor into a voltage-dependent current source at frequencies lower than the crossover frequency of the current loop. The action of the current loop is similar to that of a sample-and-hold circuit, which is a nonlinear, time-varying system.

There are seven known types of current-mode control methods. They, in turn, fall into two categories: *constant-frequency* and *variable-frequency* control methods. In the first group, the switching frequency is constant and synchronized to a clock signal $f_s = f_{CLK}$. This group contains *peak-current-mode control*, *valley-current-mode control*, *PWM conductance control with triangle-wave compensation*, and *average-current-mode control*. The second group contains self-oscillating converters, including *constant on-time*, *constant off-time*,

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and *hysteretic* methods. The most popular method is *fixed-frequency peak-current-mode control* with fixed-slope compensation ramp.

In this chapter, we shall study in detail the principle of operation of peak-current-mode control, stability of the current loop, slope compensation, small-signal current-modulator model, the block diagram of PWM converters with current-mode control, and key characteristics of current-mode-controlled converters. Current-mode control can also be used in constant-current dc–dc converters.

13.2 Principle of Operation of PWM Converters with Peak-current-mode Control

Circuits of the PWM buck, boost, and buck-boost converters with *fixed-frequency peak-current-mode control* are shown in Figures 13.1, 13.2, and 13.3, respectively. Each circuit contains two loops: an inner current loop and an outer voltage loop. The inner current loop contains an op-amp voltage comparator, a set–reset latch, a clock *CLK*, and a current sensor, for example, a current transformer or a noninductive sense resistor R_s, which senses the inductor current i_L or the switch current i_S. In general, R_s represents the transfer function from the inductor or switch current to the current sensor output voltage. It may be a transfer function of a current transformer, which has corner frequencies in the low-frequency and high-frequency ranges. The latch S input sets (or presets) the Q output to 1, and the latch R input resets (or clears) the Q output to 0. The op-amp comparator, the set–reset latch, and the clock CLK form an inductor current modulator. The analog control voltage v_C is applied to the comparator inverting input, and the voltage $R_s i_L$ (proportional to the inductor current i_L) or the voltage $R_s i_S$ (proportional to the switch current i_S) is applied to the comparator noninverting input.

If a noninductive resistor R_s is connected between the comparator inverting input and ground (as shown in Figure 13.1), the current through the resistor R_s is $i_C = v_C/R_s$. This

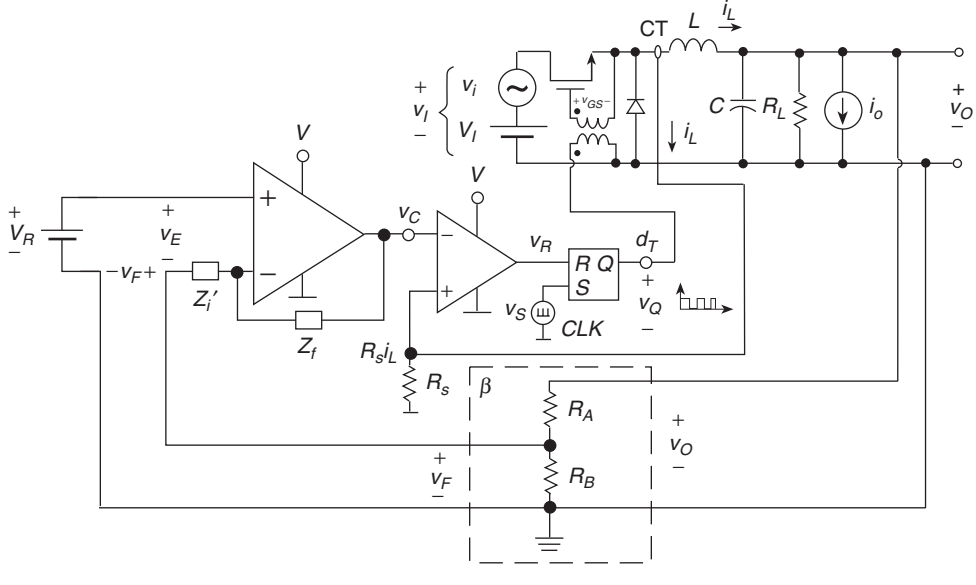


Figure 13.1 Circuit of a PWM buck converter with peak-current-mode control.

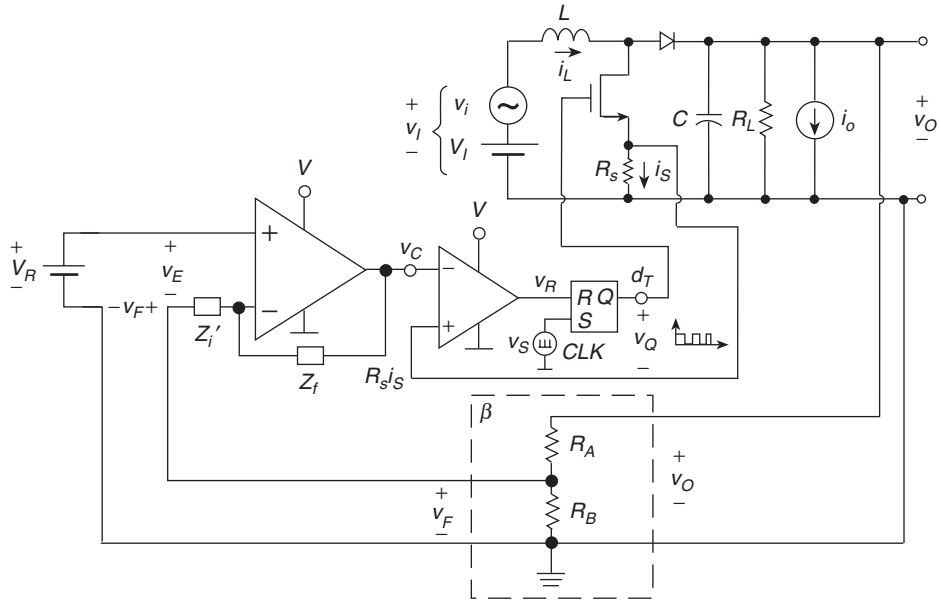


Figure 13.2 Circuit of a PWM boost converter with peak-current-mode control.

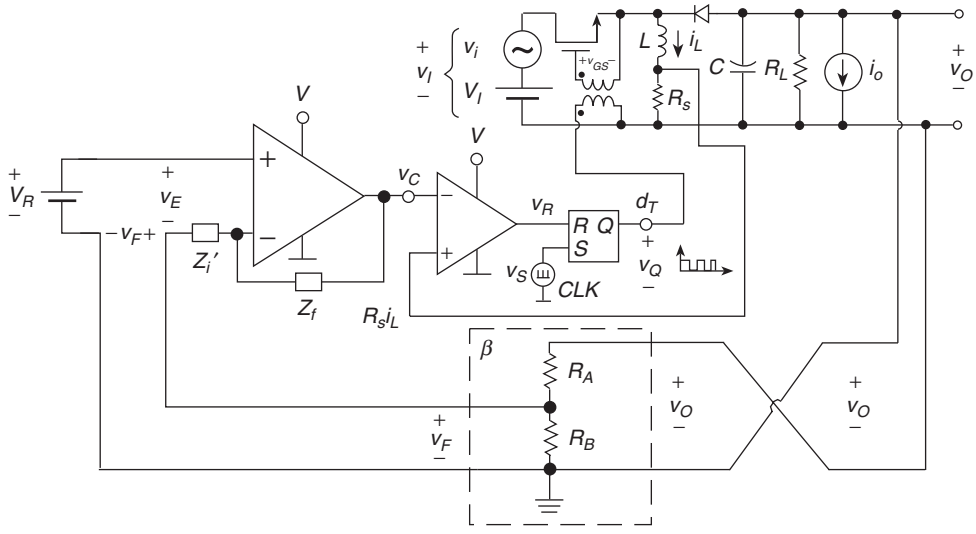


Figure 13.3 Circuit of a PWM buck-boost converter with peak-current-mode control.

current can be regarded as a control current (or a reference current) for the inner current loop.

Figure 13.4 depicts the waveforms, explaining the principle of operation of PWM converters with current-mode control. The clock generates voltage pulses at a constant clock frequency f_{CLK} equal to the switching frequency $f_s = 1/T_s$. When the clock output voltage $v_{CLK} = v_S$ goes high, the latch Q output v_Q goes high (i.e., it sets the Q output to 1). Therefore, the gate-to-source voltage v_{GS} also goes high, turning the switch on. This event

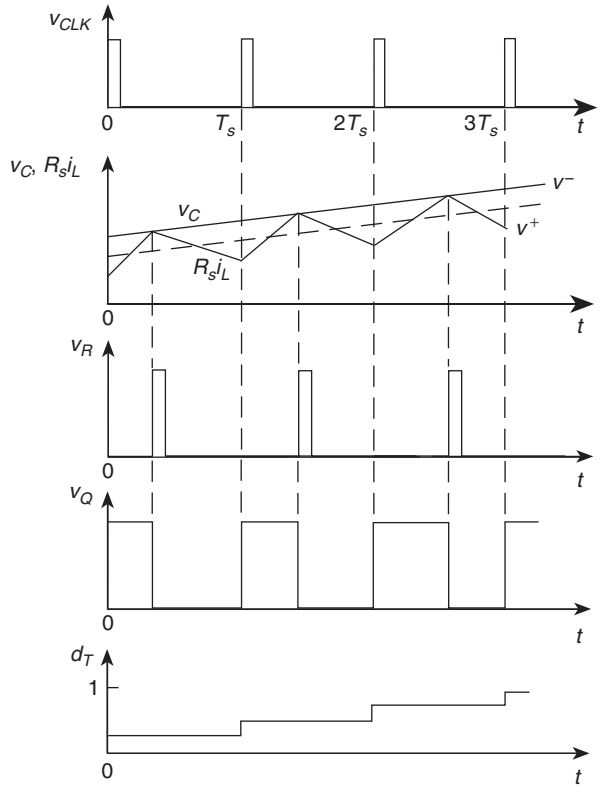


Figure 13.4 Waveforms of PWM converters with constant-frequency, trailing-edge modulation, peak-current-mode control.

initiates the transistor on-time and starts the cycle T_s of the switching frequency f_s. Since the turn-on times are periodically clocked, a constant-frequency operation is obtained. While the switch is on, the inductor current i_L and the switch current i_S increase linearly. The inductor current i_L, or the switch current i_S, is sensed by a current probe. The currents i_L and i_S are equal during the transistor on-time. The sensed inductor current i_L (or the switch current i_S) flows through the resistor R_s and develops a voltage $R_s i_L$. When the voltage $R_s i_L = v^+$ is lower than the control voltage $v_C = v^-$, the comparator output voltage v_R is low. When the voltage $R_s i_L$ reaches the control voltage v_C, the comparator output voltage v_R goes high, resetting the latch Q output to 0. Therefore, the gate-to-source voltage v_{GS} goes low, turning the switch off for the remaining time of the switching period. As a result, the inductor current i_L decreases. Since $R_s i_L < v_C$, the comparator output voltage v_R goes low. In summary, the clock sets the latch and turns the transistor on at the beginning of the cycle T_s. The comparator resets the latch and turns the transistor off when the inductor current i_L reaches the control current i_C. Consequently, the peak inductor current I_{Lpk} and the peak switch current I_{Spk} follow the control current $i_C = v_C/R_s$. Thus, amplitude modulation of the inductor current i_L takes place, where the control current i_C or the control voltage v_C is the modulating signal. The average inductor current is

$$I_L \approx I_{Lpk} - \frac{\Delta i_L}{2}. \tag{13.1}$$

Since the peak inductor current is directly controlled, this method is called *peak-current-mode control*. It can be regarded as an amplitude modulation of the inductor current by

the control current. The inner current loop is capable of responding very rapidly to control voltage (or control current) changes on a *cycle-by-cycle* or *pulse-by-pulse* basis. This control strategy is referred to as *constant-frequency trailing-edge modulation peak-current-mode control* or *constant-frequency peak-current-mode on-time control* because a fixed-frequency clock signal is used to turn on the switch, and the intersection of the voltage $R_s i_L$ (proportional to the inductor current i_L) with the control voltage v_C is used to turn the switch off. In other words, the clock initiates the on-time interval t_{on} and the control voltage initiates the off-time interval t_{off}. Thus, the switch on-time is controlled at a fixed frequency. This method requires inductor current information during the switch on-time. The average value of the inductor current is lower than the peak value of the inductor current by one-half of the inductor peak-to-peak current ripple Δi_L; therefore, the average inductor current is controlled indirectly. The outer voltage loop senses the output voltage and develops a control voltage v_C, which serves as a reference voltage for the inner current loop; thus, the outer voltage loop adjusts the control voltage v_C. The inductor current is fed back through a sensing resistor R_s and the resulting voltage $R_s i_L$ is compared with the control voltage v_C. The output voltage is fed back through a resistive voltage divider $R_A - R_B$, is compared with the reference voltage V_R, and sets the control voltage v_C. The input to the current loop is the control voltage v_C, which is compared to the sensed inductor current i_L (or voltage $R_s i_L$) and sets the duty cycle. In turn, the duty cycle produces a corresponding inductor current and output voltage. As a first-order approximation, the current loop causes the inductor to act like a voltage-controlled (or current-controlled) current source v_C / R_s.

A dual modulation strategy uses a constant-frequency clock signal to turn the transistor off and the intersection of the inductor or diode current to turn the transistor on; thus, the switch off-time is controlled at fixed frequency. This control strategy is referred to as a *constant-frequency leading-edge modulation valley current-mode control* or *constant-frequency valley current-mode off-time control*. There are also three variable-frequency modulation strategies. The first is *constant on-time control*, the second is *constant off-time control*, and the third is *hysteretic control*. In hysteretic control, the inductor current waveform is used to turn the switch on and off, resulting in free-running operation. In addition to current-mode control based on instantaneous inductor current, there is also an average current-mode control method, where inductor current waveform is integrated by a low-pass filter placed at the output of the sense resistor R_s. The advantage of this method is the ability to directly control the average inductor current and increase the noise immunity. The constant-frequency trailing-edge modulation control strategy is the most widely used in practice, with a large number of control ICs in the market, and therefore is studied here in detail.

Current-mode control exhibits a feedforward control feature. When the converter input voltage V_I is increased, the slope of the rising inductor current also increases. Therefore, the switch turns off sooner, yielding nearly constant volt-second balance and making the converter output voltage V_O less dependent on the input voltage V_I.

In general, basic PWM converters (buck, boost, and buck-boost) are second-order systems, in which one state variable is the inductor current and the other state variable is the capacitor voltage (which is approximately equal to the output voltage). The converter dynamic performance can be improved by controlling both state variables. When current-mode control is used, the reference signal for the inner loop and the inductor current depends on the converter output voltage. As a result, one variable controls the other. Consequently, there is only one true state variable (i.e., the capacitor voltage), resulting in a system that behaves approximately as a first-order system.

Current-mode control offers several advantages over voltage-mode control. Firstly, if the maximum value of the control current i_C is limited, then the maximum value of switch

current i_S is also limited. Since the inductor peak current is approximately equal to the inductor average current, which in turn is related to the load current, the output current can be limited simply by clamping the control voltage. The transistor turns off whenever its current becomes too high. Therefore, transistor and diode failures due to excessive currents can be prevented and the load current can be held below a predetermined maximum level. Thus, current-mode control inherently provides a fast pulse-by-pulse short circuit and overcurrent load protection, enhancing the converter reliability. In addition, the transient peak values of the inductor, switch, and diode currents are limited. A Zener diode may be connected between the comparator noninverting input and ground to limit the maximum value of the control voltage. Secondly, it is easy to connect power converters with current-mode control in parallel in order to increase current capability and/or redundancy without load current-sharing problems. This is because the output current of each unit is determined by the control signal. If all units receive the same control signal, then all of them will deliver the same amount of current. Thirdly, current-mode control is a perfect solution to transformer imbalance in symmetrical converters, such as full-bridge and push-pull converters. The imbalance may be caused by the volt-second differences between the positive and negative pulses applied to the transformer. A series capacitor, which is usually used in full-bridge converters to remedy the transformer imbalance, should be removed if current-mode control is used.

A disadvantage of peak-current-mode control is its inherent instability of the inner current loop when $D > 0.5$, resulting in subharmonic oscillations. For a duty ratio greater than 0.5, slope compensation is required. Moreover, this control scheme is susceptible to noise, especially when the inductor ripple is small. This noise may corrupt the control voltage, the inductor current or switch current, generating a false signal for the noninverting comparator input. Current spikes caused by the diode reverse recovery may have a detrimental effect. The current-mode control scheme requires a current sensor, which is usually a resistor R_s connected in series with the inductor L or the MOSFET source. Current flow through this resistor causes power loss. In addition, the sense resistor connected in series with the MOSFET source causes a degradation of the transistor current capability and may require a larger transistor size [46].

In the average-current-mode control [8]–[43], the inductor current is sensed and fed to a two-pole and one-zero compensation network, which averages the inductor current. Consequently, the average inductor current follows the control reference current. The advantage of this control scheme is good immunity of a converter to switching noise because the average current is sensed. In addition, there is no need for slope compensation.

With charge control [44], the inductor current is sensed and used to charge a capacitor. The capacitor voltage is compared to a control voltage, which represents the current to be controlled. As soon as the capacitor voltage reaches the control voltage, the active switch is turned off and the capacitor is quickly discharged to zero by an auxiliary switch connected in parallel with the capacitor. In this technique, the inductor current is indirectly controlled by regulating the peak capacitor voltage, which is proportional to the integral of the inductor current within one cycle. The advantage of this control scheme is good noise immunity due to integration of the inductor current.

13.3 Relationship between Duty Cycle and Inductor-current Slopes

Let us assume that a PWM converter is operated in steady state with constant input voltage V_I, output voltage V_O, load resistance R_L, and duty cycle D. Figure 13.5 shows the inductor

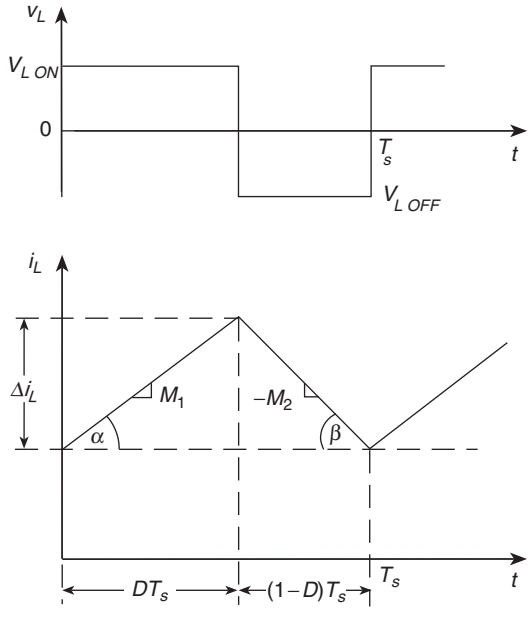


Figure 13.5 Steady-state waveforms of the inductor voltage and current in PWM converters for CCM.

voltage and current waveforms under these conditions for CCM. The rising and falling slopes of the inductor current waveform are

$$M_1 = \tan\alpha = \frac{\Delta i_L}{DT_s} \tag{13.2}$$

and

$$M_2 = \tan\beta = \frac{\Delta i_L}{(1-D)T_s}. \tag{13.3}$$

Hence, the ratio of the absolute values of the inductor-current slopes for all basic PWM converters in steady state is given by

$$\frac{M_2}{M_1} = \frac{D}{1-D}. \tag{13.4}$$

Hence, the on-time slope M_1 is equal to the off-time slope M_2 at $D = 0.5$, $M_2 < M_1$ for $D < 0.5$, and $M_2 > M_1$ for $D > 0.5$.

In general, the rising and falling slopes of the inductor current are

$$M_1 = \frac{V_{L\,ON}}{L} \tag{13.5}$$

and

$$M_2 = \frac{V_{L\,OFF}}{L}. \tag{13.6}$$

For the buck converter,

$$M_1 = \frac{V_I - V_O}{L} \tag{13.7}$$

and

$$M_2 = \frac{V_O}{L}. \tag{13.8}$$

For the boost converter,

$$M_1 = \frac{V_I}{L} \tag{13.9}$$

and

$$M_2 = -\frac{V_I - V_O}{L}. \tag{13.10}$$

For the buck-boost converter,

$$M_1 = \frac{V_I}{L} \tag{13.11}$$

and

$$M_2 = \frac{V_O}{L}. \tag{13.12}$$

13.4 Instability of Closed-current Loop

Consider a PWM converter with constant-frequency, trailing-edge modulation, peak-current-mode control operated in CCM, in which the inner current loop is closed and the outer voltage loop is open. Assume that there is a small perturbation in $i_L(0)$. Figure 13.6 shows two inductor current waveforms: one for steady state and the other after a small perturbation $|\Delta i_{L0}|$ at the beginning of the transistor on-time interval at $t = 0$. The perturbation causes a series of changes in the inductor current Δi_{Ln} from the steady-state waveform in successive cycles in the form of a *geometric progression* whose *common ratio* is $r_p = \Delta i_{Ln}/\Delta i_{L(n-1)} = -D/(1-D)$. Each new term is equal to the previous term multiplied by the factor $r_p = -D/(1-D)$, and its magnitude may decrease, remain constant, or increase with time.

Initially assume the input voltage V_I and the output voltage V_O are constant, that is, their ac components are zero. Therefore, the slopes of the inductor current waveform $M_1 =$

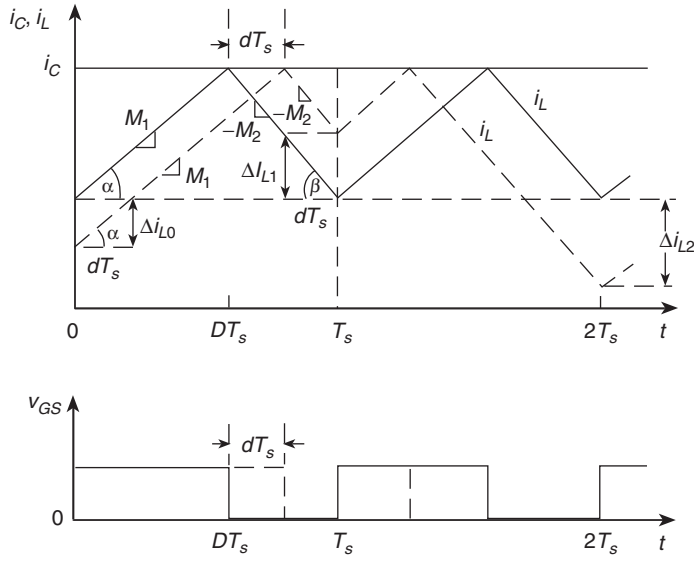


Figure 13.6 Steady-state and perturbed (transient) waveforms of inductor current in PWM converters with current-mode control in CCM.

$V_{L\,ON}/L$ and $M_2 = V_{L\,OFF}/L$ are also constant, where $V_{L\,ON}$ and $V_{L\,OFF}$ are the voltages across the inductor during the transistor on-time and off-time intervals, respectively. These slopes are obtained from geometric considerations as

$$M_1 = \tan\alpha = \frac{|\Delta i_{L0}|}{dT_s} \tag{13.13}$$

and

$$M_2 = \tan\beta = \frac{|\Delta i_{L1}|}{dT_s}, \tag{13.14}$$

where $|\Delta i_{L0}|$ is the absolute value (or magnitude) of the inductor current change at $t = 0$ and $|\Delta i_{L1}|$ is the absolute value of the inductor current change at $t = T_s$. Using (13.4), (13.13), and (13.14), one obtains the ratio of the inductor current change after one cycle $|\Delta i_{L1}|$ to the inductor current change at the beginning of the cycle $|\Delta i_{L0}|$,

$$a = a_{i1} = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_2}{M_1} = \frac{D}{1-D}. \tag{13.15}$$

The ratio of the inductor current change after two cycles Δi_{L2} to the initial inductor current change Δi_{L0} is

$$a_{i2} = \frac{|\Delta i_{L2}|}{|\Delta i_{L0}|} = \frac{|\Delta i_{L2}|}{|\Delta i_{L1}|} \times \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \left(\frac{M_2}{M_1}\right)^2 = \left(\frac{D}{1-D}\right)^2, \tag{13.16}$$

and the ratio after n cycles is

$$a_{in} = \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \left(\frac{M_2}{M_1}\right)^n = \left(\frac{D}{1-D}\right)^n, \tag{13.17}$$

where $a = a_{i2}/a_{i1} = a_{in}/a_{in-1}$. Hence,

$$\lim_{n\to\infty} a_{in} = \lim_{n\to\infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n\to\infty} \left(\frac{D}{1-D}\right)^n = 0, \qquad \text{for } D < 0.5 \tag{13.18}$$

$$\lim_{n\to\infty} a_{in} = \lim_{n\to\infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n\to\infty} \left(\frac{D}{1-D}\right)^n = 1, \qquad \text{for } D = 0.5 \tag{13.19}$$

and

$$\lim_{n\to\infty} a_{in} = \lim_{n\to\infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n\to\infty} \left(\frac{D}{1-D}\right)^n = \infty, \qquad \text{for } D > 0.5. \tag{13.20}$$

Equation (13.15) has the following consequences:

1. The inner current loop is stable if

$$a = a_{i1} = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_2}{M_1} = \frac{D}{1-D} < 1, \tag{13.21}$$

which occurs for

$$M_1 > M_2. \tag{13.22}$$

The condition of stability of the inner current loop is satisfied for $D < 0.5$. In this case, $|\Delta i_{L1}| < |\Delta i_{L0}|$, the perturbation magnitude $|\Delta i_{Ln}|$ decays with time to zero as n approaches infinity, and the converter returns to its initial state.

2. The inner current loop is marginally stable if

$$a = a_{i1} = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_2}{M_1} = \frac{D}{1-D} = 1, \tag{13.23}$$

which occurs for

$$M_1 = M_2. \tag{13.24}$$

This condition is satisfied at $D = 0.5$, for which $|\Delta i_{Ln}| = |\Delta i_{L0}|$, that is, the magnitude of oscillations remains constant, and the converter does not return to its initial state.

3. The inner current loop is unstable if

$$a_{i1} = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_2}{M_1} = \frac{D}{1-D} > 1, \tag{13.25}$$

which occurs for

$$M_1 < M_2. \tag{13.26}$$

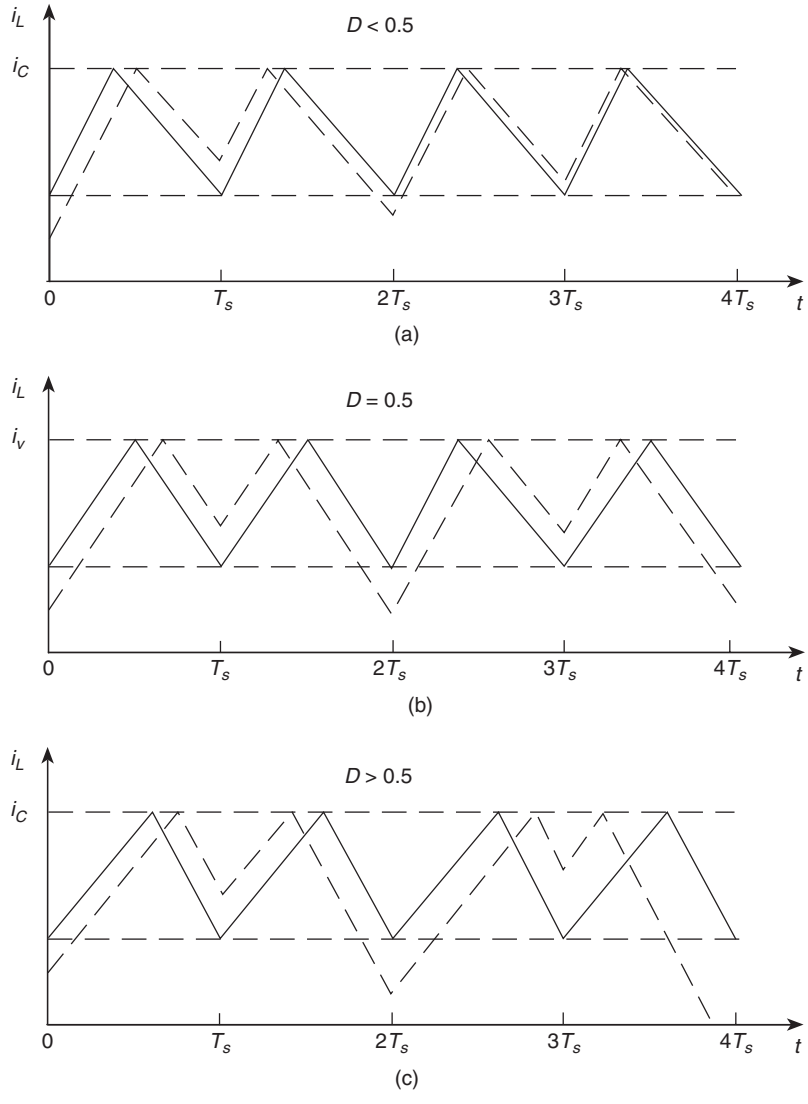


Figure 13.7 Steady-state (solid line) and perturbed (dashed line) waveforms of inductor current i_L for PWM converters with current-mode control. (a) For a stable current loop ($D < 0.5$). (b) For a marginally stable current loop ($D = 0.5$). (c) For an unstable current loop ($D > 0.5$).

The instability condition of the inner current loop is satisfied for $D > 0.5$. In this case, $|\Delta i_{L1}| > |\Delta i_{L0}|$, the magnitude of oscillations increases with time, and the converter does not return to its initial state. This leads to subharmonic oscillations at half the switching frequency $f_{osc} = f_s/2$. This may also cause a saturation of the current loop controller.

Figure 13.7 shows the steady-state and perturbed (transient) inductor current waveforms for a stable inner current loop ($D < 0.5$), a marginally stable current loop ($D = 0.5$), and an unstable current loop ($D > 0.5$). For $D < 0.5$, the perturbed inductor current waveform is convergent to the steady-state waveform. Conversely, for $D > 0.5$, the perturbed inductor current waveform is divergent and does not return to the steady-state waveform. To achieve a sufficient margin of stability, D_{max} should be lower than 0.5, e.g., $D_{max} = 0.2$.

13.5 Slope Compensation

The instability of the current loop can be eliminated by subtracting an artificial periodic ramp waveform from the control signal waveform, or by adding an artificial ramp waveform to the inductor or switch current waveform. We will consider a fixed-slope compensation ramp case. Figure 13.8 shows an implementation of slope compensation using a differential amplifier. Figure 13.9 shows the waveforms illustrating the slope compensation, where an artificial periodic ramp current waveform i_A is subtracted from the control current i_C; consequently, the slope M_2 is reduced, and the switch turns off when

$$i_L(DT_s) = i_C(DT_s) - i_A(DT_s) = i_C(DT_s) - M_3 DT_s. \tag{13.27}$$

Consider the steady-state and perturbed waveforms of the inductor current, depicted in Figure 13.10. The slope of the inductor current waveform i_L during the switch on-time interval $0 < t \leq DT_s$ is

$$M_1 = \tan\alpha = \frac{BC}{dT_s}, \tag{13.28}$$

and the slope of the ramp current $i_C - i_A$ is

$$M_3 = \tan\gamma = \frac{AB}{dT_s}, \tag{13.29}$$

giving the magnitude of the inductor current perturbation at $t = 0$,

$$\Delta i_{L0} = AC = AB + BC = (M_1 + M_3)\, dT_s. \tag{13.30}$$

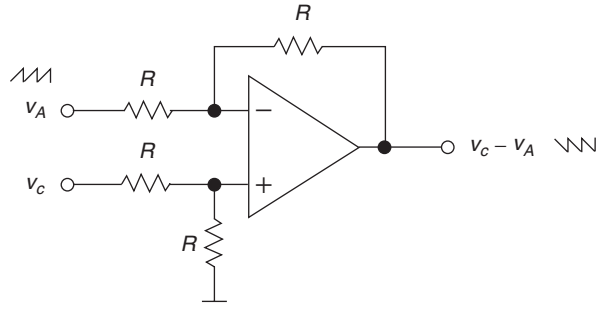


Figure 13.8 Implementation of slope compensation using a differential amplifier.

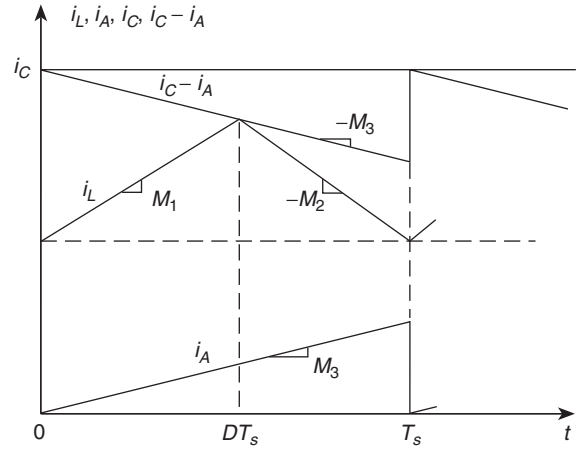


Figure 13.9 Steady-state waveforms of the inductor current i_L, the control current i_C, an artificial ramp current i_A, and $i_C - i_A$ illustrating slope compensation by subtracting a ramp current i_A from the control current i_C in PWM converters with current-mode control for CCM.

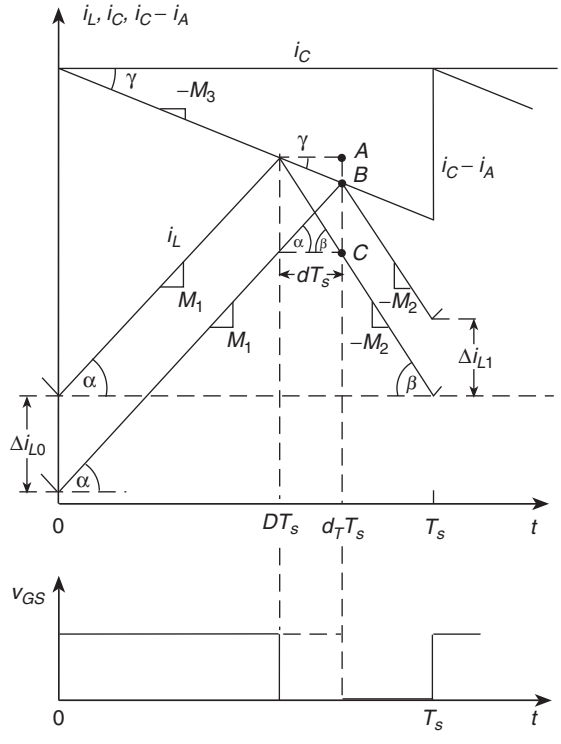


Figure 13.10 Waveforms of the inductor current i_L, the control current i_C, and $i_C - i_A$ used to derive the stability condition for the current loop with slope compensation.

The slope of the inductor current waveform i_L during the switch off-time interval $DT_s < t \le T_s$ is

$$M_2 = \tan\beta = \frac{AC}{dT_s} = \frac{\Delta i_{L0}}{dT_s} = M_1 + M_3, \tag{13.31}$$

resulting in the magnitude of the inductor current perturbation at $t = T_s$,

$$\Delta i_{L1} = BC = AC - AB = (M_2 - M_3)\, dT_s. \tag{13.32}$$

From (13.30) and (13.32), one obtains the ratio of the absolute values of the inductor current changes at $t = T_s$ and $t = 0$,

$$a = \frac{\Delta i_{L1}}{\Delta i_{L0}} = \frac{M_2 - M_3}{M_1 + M_3}. \tag{13.33}$$

The current loop with slope compensation is stable if

$$a < 1, \tag{13.34}$$

which happens when

$$M_3 > \frac{M_2 - M_1}{2}. \tag{13.35}$$

Substitution of (13.4) into (13.33) gives a in terms of M_1, M_3, and D,

$$a = \frac{\dfrac{M_2}{M_1} - \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}} = \frac{\dfrac{D}{1-D} - \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}} < 1. \tag{13.36}$$

The maximum value of the duty cycle below which the current loop is stable for a given slope ratio M_3/M_1 is given by

$$D_{lim} = 1 - \frac{0.5}{1 + \dfrac{M_3}{M_1}} = \frac{0.5 + \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}}, \quad \text{for } D > 0.5. \tag{13.37}$$

As the normalized compensating ramp slope M_3/M_1 increases, the range of the duty cycle, in which the inner current loop is stable, increases above 0.5. For example, for $M_3/M_1 = 0.5$, the inner loop is stable for $0 < D < 2/3$. From (13.37),

$$D'_{lim} = 1 - D_{lim} = \frac{0.5}{1 + \dfrac{M_3}{M_1}}. \tag{13.38}$$

The condition of stability can be also expressed [36] by

$$\frac{M_3}{M_1} > \frac{D - 0.5}{1 - D}, \quad \text{for } D > 0.5. \tag{13.39}$$

At the boundary between unstable and stable operation of the inner loop,

$$\frac{M_3}{M_1} = \frac{D - 0.5}{1 - D}. \tag{13.40}$$

Figure 13.11 shows the plot of M_3/M_1 as a function of D. As D is increased from 0.5 to 1, M_3/M_1 increases from 0 to ∞. The minimum value of the compensating slope is

$$M_{3min} = \frac{M_{1min}(D_{lim} - 0.5)}{1 - D_{lim}}. \tag{13.41}$$

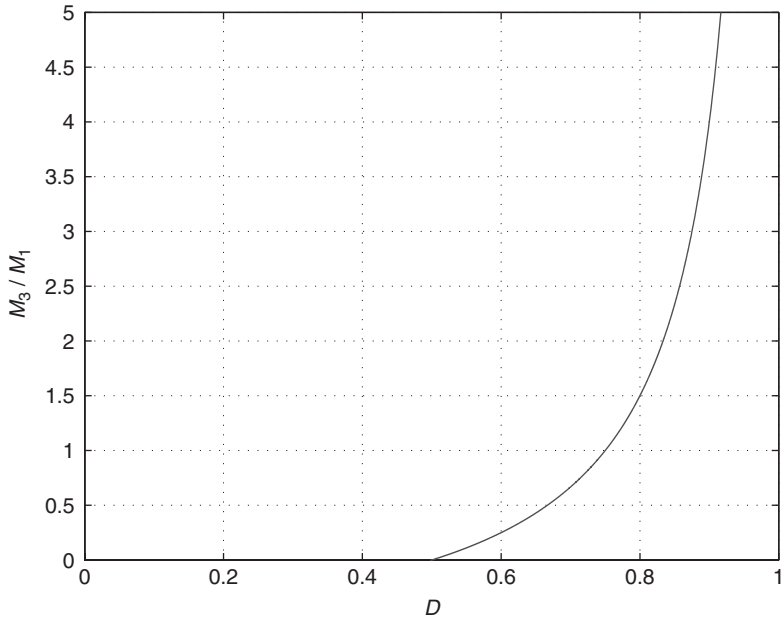


Figure 13.11 Plot of M_3/M_1 as a function of D.

At $D_{lim} = 0.5$, $M_{3min} = 0$ as expected. As the maximum duty cycle D_{lim} is increased from 0.5 to 1, M_{3min} increases from zero to ∞. To achieve relative stability, one should select M_3 sufficiently higher than M_{3min}.

Using (13.4), (13.33) can be expressed in terms of the slopes M_2 and M_3 and the duty cycle D as

$$a = \frac{M_2 - M_3}{M_1 + M_3} = \frac{1 - \dfrac{M_3}{M_2}}{\dfrac{M_1}{M_2} + \dfrac{M_3}{M_2}} = \frac{1 - \dfrac{M_3}{M_2}}{\dfrac{1-D}{D} + \dfrac{M_3}{M_2}} < 1, \tag{13.42}$$

yielding the condition of stability [36]

$$\frac{M_3}{M_2} > 1 - \frac{1}{2D}, \quad \text{for } D > 0.5. \tag{13.43}$$

At the boundary between stable and unstable operation of the inner loop,

$$\frac{M_3}{M_2} = 1 - \frac{1}{2D}. \tag{13.44}$$

Figure 13.12 shows M_3/M_2 as a function of D. As D is increased from 0.5 to 1, the ratio M_3/M_2 increases from 0 to 0.5. The minimum compensating slope at a maximum duty cycle D_{max} is given by

$$M_{3min} = M_{2max}\left(1 - \frac{1}{2D_{lim}}\right). \tag{13.45}$$

For the worst case, which occurs at $D = 1$, (13.42) becomes

$$A_{ic} = \frac{M_2}{M_3} - 1 < 1, \tag{13.46}$$

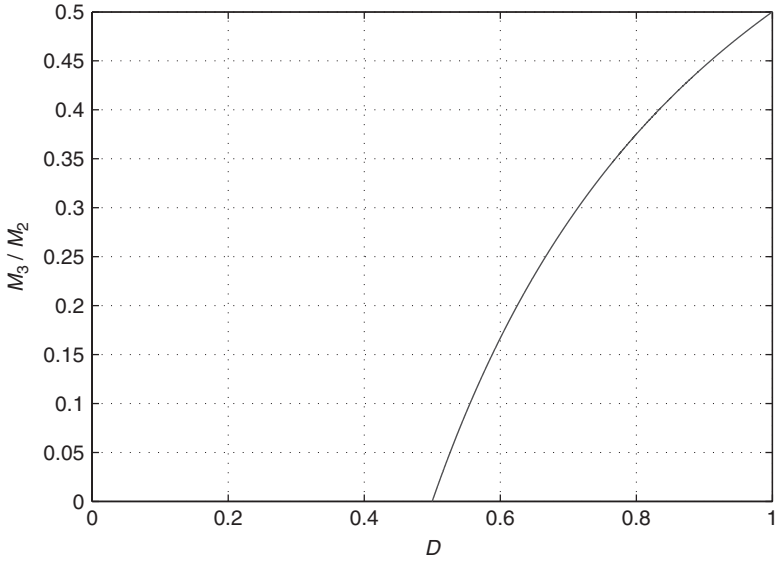


Figure 13.12 Plot of M_3/M_2 as a function of D.

and the condition of stability at any duty cycle D is given by

$$M_3 > \frac{M_2}{2}. \tag{13.47}$$

Note that the falling slope M_2 approaches infinity as the duty cycle D approaches 1.

From (13.42), $a = 0$, when the compensating slope M_3 is equal to the inductor current falling slope M_2, resulting in the optimum slope compensation

$$M_{3opt} = M_2, \tag{13.48}$$

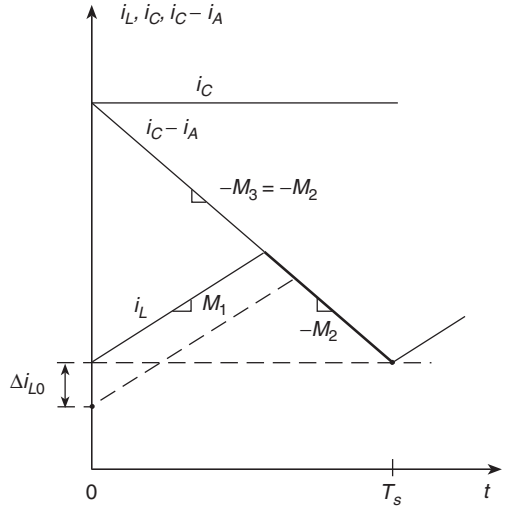


Figure 13.13 Elimination of perturbation in the inductor current waveform in closed-inner loop during one cycle at $M_3 = M_2$ (dead-beat control).

as illustrated in Figure 13.13. In this case, the inductor current waveform reaches steady state in exactly one cycle, yielding the fastest possible response of the inner loop. A perturbation ends within the same cycle in which it starts. Operation at $M_3 = M_2$ is called *dead-beat control*. Note that if $M_3 = 0$, then (13.42) reduces to $M_2/M_1 < 1$. From (13.42),

$$M_3 = \frac{M_2 - aM_1}{a+1} = \frac{\left(\dfrac{D}{1-D} - a\right) M_1}{a+1}. \tag{13.49}$$

13.6 Sample-and-hold Effect on Current Loop

Modeling current-mode-controlled converters involves discrete-time signals and nonlinear, time-varying circuits. Operation of the closed-current loop is similar to that of sample-and-hold circuits. 'Sampling' the analog, continuous-time control current i_C (or control voltage v_C) occurs once in a switching cycle T_s at the instant when the inductor current i_L reaches the control current i_C, turning the switch on and setting the duty cycle for that switching cycle. Only the control current values at the sampling instants (i.e., sampled-data information) are used to control the inner loop. The changes in the inductor current waveform and the changes in the average values of the inductor current in successive cycles can be described by the zero-order-hold function. The waveforms of the duty cycle and changes in the duty cycle in successive cycles are 'staircase' functions (discrete in magnitude) by nature and are similar to the waveforms in the zero-order-hold circuit. Therefore, some waveforms in current loop are discrete-time signals and can be described in the z-domain.

A review of sample-and-hold medeling in given in the Appendix to this chapter.

13.6.1 Natural Response of Inductor Current to Small Perturbation in Closed-current Loop

Figure 13.14(a) shows a *natural response* of the inductor current in the closed-current loop [25]. At $t = kT_s$, a small perturbation in the inductor current i_L is introduced when the control voltage with slope compensation remains unchanged and other perturbations are zero, that is, $v_i = 0$ and $i_o = 0$. This perturbation causes propagation of inductor current changes over subsequent cycles. The sampling occurs at the intersections of waveforms $R_s i_L$ and $v_C - v_A$. The difference between the steady-state inductor current waveform and the perturbed (transient) inductor current waveform is equal to the exact waveform of the small-signal inductor current i_l, shown in Figure 13.14(b). The exact waveform of the small-signal inductor current i_l can be approximated by the waveform depicted in Figure 13.14(c), where the finite slope after the sampling instant $t = kT_s$ is replaced by an infinite slope. The difference between the exact and approximate waveforms is very small and can be neglected. The instantaneous inductor current changes can be seen as the average inductor current changes. The approximate waveform of the small-signal inductor current i_l is the same as the zero-order-hold waveform. The time intervals between the sampling instants are not constant, but the differences between them are small enough to be neglected. Figure 13.15 shows an enlarged part of the natural response depicted in Figure 13.14(a). From geometry,

$$M_1 = \tan\alpha = \frac{BC}{\Delta t_k} \tag{13.50}$$

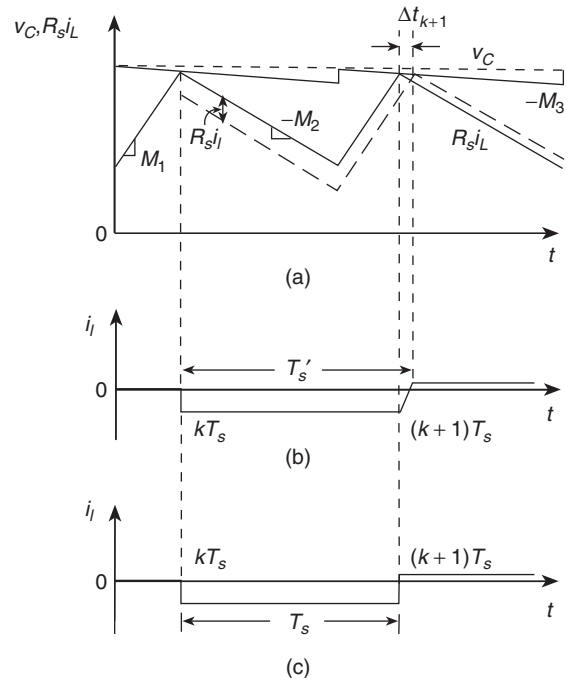


Figure 13.14 Natural response of the inductor current in the closed-current loop. Waveforms of the inductor current in the inner current loop after a small perturbation in the inductor current i_L introduced at time $t = kT_s$. (a) Waveforms of steady-state control voltage v_C, steady-state normalized inductor current $R_s i_L$ (solid line), and perturbed (transient) normalized inductor current $R_s(i_L + i_l)$ (dashed line). (b) Exact waveform of the difference between the steady-state and perturbed waveforms, resulting in a small-signal inductor current i_l. (c) Approximate waveform of the small-signal inductor current i_l.

and

$$M_3 = \tan\gamma = \frac{AB}{\Delta t_k}, \tag{13.51}$$

resulting in the small-signal component of the inductor current at the time of the perturbation $t = kT_s$,

$$R_s i_{ln}(k) = -(AB + BC) = -(M_1 + M_3)\Delta t_k. \tag{13.52}$$

Similarly,

$$M_2 = \tan\beta = \frac{AC}{\Delta t_k}, \tag{13.53}$$

yielding the small-signal component of the inductor current after one cycle from the beginning of the perturbation $t = (k + 1)T_s$,

$$R_s i_{ln}(k + 1) = AC - AB = (M_2 - M_3)\Delta t_k. \tag{13.54}$$

Thus,

$$\frac{R_s i_{ln}(k + 1)}{R_s i_{ln}(k)} = -\frac{(M_2 - M_3)\Delta t_k}{(M_1 + M_3)\Delta t_k} = -\frac{M_2 - M_3}{M_1 + M_3} = -a, \tag{13.55}$$

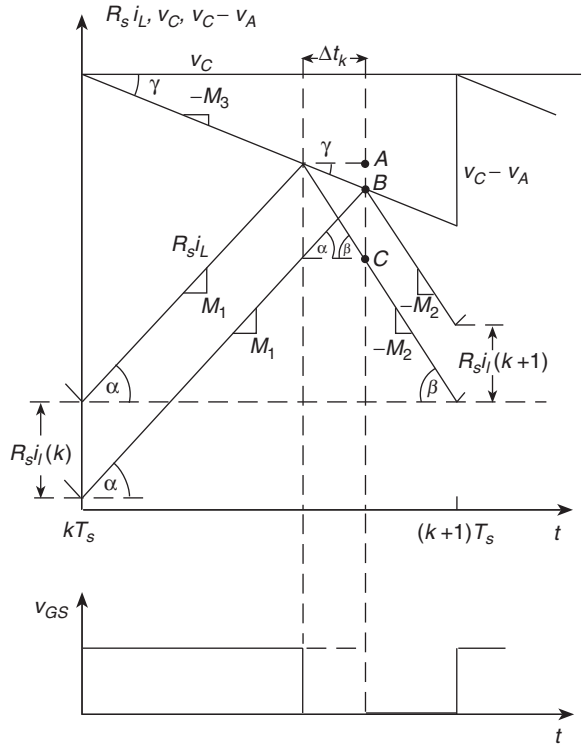


Figure 13.15 Enlarged waveforms of natural response depicted in Figure 13.14(a).

where

$$a = \frac{M_2 - M_3}{M_1 + M_3} = \frac{\dfrac{M_2}{M_1} - \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}} = \frac{\dfrac{D}{1-D} - \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}}. \tag{13.56}$$

Hence, the discrete-time natural response of the approximate small-signal inductor current from one sampling instant to the next is given by

$$i_{ln}(k+1) = -ai_{ln}(k). \tag{13.57}$$

13.6.2 Forced Response of Inductor Current to Step Change in Control Voltage in Closed-current Loop

Figure 13.16(a) illustrates a *forced response* of the inductor current to a step change in the control voltage in the closed-current loop [25]. At time $t = kT_s$, there is a step change in the control voltage v_C from V_C to $V_C + v_c$, causing a perturbation in the inductor current waveform i_L. It is assumed that the converter input voltage V_I and the output voltage V_O remain constant, which implies that the inductor rising slope M_1 and the inductor falling slope M_2 also remain constant. The sampling occurs at the intersection of the compensated control voltage waveform $v_C - v_A$ and the voltage waveform $R_s i_L$, proportional to the

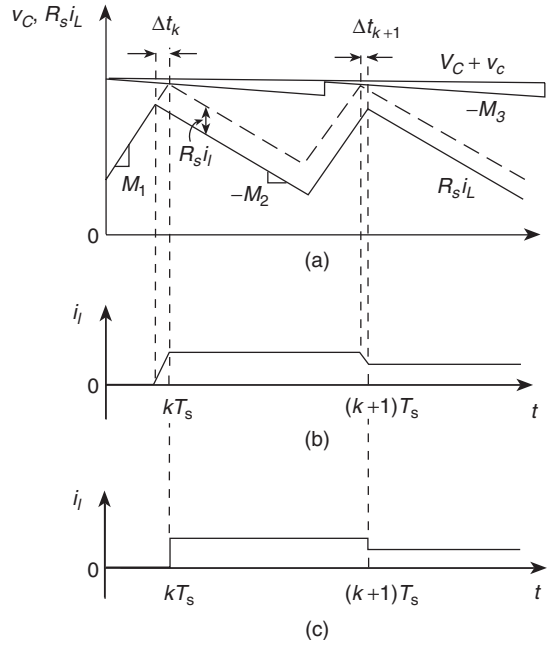


Figure 13.16 Forced response of the inductor current in the closed-current loop. Waveforms of the control voltage and inductor current in the inner current loop after a step change in the control voltage v_C from V_C to $V_C + v_c$ at time $t = kT_s$, causing a perturbation of the inductor current i_L. (a) Waveforms of control voltage $v_C = V_C + v_c$, steady-state inductor current $R_s i_L$ (solid line), and perturbed normalized inductor current $R_s(i_L + i_l)$ (dashed line). (b) Exact waveform of the difference between the steady-state and perturbed waveforms, resulting in a small-signal inductor current i_l. (c) Approximate waveform of the small-signal inductor current i_l.

inductor current i_L. Figure 13.17 shows an enlargement of the forced response shown in Figure 13.16(a). From geometry,

$$M_1 = \tan\alpha = \frac{AB}{\Delta t_k} \tag{13.58}$$

and

$$M_3 = \tan\gamma = \frac{BC}{\Delta t_k}, \tag{13.59}$$

yielding the step change in the control voltage,

$$v_c(k+1) = AB + BC = (M_1 + M_3)\Delta t_k. \tag{13.60}$$

Likewise,

$$M_2 = \tan\beta = \frac{BD}{\Delta t_k}, \tag{13.61}$$

giving the small-signal component of the inductor current after one cycle at $t = (k+1)T_s$,

$$R_s i_{lf}\,(k+1) = AB + BD = (M_1 + M_2)\Delta t_k. \tag{13.62}$$

Hence,

$$\frac{R_s i_{lf}(k+1)}{v_c(k+1)} = \frac{(M_1 + M_2)\Delta t_{k+1}}{(M_1 + M_3)\Delta t_{k+1}} = \frac{M_1 + M_2}{M_1 + M_3} = 1 + \frac{M_2 - M_3}{M_1 + M_3} = 1 + a. \tag{13.63}$$

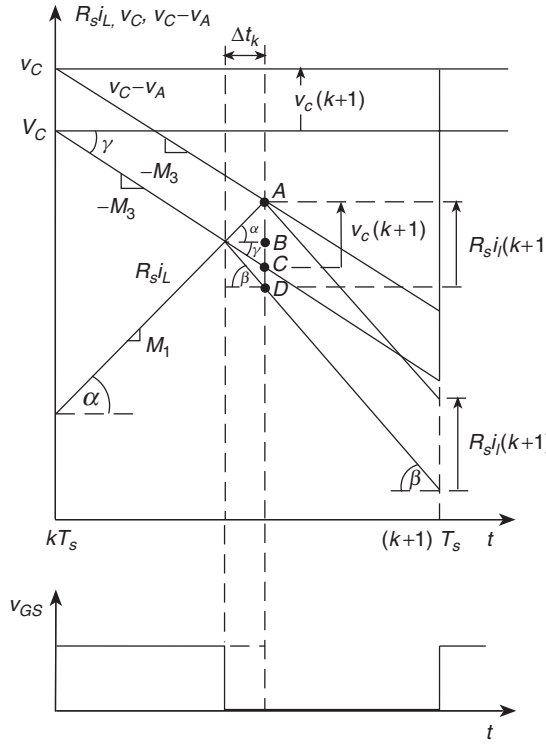


Figure 13.17 Enlargement of waveforms of forced response shown in Figure 13.16(a).

The discrete-time forced response is given by

$$i_{lf}\ (k+1) = \frac{1+a}{R_s} v_c(k+1). \tag{13.64}$$

The total response is the sum of the natural response and the forced response. The discrete-time relationship between the control voltage and the inductor current [25] is

$$i_l(k+1) = i_{ln}\ (k+1) + i_{lf}(k+1) = -a i_l(k) + \frac{1+a}{R_s} v_c(k+1). \tag{13.65}$$

13.6.3 Transfer Function of Closed-current Loop in z-Domain

From the definition of the z-transform, the sampled inductor current in the z-domain is

$$\begin{aligned} \mathcal{Z}\{i_l(k)\} = i_l(z) &= \sum_{k=0}^{\infty} i_l(k) z^{-k} \\ &= i_l(0) + i_l(1) z^{-1} + i_l(2) z^{-2} + \cdots + i_l(k) z^{-k} + \cdots, \end{aligned} \tag{13.66}$$

and, from the shifting theorem,

$$\mathcal{Z}\{i_l(k+1)\} = z i_l(z) \tag{13.67}$$

and

$$\mathcal{Z}\{v_c(k+1)\} = z v_c(z). \tag{13.68}$$

Hence, the z-transform of (13.65) is

$$zi_l(z) = -ai_l(z) + \frac{1+a}{R_s} zv_c(z), \tag{13.69}$$

which gives

$$(z+a)i_l(z) = \frac{(1+a)z}{R_s} v_c(z). \tag{13.70}$$

Thus, the *discrete closed-current-loop control voltage-to-inductor current transfer function* is given by

$$H_{icl}(z) = \frac{i_l(z)}{v_c(z)} = \frac{1+a}{R_s} \frac{z}{z+a} = \frac{1+a}{R_s} \frac{z}{z-p}. \tag{13.71}$$

This transfer function contains a pole $p = -a$. For $a > 1$, the discrete transfer function $H_{icl}(z)$ has a pole outside the unit circle, and therefore the closed-current loop is unstable, causing growing oscillations of the inductor current at $f_s/2$, called subharmonic oscillation. This situation takes place, for example, for $M_1 < M_2$ at $M_3 = 0$, that is, for $D > 0.5$ and no ramp compensation. For $a = 1$, the pole is located on the unit circle, resulting in the current loop instability and steady-state oscillations.

13.7 Current Loop in s-Domain

13.7.1 Control Voltage-to-inductor Current Transfer Function

The closed-loop discrete control voltage-to-inductor current transfer function $H_{icl}(z)$ in the z-domain can be transformed into a continuous closed-loop control voltage-to-inductor current transfer function $H_{icl}(s)$ in the s-domain. Using the definition of the z-transform $z = e^{sT_s}$ and multiplying the result by the zero-order hold transfer function

$$H_{ZOH}(s) = \frac{v_c^0(s)}{v_c^*(s)} = \frac{1 - e^{-sT_s}}{s}, \tag{13.72}$$

we obtain the inductor current in the s-domain,

$$i_l(s) = \frac{1+a}{R_s} \frac{e^{sT_s}}{e^{sT_s}+a} \frac{1-e^{-sT_s}}{s} v_c^*(s) = \frac{1+a}{R_s s} \frac{e^{sT_s}-1}{e^{sT_s}+a} v_c^*(s), \tag{13.73}$$

where the asterisk represents a sampled variable. The Laplace transform of the output voltage $v_c(s)$ of a sampler is related to the sampled-data transform $v_c^*(s)$ by the expression

$$v_c^*(s) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} v_c\,(s + jn\omega_s) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} v_c \left(s + \frac{j2\pi n}{T_s}\right), \tag{13.74}$$

which is a form of Shannon's sampling theorem showing the frequency aliasing and folding effects. This approximation assumes that the control voltage v_c does not contain significant components above $f_s/2$ (i.e., $|v_c(f)| \approx 0$), and therefore there is no aliasing. The approximation is based on sinusoidal control voltage testing and a narrow-band network analyzer measurement. If a sinusoidal control voltage with a frequency f is used, the spectrum of the sampled-control voltage occurs at $kf_s \pm f$, where $k = 0, 1, 2, \ldots$. If f is lower than the Nyquist frequency $f_s/2$, the sidebands are located above $f_s/2$. Hence, the transfer function of an ideal sampler can be approximated for $0 < f < f_s/2$ by

$$H_s(s) = \frac{v_c^*(s)}{v_c(s)} \approx \frac{1}{T_s}. \tag{13.75}$$

The control voltage-to-inductor current transfer function can be approximated in the s-domain by

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{i_l(s)}{i_1^*(s)} \times \frac{i_l^*(s)}{v_c^*(s)} \times \frac{v_c^*(s)}{v_c(s)} \approx \frac{1+a}{R_s} \frac{e^{sT_s}}{e^{sT_s}+a} \frac{1-e^{-sT_s}}{sT_s} = \frac{1+a}{R_s sT_s} \frac{e^{sT_s}-1}{e^{sT_s}+a}. \tag{13.76}$$

This is not a rational function, that is to say, it is not a ratio of two polynomials. Using the second-order Padé approximation,

$$e^{-sT_s} \approx \frac{1-\frac{sT_s}{2}+\frac{(sT_s)^2}{12}}{1+\frac{sT_s}{2}+\frac{(sT_s)^2}{12}} = \frac{1-\frac{s}{2f_s}+\frac{s^2}{12f_s^2}}{1+\frac{s}{2f_s}+\frac{s^2}{12f_s^2}} = \frac{1-\frac{s}{\omega_s/\pi}+\left(\frac{s}{\sqrt{3}\omega_s/\pi}\right)^2}{1+\frac{s}{\omega_s/\pi}+\left(\frac{s}{\sqrt{3}\omega_s/\pi}\right)^2} \tag{13.77}$$

gives the control voltage-to-inductor current transfer function of the closed-current loop approximated by a rational function [47]

$$\begin{aligned} H_{icl}(s) = \frac{i_l(s)}{v_c(s)} &\approx \frac{1}{R_s} \frac{1}{1+\frac{1-a}{1+a}\frac{sT_s}{2}+\frac{(sT_s)^2}{12}} = \frac{1}{R_s} \frac{1}{1+\frac{1-a}{1+a}\frac{s}{2f_s}+\frac{s^2}{12f_s^2}} \\ &= \frac{1}{R_s} \frac{12f_s^2}{s^2+\frac{1-a}{1+a}6f_s s+12f_s^2} = \frac{1}{R_s} \frac{\omega_i^2}{s^2+2\xi_i\omega_i s+\omega_i^2} \\ &= \frac{1}{R_s} \frac{1}{1+\frac{2\xi_i}{\omega_i}s+\left(\frac{s}{\omega_i}\right)^2}, \end{aligned} \tag{13.78}$$

where

$$\omega_i = \sqrt{12} f_s = \frac{\sqrt{3}\omega_s}{\pi} \approx 0.5513\omega_s, \tag{13.79}$$

$$\xi_i = \frac{\sqrt{3}}{2}\left(\frac{1-a}{1+a}\right), \tag{13.80}$$

$$Q_i = \frac{1}{2\xi_i} = \frac{1}{\sqrt{3}}\left(\frac{1+a}{1-a}\right), \tag{13.81}$$

and

$$p_{i1}, p_{i2} = -\xi_i\omega_i \pm j\omega_i\sqrt{1-\xi_i^2} = -\frac{1-a}{1+a}3f_s \pm j2\sqrt{3}f_s\sqrt{1-\frac{3}{4}\left(\frac{1-a}{1+a}\right)^2}. \tag{13.82}$$

At $s = 0$,

$$H_{iclo} = H_{icl}(0) = \frac{1}{R_s}. \tag{13.83}$$

Thus, $H_{icl}(s)$ represents a second-order low-pass filter transfer function and depends only on f_s, a, and R_s. It has two imaginary conjugate poles located either in the LHP or RHP. For $a < 1$, the two poles are in the LHP, and the closed-current loop is stable. For $a = 1$, $\xi_i = 0$ and $Q_i = \infty$, and the closed-current loop is unstable, causing steady-state oscillations. For $a > 1$, $\xi_i < 0$ and $Q_i < 0$, and the current loop is unstable, causing growing oscillations. Note that a is different for different converters.

Figures 13.18 and 13.19 show Bode plots of $H_{icl}(s)$ for selected values of a at $R_s = 1\,\Omega$. The maximally flat magnitude response of $|H_{icl}|$ occurs for

$$\xi_i = \frac{\sqrt{3}}{2}\left(\frac{1-a}{1+a}\right) = \frac{1}{\sqrt{2}}, \tag{13.84}$$

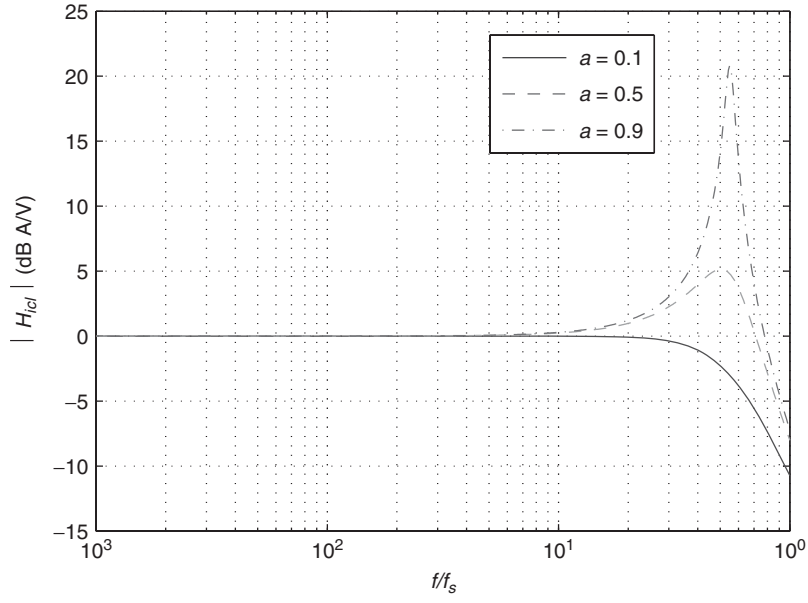


Figure 13.18 Bode plot of the magnitude of H_{icl} for selected values of a.

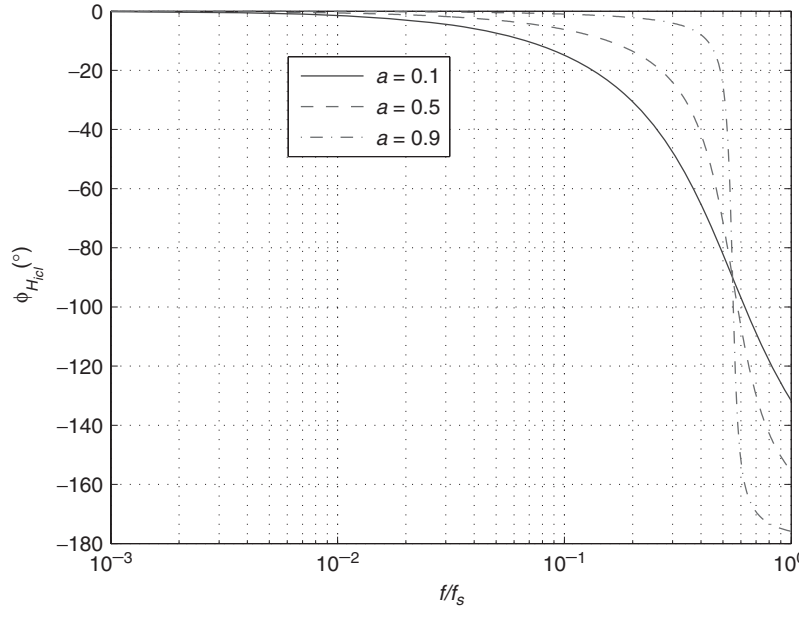


Figure 13.19 Bode plot of the phase of H_{icl} for selected values of a.

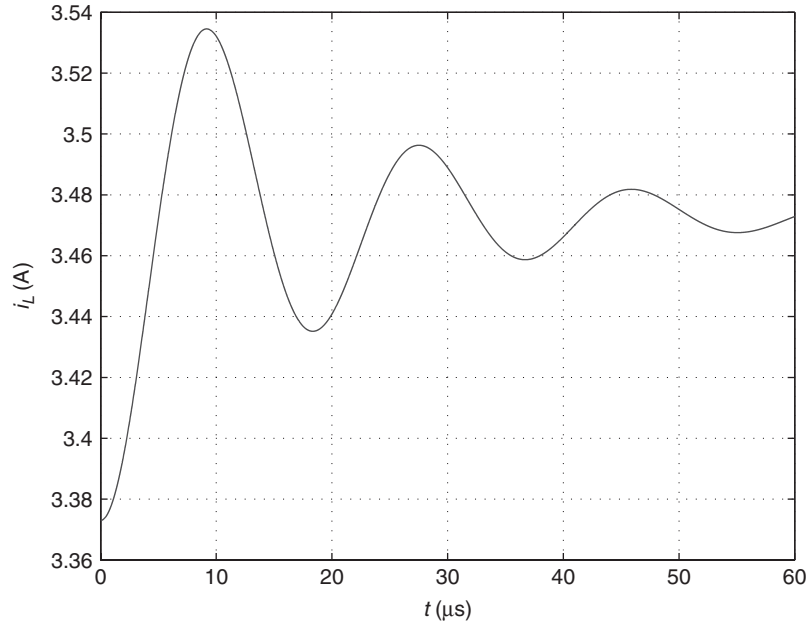


Figure 13.20 Step response of the inductor current i_L to a step change in $\Delta V_c = 0.01\,\text{V}$ at $a = 0.7$.

resulting in

$$a_{cr} = \frac{\sqrt{3} - \sqrt{2}}{\sqrt{3} + \sqrt{2}} \approx 0.1. \tag{13.85}$$

For $a > 0.1$, $\xi < 1/\sqrt{2}$ and $|H_{icl}|$ exhibits peaking. For $a = 1$, $|H_{icl}|$ approaches ∞ at $f \approx f_s/2$.

Figures 13.20–13.22 show the responses of the inductor current to $\Delta V_c = 0.01\,\text{V}$ at $a = 0.7$, 1, and 1.2, respectively. As expected, the magnitude of the inductor current waveform decays at $a = 0.7$, has a constant amplitude at $a = 1$, and increases at $a = 1.2$. The current loop is stable for $a = 0.7$, is marginally stable for $a = 1$, and is unstable for $a = 1.2$.

13.7.2 Error Voltage-to-duty Cycle Transfer Function

Figure 13.23 shows a block diagram of the closed-current loop with the inductor current i_l as an output. This loop will be used to find the sample-and-hold error voltage-to-duty cycle transfer function T_{ms}. The control voltage-to-inductor current transfer function of the closed-current loop can be expressed by [47]

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{T_{ms}T_{pi}}{1 + T_{ms}T_{pi}R_s}. \tag{13.86}$$

Equating the right-hand sides of (13.76) and (13.86),

$$H_{icl}(s) = \frac{T_{ms}T_{pi}}{1 + T_{ms}T_{pi}R_s} = \frac{1 + a}{R_s s T_s} \frac{e^{sT_s} - 1}{e^{sT_s} + a}, \tag{13.87}$$

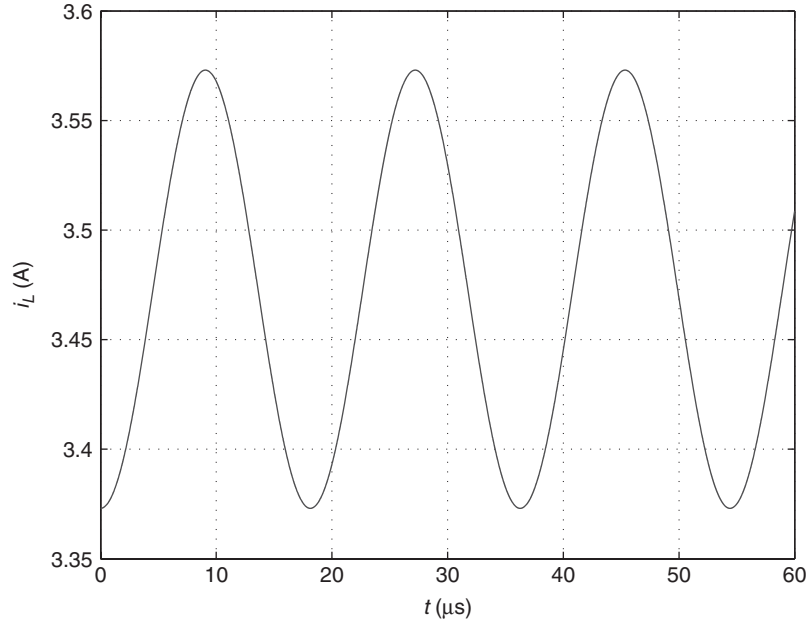


Figure 13.21 Step response of the inductor current i_L to a step change in $\Delta V_c = 0.01\,\text{V}$ at $a = 1$.

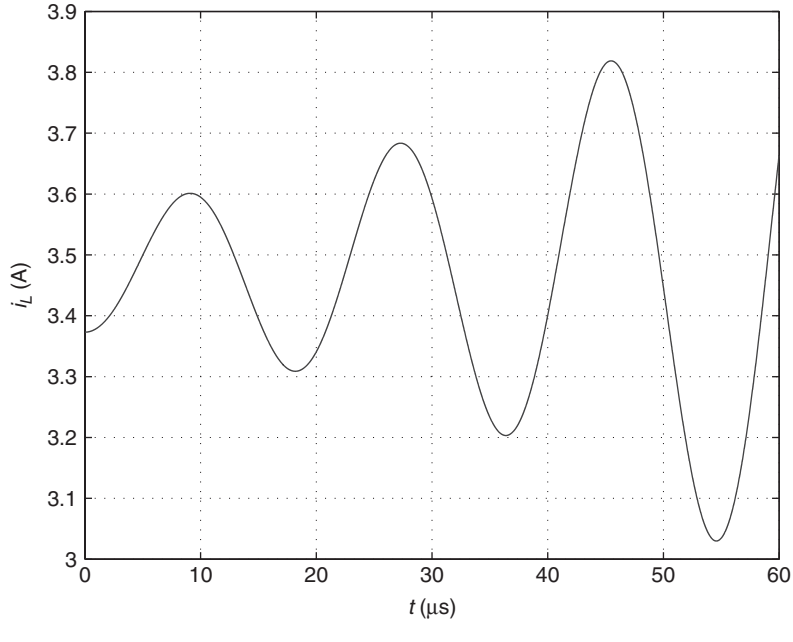


Figure 13.22 Step response of the inductor current i_L to a step change in $\Delta V_c = 0.01\,\text{V}$ at $a = 1.2$.

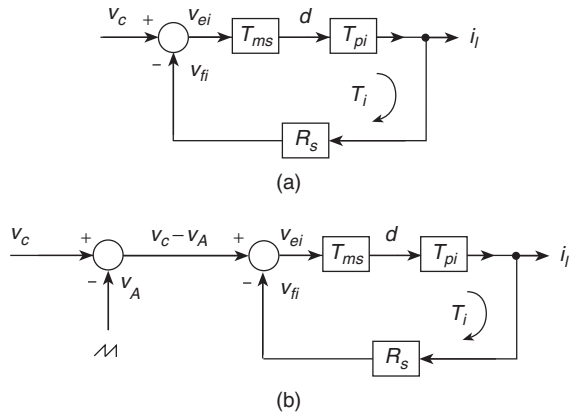


Figure 13.23 Block diagram of the closed-current loop showing the transfer function from the control voltage to the inductor current i_l, used for determining $T_{ms} = d/v_{ei}$. No disturbances are present, that is, $v_i = 0$ and $i_o = 0$. (a) Without slope compensation. (b) With slope compensation.

yields the sample-and-hold error voltage-to-duty cycle transfer function [47]

$$T_{ms}(s) = \frac{d(s)}{v_{ei}(s)} = \frac{1}{R_s T_{pi}\left(\dfrac{1}{R_s H_{icl}(s)} - 1\right)} = \frac{1}{R_s T_{pi}\left[\dfrac{sT_s(e^{sT_s} + a)}{(1+a)(e^{sT_s} - 1)} - 1\right]}. \tag{13.88}$$

Using the second-order Padé approximation given by (13.77), one obtains [47]

$$T_{ms}(s) \approx \frac{12\, f_s^2}{R_s T_{pi} s\left(s + \dfrac{1-a}{1+a} 6\, f_s\right)} = \frac{12\, f_s^2}{R_s T_{pi} s\,(s + \omega_{sh})}, \tag{13.89}$$

where

$$\omega_{sh} = \frac{1-a}{1+a} 6\, f_s = \frac{1-a}{1+a}\left(\frac{3}{\pi}\right)\omega_s = \frac{1-a}{1+a}\sqrt{3}\omega_i \tag{13.90}$$

and

$$p_{sh} = -\omega_{sh} = -\frac{1-a}{1+a} 6\, f_s. \tag{13.91}$$

Thus, the transfer function T_{ms} is converter-dependent because it depends on T_{pi}. As a increases from 0 to 1, f_{sh} decreases from $3\, f_s/\pi$ to 0.

It will be shown in subsequent chapters that the duty cycle-to-inductor current transfer function T_{pi} for simple transformerless PWM converters, such as buck, boost, and buck-boost converters, is expressed by an equation of the same form,

$$T_{pi}(s) = \frac{i_l(s)}{d(s)} = T_{pix}\frac{s + \omega_{zi1}}{s^2 + 2\xi\omega_0 s + \omega_0^2}. \tag{13.92}$$

For different converters, parameters T_{pix}, ω_{zi1}, ξ, and ω_0 are described by different equations.

The error voltage-to-duty cycle transfer function, which is equal to the forward gain of the current loop, is given by [47]

$$T_{ms}(s) = \frac{d(s)}{v_{ei}(s)} \approx \frac{12\, f_s^2}{R_s T_{pi} s\left(s + \dfrac{1-a}{1+a} 6\, f_s\right)} = \frac{12\, f_s^2}{R_s T_{pi} s\,(s + \omega_{sh})}$$

$$= \frac{12\, f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix} s(s + \omega_{sh})(s + \omega_{zi1})} = T_{msx}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{s^3 + (\omega_{sh} + \omega_{zi1})s^2 + \omega_{sh}\omega_{zi1} s}, \tag{13.93}$$

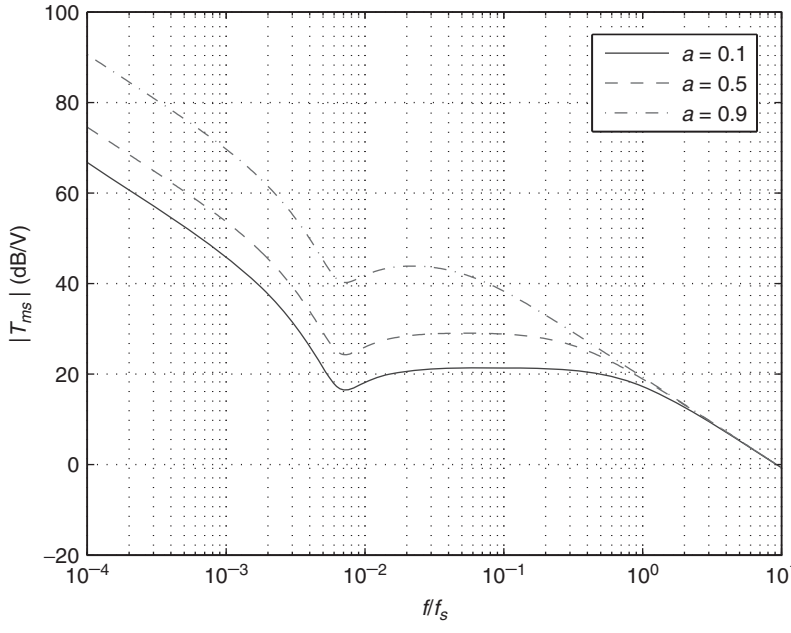


Figure 13.24 Bode plot of the magnitude of the error voltage-to-duty cycle transfer function T_{ms} for selected values of a.

where

$$T_{msx} = \frac{12\, f_s^2}{R_s T_{pix}}. \tag{13.94}$$

Figures 13.24 and 13.25 show Bode plots of T_{ms} at various values of a.

Substitution of (13.92) into (13.89) yields the normalized sample-and-hold transfer function for any basic converter,

$$H_{sh}(s) = \frac{T_{ms}(s)}{T_m} \approx \frac{12\, f_s^2 (s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_m T_{pix} s (s + \omega_{sh})(s + \omega_{zi1})}, \tag{13.95}$$

where $T_m = f_s/(M_1 + M_3)$.

13.7.3 Loop Gain of Current Loop

The loop gain of the current loop is

$$T_i(s) = \frac{v_{fi}(s)}{v_{ei}(s)} = T_{ms} T_{pi} R_s \approx \frac{12\, f_s^2}{s\left(s + \dfrac{1-a}{1+a} 6\, f_s\right)} = \frac{12\, f_s^2}{s\,(s + \omega_{sh})} = \frac{12\, f_s^2}{\omega_{sh} s \left(1 + \dfrac{s}{\omega_{sh}}\right)}$$

$$= 2\, f_s \frac{1+a}{1-a} \frac{1}{s\left(1 + \dfrac{s}{\omega_{sh}}\right)} = \frac{\omega_1}{s} \frac{1}{1 + \dfrac{s}{\omega_{sh}}}, \tag{13.96}$$

where the infinity-gain frequency of the integral part of the transfer function is

$$f_1 = \frac{\omega_1}{2\pi} = \left(\frac{f_s}{\pi}\right) \frac{1+a}{1-a}. \tag{13.97}$$

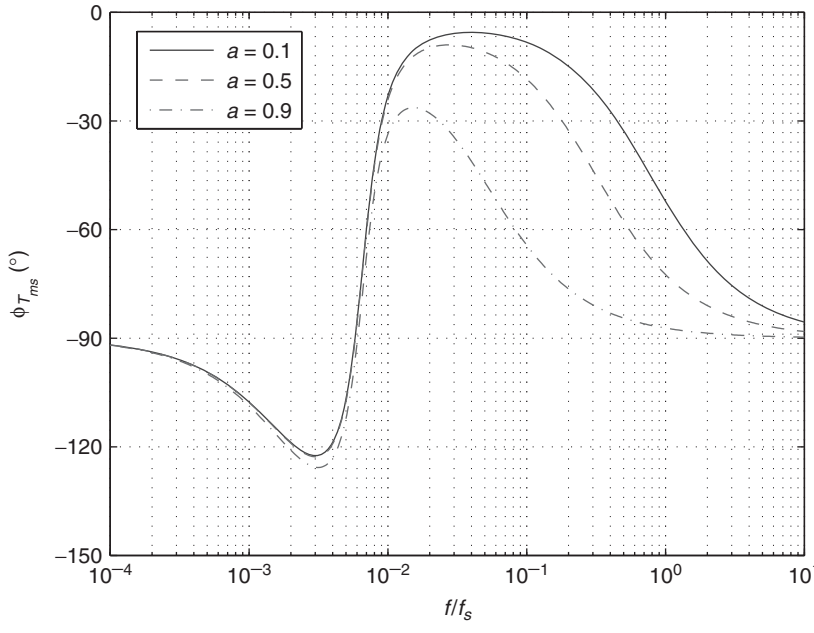


Figure 13.25 Bode plot of the phase of the error voltage-to-duty cycle transfer function T_{ms} for selected values of a.

One pole of T_i is located at the origin, and therefore the current-loop gain T_i behaves like the transfer function of an integrator. The location of the second pole $p_{sh} = -\omega_{sh}$ is dependent on a. For $a < 1$, the second pole is located in the LHP, and the current loop is stable. For $a = 1$, the second pole is located at the origin and the current loop is marginally stable. For $a > 1$, the second pole is located in the RHP, and therefore the current loop is unstable.

Figures 13.26 and 13.27 show Bode plots of the current-loop gain T_i. The crossover frequency is $f_{ci} \approx 0.4\, f_s$ for the phase margin $PM \approx 60^\circ$. Thus, the current loop is *wide-band*, yielding a fast response. The gain margin of the current loop is $GM = \infty$ because T_i is a second-order transfer function and its phase never crosses -180°.

The phase margin PM depends on a. The magnitude of the current-loop gain is

$$|T_i| = \frac{12\, f_s^2}{\omega} \frac{1}{\sqrt{\omega^2 + \omega_{sh}^2}} = \frac{3}{\pi^2} \left(\frac{f_s}{f}\right)^2 \frac{1}{\sqrt{1 + \left(\dfrac{f_{sh}}{f}\right)^2}}$$

$$= \frac{3}{\pi^2} \left(\frac{f_s}{f}\right)^2 \frac{1}{\sqrt{1 + \frac{9}{\pi^2} \left(\dfrac{1-a}{1+a}\right)^2 \left(\dfrac{f_s}{f}\right)^2}}. \tag{13.98}$$

At the crossover frequency f_{ci}, the magnitude of the current-loop gain becomes

$$|T_i(f_{ci})| = \frac{3}{\pi^2} \left(\frac{f_s}{f_{ci}}\right)^2 \frac{1}{\sqrt{1 + \left(\dfrac{f_{sh}}{f_{ci}}\right)^2}} = \frac{3}{\pi^2} \left(\frac{f_s}{f_{ci}}\right)^2 \frac{1}{\sqrt{1 + \frac{9}{\pi^2} \left(\dfrac{1-a}{1+a}\right)^2 \left(\dfrac{f_s}{f_{ci}}\right)^2}} = 1. \tag{13.99}$$

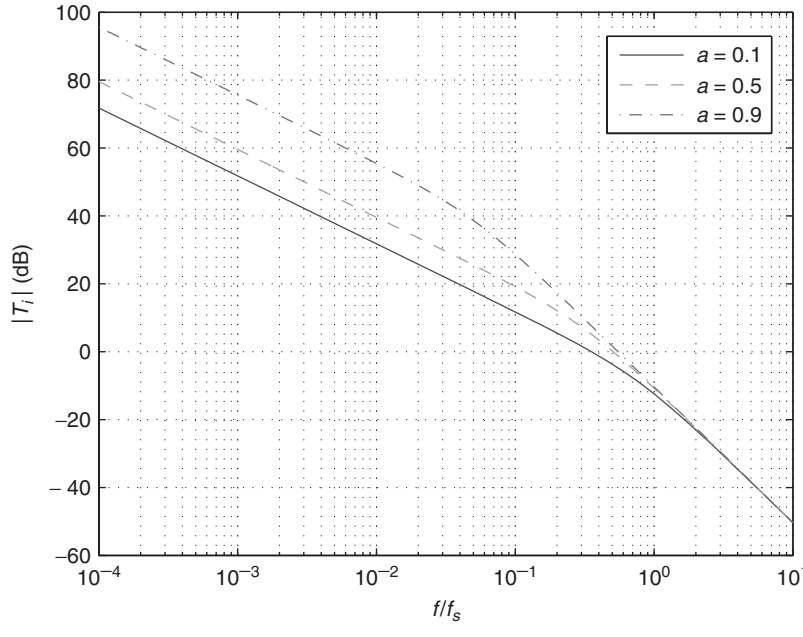


Figure 13.26 Bode plot of the magnitude of the current-loop gain T_i for selected values of a.

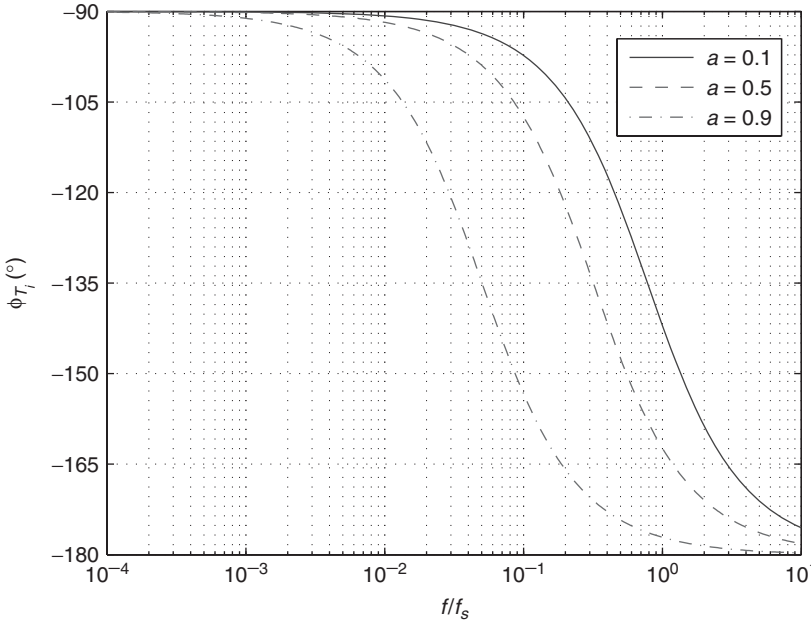


Figure 13.27 Bode plot of the phase of the current-loop gain T_i for selected values of a.

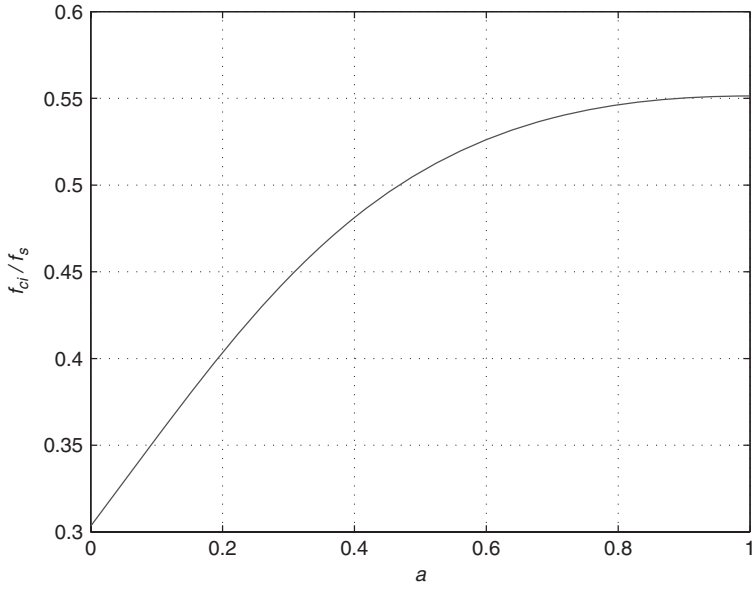


Figure 13.28 Plot of f_{ci}/f_s as a function of a.

Hence, the normalized crossover frequency of the current loop is

$$\frac{f_{ci}}{f_s} = \frac{1+a}{\pi(1-a)} \sqrt{\frac{2}{1+\sqrt{1+\frac{4}{9}\left(\frac{1+a}{1-a}\right)^4}}}. \tag{13.100}$$

Figure 13.28 shows a plot of f_{ci}/f_s as a function of a. For $a = 1$, $f_{ci}/f_s = \sqrt{3}/\pi = 0.5513$. This ratio is different from 0.5, predicted in the time domain. This difference is caused by the Padé approximation of e^{sT_s}. As a increases from 0 to 1, f_{ci}/f_s increases form 0.3 to 0.55.

The phase of the current-loop gain is

$$\begin{aligned}\phi_{Ti} &= -90^\circ - \arctan\left(\frac{\omega}{\omega_{sh}}\right) = -180^\circ - \arctan\left(\frac{\omega_{sh}}{\omega}\right) \\ &= -180^\circ + \arctan\left[\frac{3(1-a)}{\pi(1+a)}\left(\frac{f_s}{f}\right)\right].\end{aligned} \tag{13.101}$$

The phase ϕ_{Ti} at the crossover frequency f_{ci} is

$$\begin{aligned}\phi_{Ti}(f_{ci}) &= -180^\circ + arctan\left(\frac{f_{sh}}{f_{ci}}\right) = -180^\circ + arctan\left[\frac{3(1-a)}{\pi(1+a)}\left(\frac{f_s}{f_{ci}}\right)\right] \\ &= -180^\circ + arctan\left[\frac{3}{\sqrt{2}}\left(\frac{1-a}{1+a}\right)^2 \sqrt{1+\sqrt{1+\frac{4}{9}\left(\frac{1+a}{1-a}\right)^4}}\right].\end{aligned} \tag{13.102}$$

The phase margin of the current loop is defined as

$$PM = 180^\circ + \phi_{Ti}(f_{ci}). \tag{13.103}$$

Hence,

$$\tan PM = \frac{3}{\sqrt{2}}\left(\frac{1-a}{1+a}\right)^2\sqrt{1+\sqrt{1+\frac{4}{9}\left(\frac{1+a}{1-a}\right)^4}}. \tag{13.104}$$

Rearrangement of this equation gives the relationship between a and the phase margin PM,

$$a = \frac{\sqrt[4]{9(1+\tan^2 PM)}-\tan PM}{\sqrt[4]{9(1+\tan^2 PM)}+\tan PM}. \tag{13.105}$$

Figure 13.29 shows a plot of a as a function of PM. Once a is known, the required amount of compensation can be calculated. For converters without slope compensation, $a = D/(1-D)$ and the maximum duty cycle for a given phase margin PM is

$$D_{max} = \frac{a}{1+a} = \frac{\sqrt[4]{9(1+\tan^2 PM)}-\tan PM}{2\sqrt[4]{9(1+\tan^2 PM)}}. \tag{13.106}$$

Figure 13.30 shows D_{max} as a function of a. As a decreases from 1 to 0, D_{max} decreases from 0.5 to 0. The maximum duty cycle D_{max} is shown as a function of the phase margin PM in Figure 13.31. As PM increases from 0 to 72°, the maximum duty cycle D_{max} decreases from 0.5 to 0. For example, for $PM = 60^\circ$, $a = 0.1716$, resulting in $D_{max} = a/(1+a) = 0.1716/(1+0.1716) = 0.1665$ and $f_{ci}/f_s \approx 0.4$. Thus, almost all converters with current-mode control require slope compensation. For converters with slope compensation,

$$M_3 = \frac{M_2 - aM_1}{1+a} = M_1\frac{\dfrac{D}{1-D}-a}{1+a}, \tag{13.107}$$

yielding

$$D_{max} = \frac{a+(a+1)\dfrac{M_3}{M_1}}{(a+1)\left(1+\dfrac{M_3}{M_1}\right)}. \tag{13.108}$$

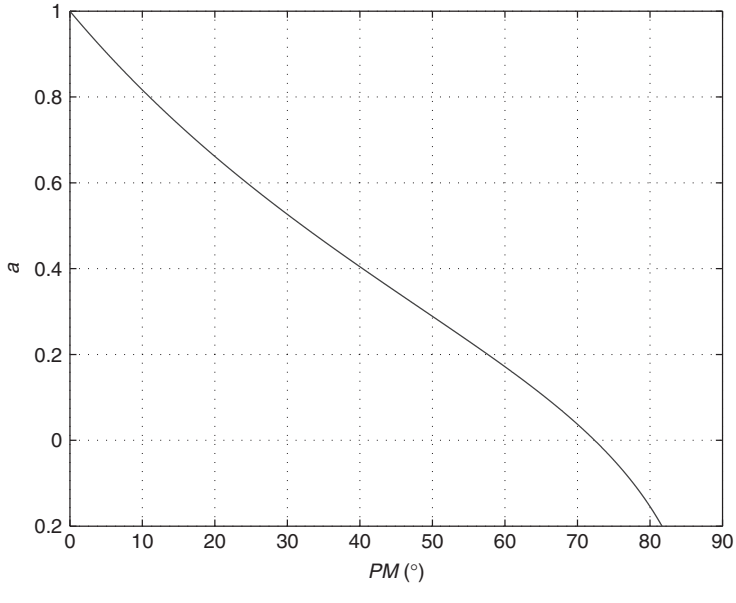


Figure 13.29 Parameter a as a function of PM.

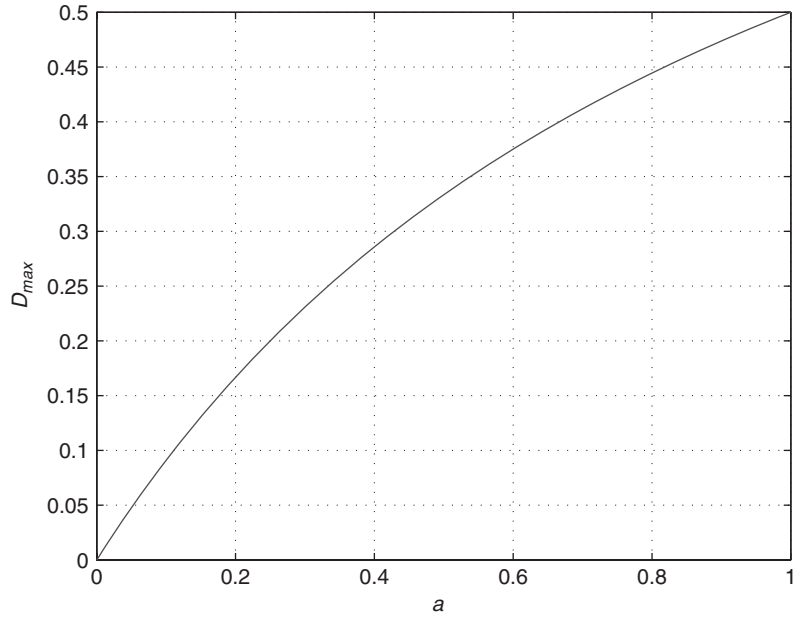


Figure 13.30 The maximum value of duty cycle D_{max} as a function of a without slope compensation.

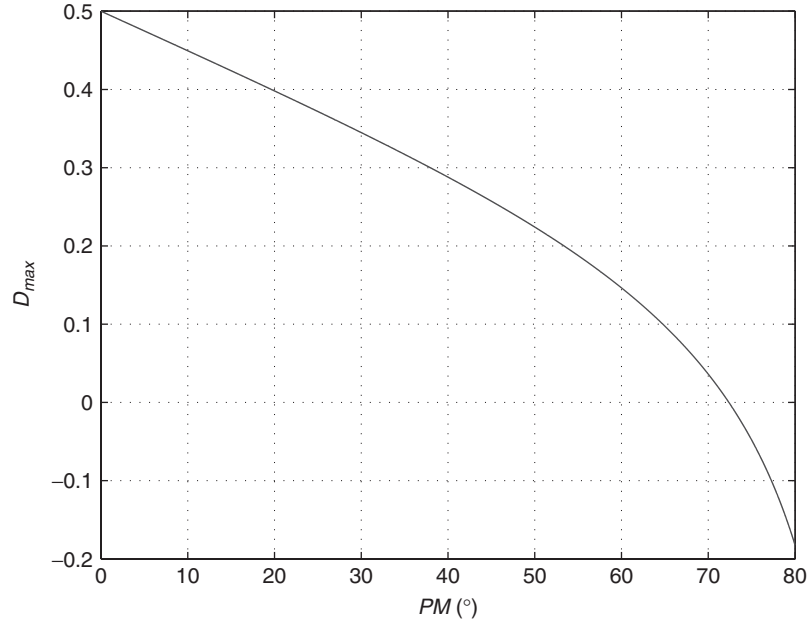


Figure 13.31 The maximum value of duty cycle D_{max} as a function of PM without slope compensation.

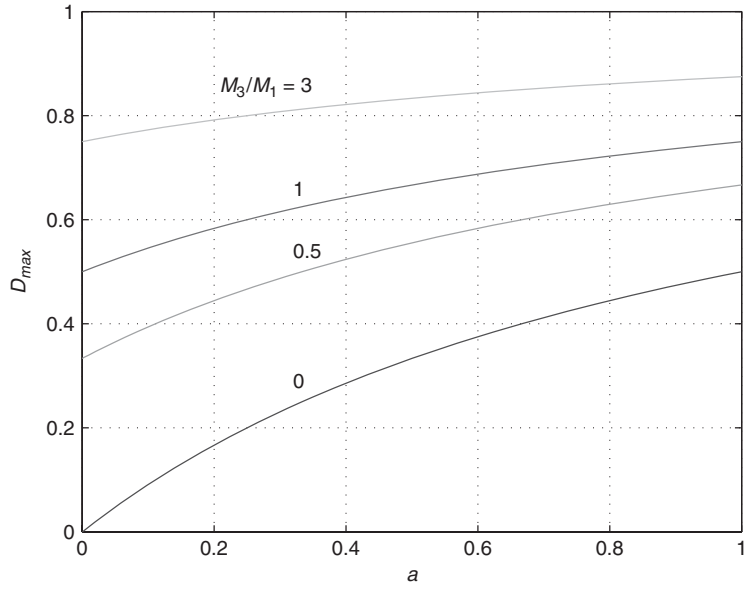


Figure 13.32 The maximum value of duty cycle D_{max} as a function of a at selected values of M_3/M_1.

Figure 13.32 shows D_{max} as a function of a at fixed values of M_3/M_1. The maximum duty cycle D_{max} as a function of PM is shown in Figure 13.33 for fixed values of M_3/M_1.

13.7.4 Closed-loop Transfer Function of Current Loop

Figure 13.34 shows a block diagram of the closed-current loop with the duty cycle as an output, as it is the case in actual converters. Using (13.96), the control voltage-to-duty cycle transfer function of the closed-current loop is

$$T_{icl}(s) = \frac{d(s)}{v_c(s)} = \frac{T_{ms}}{1 + T_{ms}T_{pi}R_s} = \frac{T_{ms}}{1 + T_i} = \frac{T_{ms}}{1 + \dfrac{12\,f_s^2}{s(s + \omega_{sh})}} = \frac{T_{ms}s(s + \omega_{sh})}{s(s + \omega_{sh}) + 12\,f_s^2}. \tag{13.109}$$

Substitution of (13.89) into this equation yields

$$\begin{aligned} T_{icl}(s) &= \frac{12\,f_s^2}{R_s T_{pi}[s(s + \omega_{sh}) + 12\,f_s^2]} = \frac{12\,f_s^2}{R_s T_{pi}s(s + \omega_{sh})} \\ &= \frac{12\,f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix}(s^2 + \omega_{sh}s + 12\,f_s^2)(s + \omega_{zi1})} = T_{iclx}\frac{(s^2 + 2\xi\omega_0 s + \omega_0^2)}{(s^2 + \dfrac{1 - a}{1 + a}6\,f_s s + 12\,f_s^2)(s + \omega_{zi1})} \\ &= T_{iclx}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{s^3 + (\omega_{sh} + \omega_{zi1})s^2 + (12\,f_s^2 + \omega_{sh}\omega_{zi1})s + 12\,f_s^2\omega_{zi1}}, \end{aligned} \tag{13.110}$$

where

$$T_{iclx} = \frac{12\,f_s^2}{R_s T_{pix}}. \tag{13.111}$$

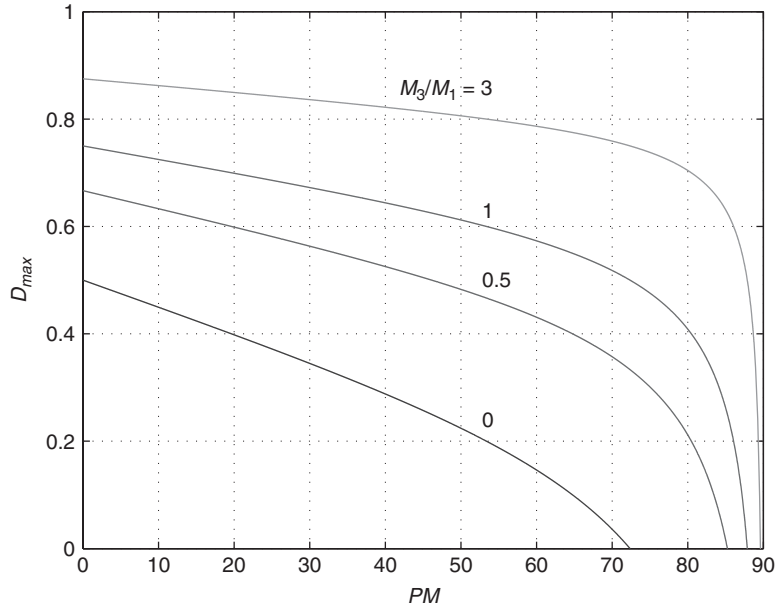


Figure 13.33 The maximum value of duty cycle D_{max} as a function of PM at selected values of M_3/M_1.

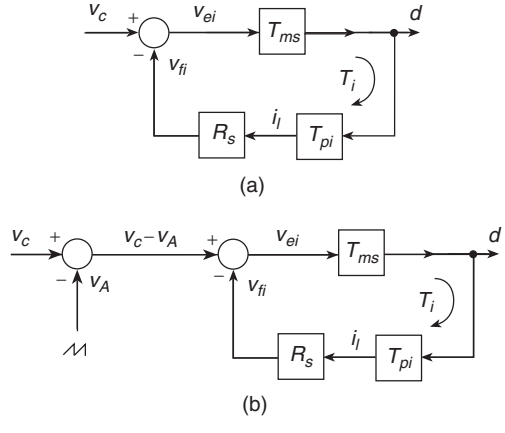


Figure 13.34 Block diagram of the closed-current loop showing the transfer function from control voltage to the duty cycle d, as in actual converters. The disturbances are zero (i.e., $v_i = 0$ and $i_o = 0$.) (a) Without slope compensation. (b) With slope compensation.

The two poles of T_{icl} are

$$p_{i1}, p_{i2} = -\xi_i \omega_i \pm j\omega_i \sqrt{1-\xi_i^2} = -\frac{1-a}{1+a} 3 f_s \pm j 2\sqrt{3} f_s \sqrt{1 - \frac{3}{4}\left(\frac{1-a}{1+a}\right)^2}. \quad (13.112)$$

The closed-current loop transfer function depends on the converter topology, slope compensation, and sample-and-hold effect. Figures 13.35 and 13.36 show Bode plots for the closed-current loop T_{icl} at selected values of a for a buck-boost converter as an example. It can be seen that the magnitude of T_{icl} exhibits peaking at $f_s/2$ for $a = 0.5$ and 0.9. For

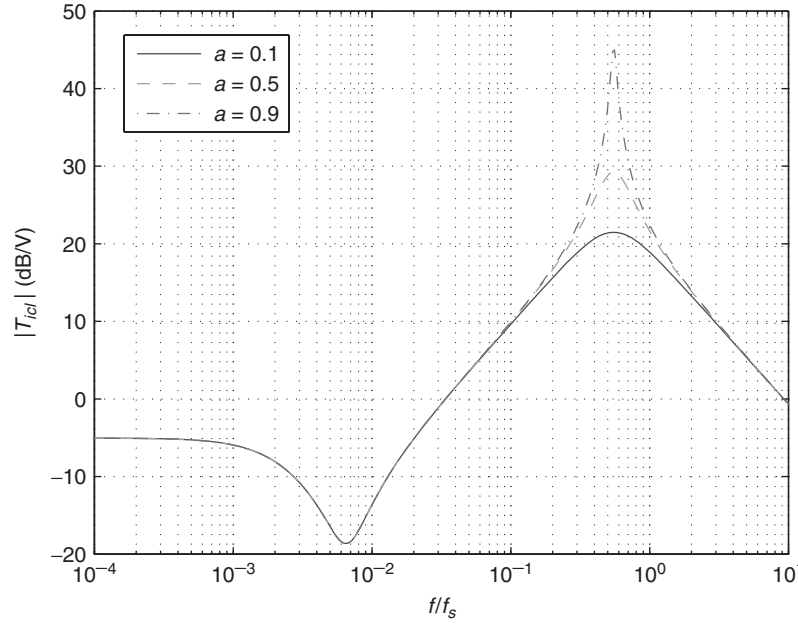


Figure 13.35 Bode plot of the magnitude of the closed-current loop $T_{icl}(s)$ for selected values of a.

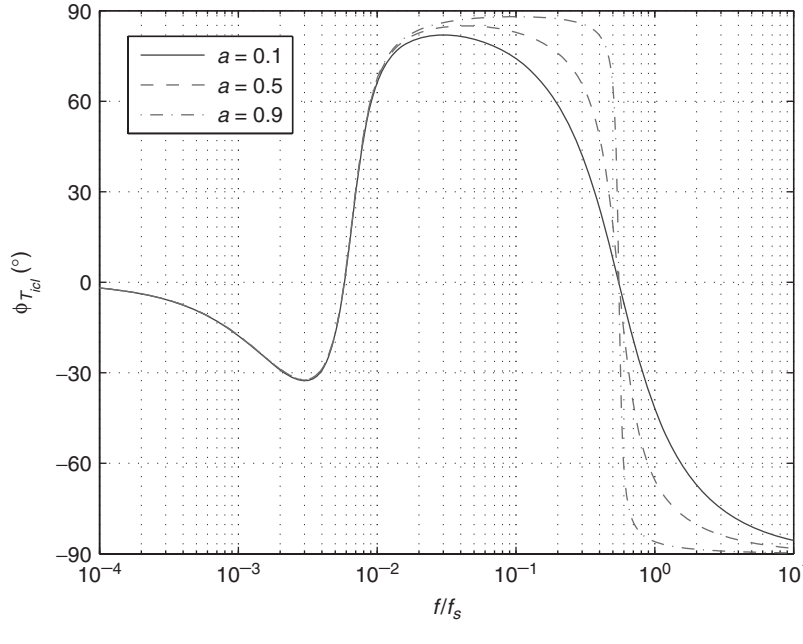


Figure 13.36 Bode plot of the phase of closed-current loop $T_{icl}(s)$ for selected values of a.

$a = 1$, $|T_{icl}|$ approaches infinity at $f_s/2$. For $a > 1$, T_{icl} has two poles in the RHP, making the current loop unstable. The phase ϕ_{Ticl} has positive values close to 90° at high frequencies, and therefore the closed-current loop acts like a partial lead compensator for the outer voltage loop, helping to offset the negative phase of T_p introduced, for example, by the RHP zero for the boost and buck-boost converters, which are nonminimal phase circuits. Alternatively, the positive phase ϕ_{Ticl} of the closed-current loop may partially offset the negative phase introduced by the poles in all converters, for example, a buck converter.

13.7.5 Alternative Representation of Current Loop

An alternative method of representation of current loop is shown in Figure 13.37. The closed-loop transfer function of the current loop is

$$T_{icl}(s) = \frac{d(s)}{v_c(s)} = \frac{i_l(s)}{v_c(s)} \times \frac{d(s)}{i_l(s)} = H_{icl}(s) \times \frac{1}{T_{pi}(s)} = \frac{12 f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix}(s^2 + \omega_{sh}s + 12 f_s^2)(s + \omega_{zi1})}$$

$$= T_{iclx}\frac{(s^2 + 2\xi\omega_0 s + \omega_0^2)}{(s^2 + \frac{1-a}{1+a}6 f_s s + 12 f_s^2)(s + \omega_{zi1})}. \tag{13.113}$$

13.7.6 Current Loop with Disturbances

Figure 13.38 depicts a block diagram of the current loop with disturbances by the input voltage v_i and the load current i_o. Figure 13.39 shows block diagram for determining the transfer function from the input voltage to the duty cycle for closed-current loop. The inductor current is given by

$$i_l = i_l{}' + i_l{}'' = T_{pi}d + M_{vi}v_i, \tag{13.114}$$

and the duty cycle is

$$d = T_{ms}(-R_s i_l) = -T_{ms}R_s T_{pi}d - T_{ms}R_s M_{vi}v_i, \tag{13.115}$$

resulting in

$$d(1 + T_{ms}R_s T_{pi}) = -T_{ms}R_s M_{vi}v_i. \tag{13.116}$$

Hence, the input voltage-to-duty cycle transfer function is

$$M_{vd}(s) \equiv \left.\frac{d(s)}{v_i(s)}\right|_{v_c = i_o = 0} = -\frac{R_s T_{ms} M_{vi}}{1 + T_i}. \tag{13.117}$$

Figure 13.40 shows a block diagram for determining the transfer function from the load current to the duty cycle for the closed-current loop. From this block diagram, we obtain the inductor current

$$i_l = i_l' - i_l{}''' = T_{pi}d - A_i i_o \tag{13.118}$$

and the duty cycle

$$d = -T_{ms}R_s i_l = -T_{ms}R_s T_{pi}d + T_{ms}R_s A_i i_o, \tag{13.119}$$

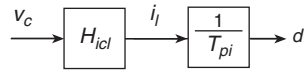


Figure 13.37 Block diagram for the alternative representation of T_{icl} for PWM converters.

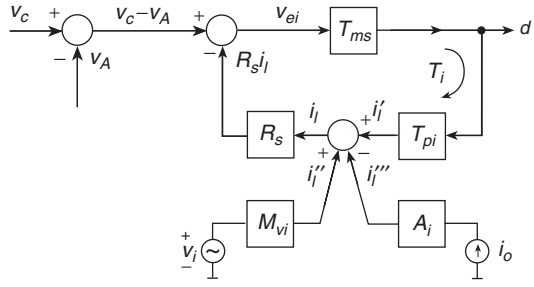


Figure 13.38 Block diagram of current loop with disturbances.

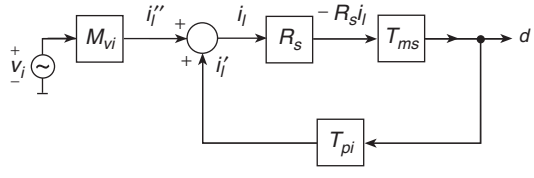


Figure 13.39 Block diagram for determining the input voltage-to-duty cycle transfer function M_{vd} for closed-current loop.

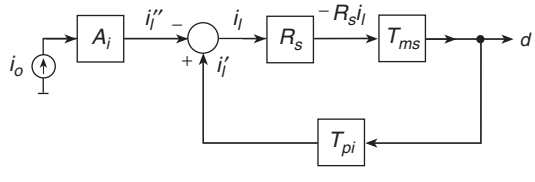


Figure 13.40 Block diagram for determining the load-current-to-duty cycle transfer function A_{id} for closed-current loop.

yielding

$$d(1 + T_{ms}R_s T_{pi}) = T_{ms}R_s A_i i_o. \tag{13.120}$$

Hence, we obtain the load current-to-duty cycle transfer function

$$A_{id}(s) \equiv \frac{d(s)}{i_o(s)}\,|_{v_c = v_i = 0} = \frac{R_s T_{ms} A_i}{1 + T_i}. \tag{13.121}$$

13.7.7 Modified Approximation of Current Loop

A modified Padé approximation [25] can be obtained by placing the corner frequency f_h at half the switching frequency f_s, yielding

$$e^{-sT_s} \approx \frac{1 - \dfrac{1}{2/\pi}\left(\dfrac{s}{\omega_s/2}\right) + \left(\dfrac{s}{\omega_s/2}\right)^2}{1 + \dfrac{1}{2/\pi}\left(\dfrac{s}{\omega_s/2}\right) + \left(\dfrac{s}{\omega_s/2}\right)^2} = \frac{1 - \dfrac{s}{2f_s} + \dfrac{s^2}{(\pi f_s)^2}}{1 + \dfrac{s}{2f_s} + \dfrac{s^2}{(\pi f_s)^2}} = \frac{1 - \dfrac{sT_s}{2} + \dfrac{(sT_s)^2}{\pi^2}}{1 + \dfrac{sT_s}{2} + \dfrac{(sT_s)^2}{\pi^2}}. \tag{13.122}$$

Hence, (13.76) becomes

$$H_{iclm}(s) \approx \frac{1}{R_s}\frac{1}{1+\dfrac{1-a}{1+a}\dfrac{1}{2/\pi}\left(\dfrac{s}{\omega_s/2}\right)+\left(\dfrac{s}{\omega_s/2}\right)^2} = \frac{1}{R_s}\frac{(\omega_s/2)^2}{s^2+\dfrac{\pi}{4}\dfrac{1-a}{1+a}\omega_s s+(\omega_s/2)^2}$$

$$= \frac{1}{R_s}\frac{\pi^2 f_s^2}{s^2+\dfrac{\pi^2 f_s}{2}\dfrac{1-a}{1+a}s+\pi^2 f_s^2} = \frac{1}{R_s}\frac{\omega_h^2}{s^2+2\xi_h\omega_h s+\omega_h^2}, \tag{13.123}$$

where

$$\omega_h = \frac{\omega_s}{2} = \pi f_s, \tag{13.124}$$

$$\xi_h = \frac{\pi}{4}\left(\frac{1-a}{1+a}\right), \tag{13.125}$$

$$Q_h = \frac{2}{\pi}\left(\frac{1+a}{1-a}\right), \tag{13.126}$$

and

$$p_1, p_2 = -\omega_h\xi_h \pm j\omega_h\sqrt{1-\xi_h^2} = -\frac{\pi^2 f_s}{4}\frac{1-a}{1+a} \pm j\pi f_s\sqrt{1-\frac{\pi^2}{16}\left(\frac{1-\alpha}{1+\alpha}\right)^2}. \tag{13.127}$$

Substitution of (13.122) into (13.88) gives the normalized sample-and-hold transfer function

$$H_{sh}(s) \approx \frac{\pi^2 f_s^2}{R_s T_m T_{pi} s\left(s+\dfrac{\pi^2}{2}\dfrac{1-a}{1+a}f_s\right)} = \frac{\pi^2 f_s^2}{R_s T_m T_{pi} s\,(s+\omega_{shm})}, \tag{13.128}$$

where

$$\omega_{shm} = \frac{\pi^2}{2}\frac{1-a}{1+a}f_s = \left(\frac{\pi}{4}\right)\frac{1-a}{1+a}\omega_s = \left(\frac{\pi}{2}\right)\frac{1-a}{1+a}\omega_h. \tag{13.129}$$

The normalized sample-and-hold transfer function for any converter is obtained as

$$H_{sh}(s) \approx \frac{\pi^2 f_s^2(s^2+2\xi\omega_0 s+\omega_0^2)}{R_s T_m T_{pix} s(s+\omega_{zi1})(s+\omega_{shm})}. \tag{13.130}$$

The error voltage-to-duty cycle transfer function of the current loop is

$$T_{ms}(s) = \frac{d(s)}{v_{ei}(s)} \approx \frac{\pi^2 f_s^2(s^2+2\xi\omega_0 s+\omega_0^2)}{R_s T_{pix} s(s+\omega_{zi1})(s+\omega_{shm})}. \tag{13.131}$$

The loop gain of the current loop is given by

$$T_{im}(s) = \frac{v_{fi}(s)}{v_{ei}(s)} = T_{ms}T_{pi}R_s \approx \frac{\pi^2 f_s^2}{s\left(s+\dfrac{1-a}{1+a}\dfrac{\pi^2}{2}f_s\right)} = \frac{\pi^2 f_s^2}{s\,(s+\omega_{shm})} = \frac{\pi^2 f_s^2}{\omega_{sh}s\left(1+\dfrac{s}{\omega_{sh}}\right)}. \tag{13.132}$$

The magnitude of the current-loop gain is

$$|T_{im}| = \frac{\pi^2 f_s^2}{\omega}\frac{1}{\sqrt{\omega^2+\omega_{shm}^2}} = \frac{1}{4}\left(\frac{f_s}{f}\right)^2\frac{1}{\sqrt{1+\left(\dfrac{f_{shm}}{f}\right)^2}}$$

$$= \frac{1}{4}\left(\frac{f_s}{f}\right)^2\frac{1}{\sqrt{1+\dfrac{\pi^4}{16}\left(\dfrac{1-a}{1+a}\right)^2\left(\dfrac{f_s}{f}\right)^2}}. \tag{13.133}$$

At the crossover frequency f_{cim}, the magnitude of the current-loop gain becomes

$$|T_{im}(f_{cim})| = \frac{1}{4}\left(\frac{f_s}{f_{cim}}\right)^2 \frac{1}{\sqrt{1+\left(\frac{f_{sh}}{f_{cim}}\right)^2}} = \frac{1}{4}\left(\frac{f_s}{f_{cim}}\right)^2 \frac{1}{\sqrt{1+\frac{\pi^4}{16}\left(\frac{1-a}{1+a}\right)^2\left(\frac{f_s}{f_{cim}}\right)^2}} = 1. \tag{13.134}$$

Thus, the normalized crossover frequency of the current loop is

$$\frac{f_{cim}}{f_s} = \frac{1}{2\sqrt{\frac{\pi^2}{8}\left(\frac{1-a}{1+a}\right)^2 + \sqrt{\frac{\pi^4}{64}\left(\frac{1-a}{1+a}\right)^4 + 1}}}. \tag{13.135}$$

For $a = 1, f_{cim}/f_s = 1/2$, the current loop is unstable and oscillates at half of the switching frequency, as predicted in the time domain. Figure 13.41 shows plots of f_{ci}/f_s and f_{cim}/f_s. As a increases from 0 to 1, f_{cim}/f_s increases from 0.3 to 0.5.

The phase of the current-loop gain is

$$\begin{aligned}\phi_{Ti} &= -90^\circ - \arctan\left(\frac{\omega}{\omega_{shm}}\right) = -180^\circ + \arctan\left(\frac{\omega_{shm}}{\omega}\right) \\ &= -180^\circ + \arctan\left[\frac{\pi(1-a)}{4(1+a)}\left(\frac{f_s}{f}\right)\right].\end{aligned} \tag{13.136}$$

The phase ϕ_{Ti} at the crossover frequency f_{cim} is

$$\begin{aligned}\phi_{Ti}(f_{cim}) &= -180^\circ + \arctan\left(\frac{f_{shm}}{f_{ci}}\right) = -180^\circ + \arctan\left[\frac{\pi(1-a)}{4(1+a)}\left(\frac{f_s}{f_{cim}}\right)\right] \\ &= -180^\circ + \arctan\left[\frac{\pi(1-a)}{2(1+a)}\sqrt{\frac{\pi^2}{8}\left(\frac{1-a}{1+a}\right)^2 + \sqrt{\frac{\pi^4}{64}\left(\frac{1-a}{1+a}\right)^4 + 1}}\right].\end{aligned} \tag{13.137}$$

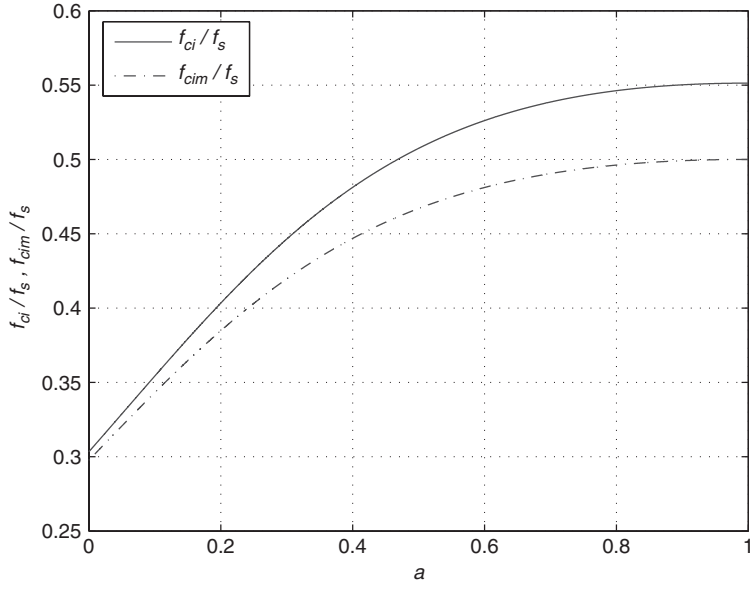


Figure 13.41 Crossover frequencies f_{ci}/f_s and f_{cim}/f_s as functions of a.

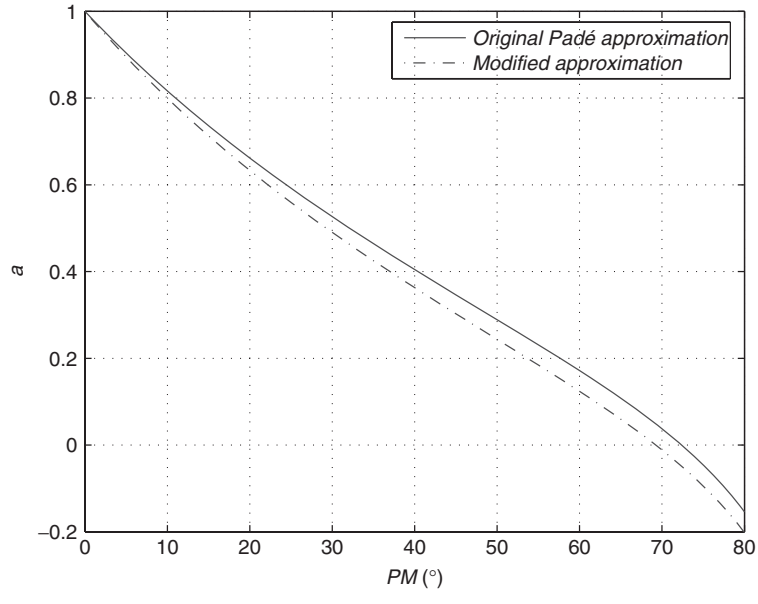


Figure 13.42 a as a function of phase margin PM for the Padé approximation and for the modified approximation.

The phase margin of the current loop is defined as

$$PM = 180^\circ + \phi_{Ti}(f_{cim}). \tag{13.138}$$

Thus,

$$\tan PM = \frac{\pi(1-a)}{2(1+a)}\sqrt{\frac{\pi^2}{2}\left(\frac{1-a}{1+a}\right)^2 + \sqrt{\frac{\pi^4}{4}\left(\frac{1-a}{1+a}\right)^4 + 1}}, \tag{13.139}$$

yielding the relationship between a and PM,

$$a = \frac{\sqrt[4]{(1+\tan^2 PM)} - \dfrac{2}{\pi}\tan PM}{\sqrt[4]{(1+\tan^2 PM)} + \dfrac{2}{\pi}\tan PM}. \tag{13.140}$$

Figure 13.42 shows a as a function of PM for the Padé approximation and for the modified approximation.

The control voltage-to-duty cycle transfer function of the closed-current loop is given by

$$T_{iclm}(s) = \frac{H_m(s)}{T_{pi}(s)} = \frac{\pi^2 f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix}(s^2 + \omega_{shm}s + \pi^2 f_s^2)(s + \omega_{zi1})}. \tag{13.141}$$

13.8 Voltage Loop of PWM Converters with Current-mode Control

Figure 13.43 shows a block diagram of open-loop PWM converters. Figure 13.44 shows a block diagram of PWM converters with current-mode control without feedforward gains,

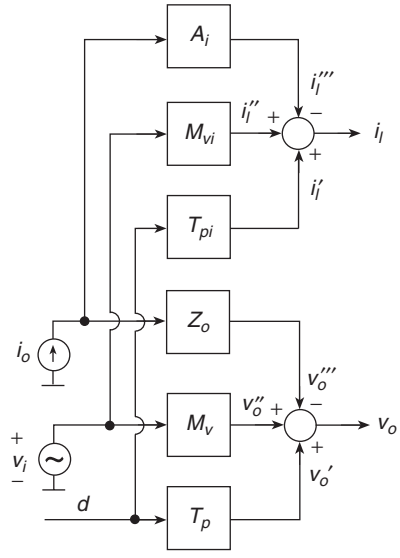


Figure 13.43 Block diagram of the power stage of PWM converters.

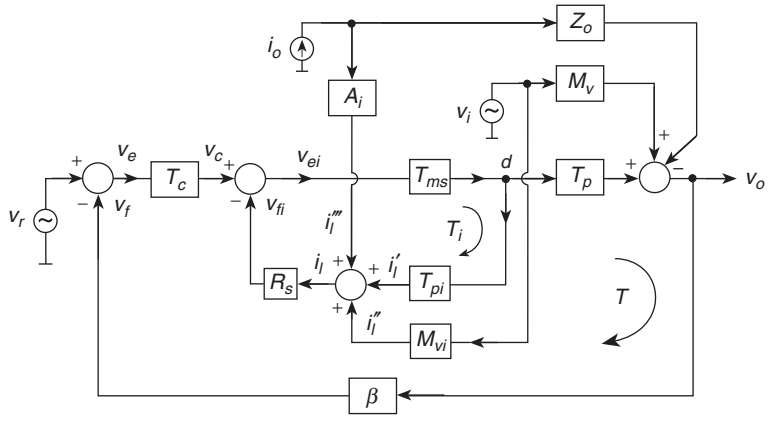


Figure 13.44 Current-mode control block diagram of PWM converters without feedforward gains.

where i_l is the small-signal component of the average inductor current, $T_{pi} = i_l/d$ is the open-loop duty cycle-to-inductor current transfer function, $M_{vi} = i_l/v_i$ is the open-loop input voltage-to-inductor current transfer function, $T_p = v_o/d$ is the open-loop duty cycle-to-output voltage transfer function, $M_v = v_o/v_i$ is the open-loop input voltage-to-output voltage transfer function, and $T_c = v_c/v_e$ is the voltage transfer function of the control circuit. Figure 13.45 shows a block diagram of PWM converters with peak current-mode control for the critical paths only without disturbances, that is, for v_i and $i_o = 0$, where the peak inductor current is controlled along with the output voltage. The current loop T_i controls the peak inductor current and the voltage loop T controls the output voltage.

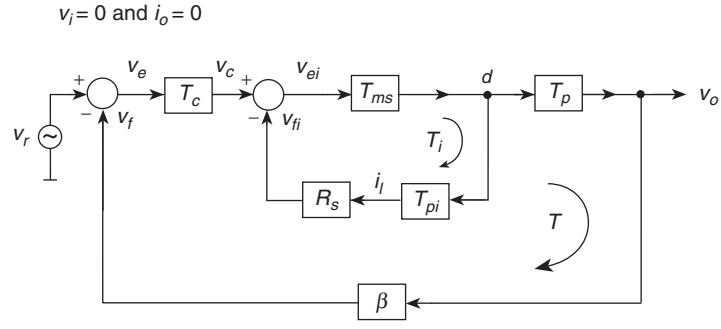


Figure 13.45 Block diagram for the critical path of closed-loop PWM converters with current-mode control at $v_i = 0$ and $i_o = 0$.

13.8.1 Closed-voltage Loop Transfer Function

The closed-loop transfer function from the reference voltage v_r to the output voltage v_o is

$$T_{cl} \equiv \frac{v_o}{v_r} \mid_{v_i = i_o = 0} = \frac{T_c T_{icl} T_p}{1 + T_c T_{icl} T_p \beta}. \tag{13.142}$$

13.8.2 Closed-loop Audio Susceptibility

Figure 13.46 shows a block diagram for determining the closed-loop audio susceptibility, which can be obtained by setting $v_r = 0$ and $i_o = 0$. The derivation of this transfer function is as follows:

$$i_l' = T_{pi} d, \tag{13.143}$$

$$i_l'' = M_{vi} v_i, \tag{13.144}$$

$$i_l = i_l' + i_l'' = T_{pi} d + M_{vi} v_i, \tag{13.145}$$

$$v_{fi} = R_s i_l = R_s T_{pi} d + R_s M_{vi} v_i, \tag{13.146}$$

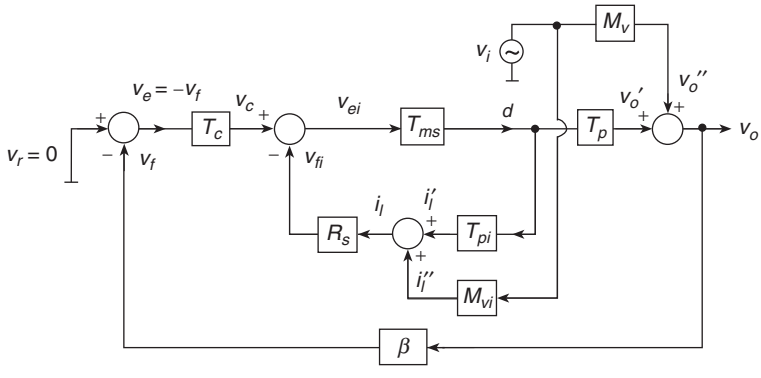


Figure 13.46 Block diagram of PWM converters with current-mode control for determining the closed-loop audio susceptibility.

$$v_{ei} = v_c - v_{fi} = v_c - R_s T_{pi} d - R_s M_{vi} v_i, \tag{13.147}$$

$$v_f = \beta v_o, \tag{13.148}$$

$$v_e = -v_f = -\beta v_o, \tag{13.149}$$

$$v_c = T_c v_e = -\beta T_c v_o, \tag{13.150}$$

$$v_{ei} = v_c - v_{fi} = -\beta T_c v_o - R_s T_{pi} d - R_s M_{vi} v_i, \tag{13.151}$$

$$d = T_{ms} v_{ei} = -\beta T_c T_{ms} v_o - R_s T_{pi} T_{ms} d - R_s M_{vi} T_{ms} v_i \tag{13.152}$$

$$d = -\frac{\beta T_c T_{ms}}{1 + R_s T_{pi} T_{ms}} v_o - \frac{R_s M_{vi} T_{ms}}{1 + R_s T_{pi} T_{ms}} v_i, \tag{13.153}$$

$$v_o' = T_p d = -\frac{\beta T_c T_{ms} T_p}{1 + R_s T_{pi} T_{ms}} v_o - \frac{R_s M_{vi} T_{ms} T_p}{1 + R_s T_{pi} T_{ms}} v_i, \tag{13.154}$$

$$v_o'' = M_v v_i, \tag{13.155}$$

$$v_o = v_o' + v_o'' = -\frac{\beta T_c T_{ms} T_p}{1 + R_s T_{pi} T_{ms}} v_o - \frac{R_s M_{vi} T_{ms} T_p}{1 + R_s T_{pi} T_{ms}} v_i + M_v v_i, \tag{13.156}$$

$$v_o(1 + T_i + T_v) = [M_v + T_i M_v - R_s T_{ms} T_p M_{vi}] v_i, \tag{13.157}$$

$$v_o(1 + T_i + T_v) = [M_v + T_i M_v - T_{ms} T_{pi} R_s T_p M_{vi} / T_{pi}] v_i, \tag{13.158}$$

$$v_o(1 + T_i + T_v) = [M_v + T_i M_v - T_i T_p M_{vi} / T_{pi}] v_i, \tag{13.159}$$

where

$$T_v = T_c T_{ms} T_p \beta. \tag{13.160}$$

Finally, the closed-loop audio susceptibility is given by

$$M_{vcl} \equiv \left.\frac{v_o}{v_i}\right|_{v_r = i_o = 0} = \frac{M_v + T_i M_v - R_s T_{ms} T_p M_{vi}}{1 + T_i + T_v} = \frac{M_v + T_p T_i \left(\dfrac{M_v}{T_p} - \dfrac{M_{vi}}{T_{pi}}\right)}{1 + T_i + T_v}. \tag{13.161}$$

13.8.3 Closed-loop Output Impedance

Figure 13.47 shows a block diagram for determining the closed-loop output impedance, obtained by setting $v_r = 0$ and $v_i = 0$. The derivation of this impedance is as follows:

$$i_l' = T_{pi} d, \tag{13.162}$$

$$i_l'' = A_i i_o, \tag{13.163}$$

$$i_l = i_l' + i_l'' = T_{pi} d + A_i i_o, \tag{13.164}$$

$$v_{fi} = R_s i_l = R_s T_{pi} d + R_s A_i i_o, \tag{13.165}$$

$$v_f = \beta v_o, \tag{13.166}$$

$$v_e = -v_f = -\beta v_o, \tag{13.167}$$

$$v_c = T_c v_e = -\beta T_c v_o, \tag{13.168}$$

$$v_{ei} = v_c - v_{fi} = -\beta T_c v_o - R_s T_{pi} d - R_s A_i i_o, \tag{13.169}$$

$$d = T_{ms} v_{ei} = -T_{ms} \beta T_c v_o - T_{ms} T_{pi} R_s d - R_s A_i T_{ms} i_o, \tag{13.170}$$

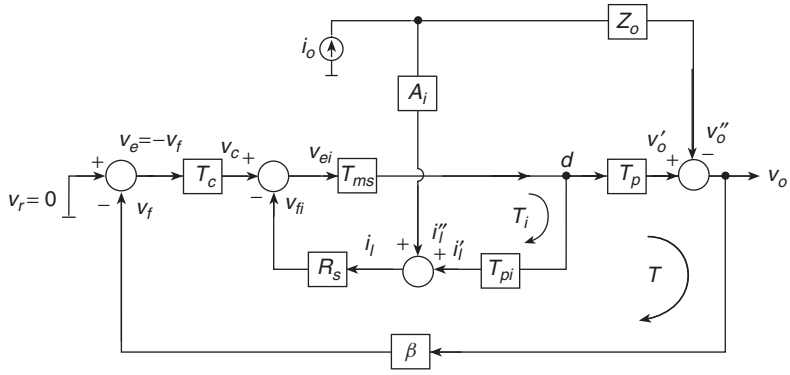


Figure 13.47 Block diagram of PWM converters with current-mode control for determining the closed-loop output impedance.

$$d(1 + T_{ms}T_{pi}R_s) = -T_{ms}\beta T_c v_o - R_s A_i T_{ms} i_o, \tag{13.171}$$

$$d = -\frac{T_{ms}\beta T_c}{1 + T_{ms}T_{pi}R_s} v_o - \frac{R_s T_{ms} A_i}{1 + T_{ms}T_{pi}R_s} i_o, \tag{13.172}$$

$$v_o' = T_p d = -\frac{T_{ms}\beta T_c T_p}{1 + T_{ms}T_{pi}R_s} v_o - \frac{R_s T_{ms} A_i T_p}{1 + T_{ms}T_{pi}R_s} i_o, \tag{13.173}$$

$$v_o'' = -Z_o i_o, \tag{13.174}$$

$$v_o = v_o' + v_o'' = -\frac{T_{ms}\beta T_c T_p}{1 + T_{ms}T_{pi}R_s} v_o - \frac{R_s T_{ms} A_i T_p}{1 + T_{ms}T_{pi}R_s} i_o - Z_o i_o, \tag{13.175}$$

$$v_o(1 + T_i + T_v) = -[Z_o(1 + T_i) + R_s T_{ms} A_i T_p] i_o. \tag{13.176}$$

Finally, the closed-loop output impedance is

$$Z_{ocl} \equiv -\frac{v_o}{i_o}\Big|_{v_r = v_i = 0} = \frac{Z_o(1 + T_i) + R_s T_{ms} A_i T_p}{1 + T_i + T_v}. \tag{13.177}$$

13.9 Feedforward Gains in PWM Converters with Current-mode Control without Slope Compensation

The preceding analysis was performed under the assumption of fixed converter input voltage V_I and output voltage V_O. Let us relax this assumption and consider the case for which the input and output voltages consist of dc and small-signal ac components: $v_I = V_I + v_i$ and $v_O = V_O + v_o$. The slopes of the inductor current waveform depend on the input and/or output voltages. When the input and output voltages contain small-signal ac components, the slopes also contain dc and small-signal components: $m_{T1} = M_1 + m_1$ and $m_{T2} = M_2 + m_2$. Figure 13.48 shows the waveforms in PWM converters with current-mode control and without slope compensation, where the control voltage V_C is held constant and the slope of the rising inductor current waveform is increased by a small change m_1 from the steady-state value M_1 to $M_1 + m_1$. This causes the duty cycle to decrease from D to $d_T = D + d$, where

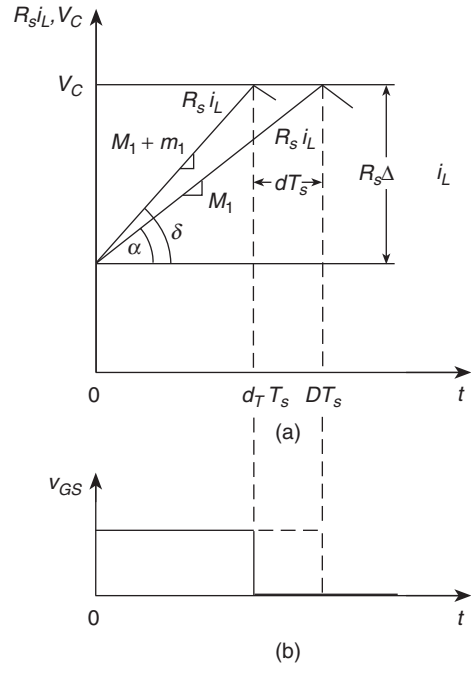


Figure 13.48 Waveforms of the inductor current with steady-state slope M_1 and with perturbed slope $M_1 + m_1$ at fixed control voltage V_C in PWM converter with current-mode control and without slope compensation. (a) Waveforms of the inductor and control currents. (b) Waveform of the gate-to-source voltage.

$d < 0$. The slopes of the rising inductor current waveforms before and after perturbation are

$$M_1 = \tan\alpha = \frac{R_s \Delta i_L}{DT_s} \tag{13.178}$$

and

$$M_1 + m_1 = \tan\delta = \frac{R_s \Delta i_L}{d_T T_s} = \frac{R_s \Delta i_L}{(D+d)T_s}. \tag{13.179}$$

These two equations lead to

$$M_1 D = (M_1 + m_1)(D + d), \tag{13.180}$$

from which

$$M_1 D = M_1 D + M_1 d + D m_1 + m_1 d. \tag{13.181}$$

If $m_1 d \ll M_1 d$ and $m_1 d \ll D m_1$, that is, if the small-signality conditions $m_1 \ll M_1$ and $d \ll D$ are satisfied, the product of the small-signal components $m_1 d$ can be neglected. Hence, one obtains a general and linear relationship between m_1 and d given by [36]

$$d = -\frac{D}{M_1} m_1. \tag{13.182}$$

For the buck converter,

$$M_1 + m_1 = \frac{v_I - v_O}{L} = \frac{(V_I + v_i) - (V_O + v_o)}{L} = \frac{V_I - V_O}{L} + \frac{v_i - v_o}{L}, \tag{13.183}$$

where

$$m_1 = \frac{v_i - v_o}{L} \tag{13.184}$$

and M_1 is given by (13.7). As a result, (13.182) becomes [36]

$$d = -\frac{D}{V_I - V_O}(v_i - v_o) = -\frac{D}{V_I - V_O}v_i + \frac{D}{V_I - V_O}v_o = K_i v_i + K_o v_o. \tag{13.185}$$

Using $D = V_O/V_I$, the input feedforward gain is given by

$$K_i \equiv \frac{d}{v_i}|_{v_c=0 \text{ and } v_o=0} = -\frac{D}{V_I - V_O} = -\frac{D^2}{(1-D)V_O}, \tag{13.186}$$

and the output feedforward gain is given by

$$K_o \equiv \frac{d}{v_o}|_{v_c=0 \text{ and } v_i=0} = \frac{D}{V_I - V_O} = \frac{D^2}{(1-D)V_O} = -K_i, \tag{13.187}$$

yielding

$$d = K_i(v_i - v_o) = -\frac{D^2}{(1-D)V_O}(v_i - v_o). \tag{13.188}$$

For the boost and buck-boost converters,

$$M_1 + m_1 = \frac{v_I}{L} = \frac{V_I + v_i}{L} = \frac{V_I}{L} + \frac{v_i}{L}, \tag{13.189}$$

where

$$m_1 = \frac{v_i}{L} \tag{13.190}$$

and M_1 is given by (13.9). Thus, from (13.182),

$$d = -\frac{D}{V_I}v_i = K_i v_i, \tag{13.191}$$

where the input feedforward gain is

$$K_i \equiv \frac{d}{v_i}|_{v_c=0} = -\frac{D}{V_I} \tag{13.192}$$

and the output feedforward gain is $K_o = 0$. For the boost converter, $V_I = (1-D)V_O$ and (13.192) becomes

$$K_i = -\frac{D}{V_I} = -\frac{D}{(1-D)V_O}. \tag{13.193}$$

For the buck-boost converter, $V_I = V_O(1-D)/D$ and (13.192) becomes

$$K_i = -\frac{D}{V_I} = -\frac{D^2}{(1-D)V_O}. \tag{13.194}$$

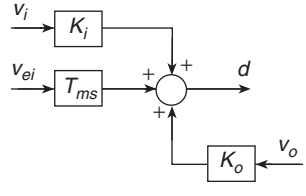


Figure 13.49 Block diagram of the current modulator that includes feedforward gains.

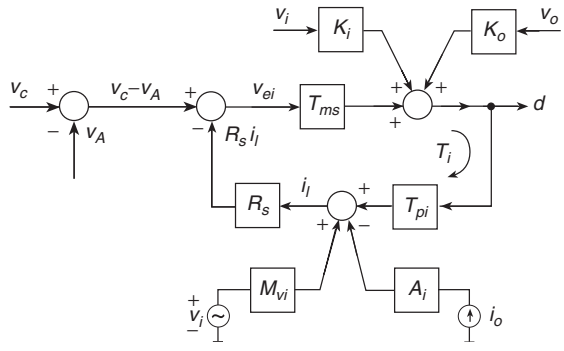


Figure 13.50 Block diagram of current loop with disturbances and feedforward gains.

Figure 13.49 shows a block diagram of the current-mode pulse-width modulator, in which the feedforward gains K_i and K_o are included. A block diagram of the current loop with feedforward gains and disturbances is shown in Figure 13.50.

13.10 Feedforward Gains in PWM Converters with Current-mode Control and Slope Compensation

Figure 13.51 shows the waveforms in PWM converters with current-mode control and slope compensation, where the control voltage V_C is held constant, the slope of the voltage $V_C - v_A$ remains constant, and the slope of the rising inductor current waveform is increased by a small amount m_1 from the steady-state value M_1 to $M_1 + m_1$. Note that $(D + d)T_s < DT_s$; therefore, $dT_s < 0$. The slopes of the rising inductor current waveforms are

$$M_1 = \tan\alpha = \frac{R_s \Delta i_{L0}}{DT_s}, \tag{13.195}$$

$$M_1 + m_1 = \tan\delta = \frac{R_s \Delta i_{L1}}{d_T T_s} = \frac{R_s \Delta i_{L1}}{(D + d)T_s}, \tag{13.196}$$

and the slope of the compensating ramp voltage $v_C - v_A$ is

$$-M_3 = \tan\gamma = \frac{R_s(\Delta i_{L1} - \Delta i_{L0})}{dT_s}. \tag{13.197}$$

Hence,

$$-M_3 d = (M_1 + m_1)(D + d) - M_1 D, \tag{13.198}$$

which simplifies to

$$-M_3 d = M_1 d + D m_1 + m_1 d. \tag{13.199}$$

If the small-signality conditions $m_1 \ll M_1$ and $d \ll D$ are satisfied, the product of the small-signal components $m_1 d$ can be neglected. Hence, one obtains [36]

$$d = -\frac{D}{M_1 + M_3} m_1 = -\frac{D}{M_1\left(1 + \dfrac{M_3}{M_1}\right)} m_1. \tag{13.200}$$

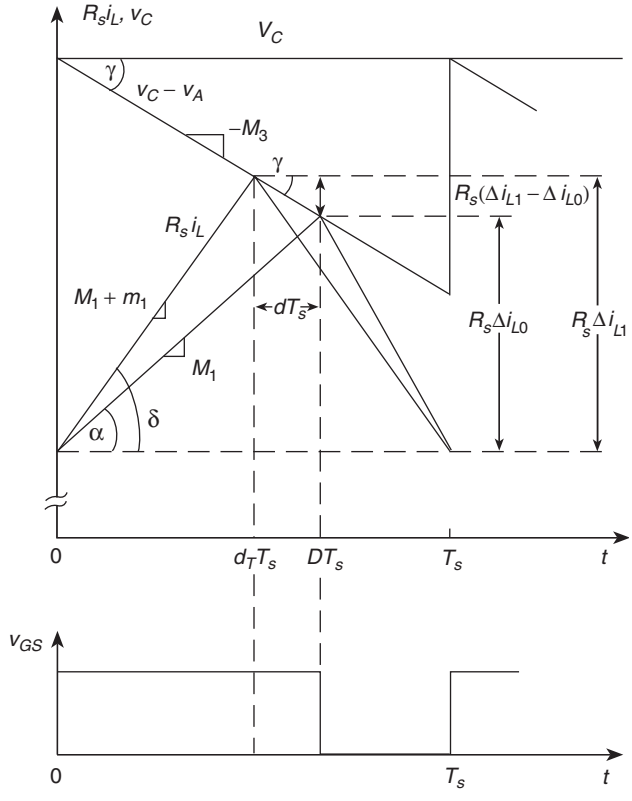


Figure 13.51 Waveforms of the inductor current with steady-state slope M_1 and with perturbed slope $M_1 + m_1$ for fixed control voltage V_C and compensating slope M_3 in PWM converter with current-mode control and slope compensation.

Substitution of (13.7) and (13.184) into (13.200) produces d for the buck converter,

$$d = -\frac{D}{\left(1+\frac{M_3}{M_1}\right)(V_I - V_O)}(v_i - v_o)$$

$$= -\frac{D}{\left(1+\frac{M_3}{M_1}\right)(V_I - V_O)}v_i + \frac{D}{\left(1+\frac{M_3}{M_1}\right)(V_I - V_O)}v_o, = K_i v_i + K_o v_o, \quad (13.201)$$

where the input feedforward gain is given by

$$K_i \equiv \left.\frac{d}{v_i}\right|_{v_c=0 \text{ and } v_o=0} = -\frac{D}{\left(1+\frac{M_3}{M_1}\right)(V_I - V_O)} = -\frac{D^2}{\left(1+\frac{M_3}{M_1}\right)(1-D)V_O} \quad (13.202)$$

and the output feedforward gain is given by

$$K_o \equiv \frac{d}{v_o}|_{v_c=0 \text{ and } v_i=0} = \frac{D}{\left(1+\frac{M_3}{M_1}\right)(V_I - V_O)} = \frac{D^2}{\left(1+\frac{M_3}{M_1}\right)(1-D)V_O} = -K_i. \quad (13.203)$$

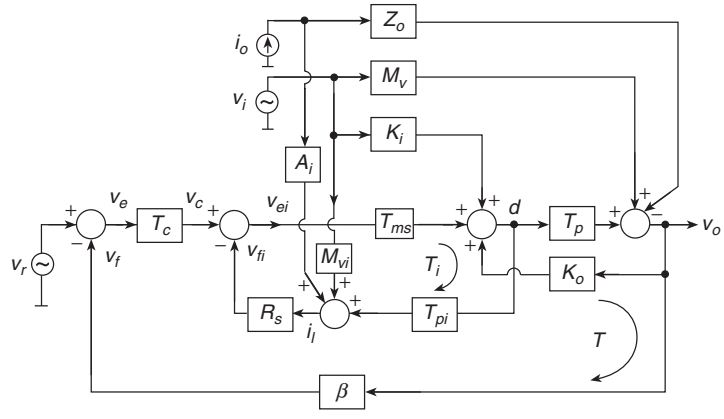


Figure 13.52 Control block diagram of a PWM converter with current-mode control, where the feedforward gains are included.

Using (13.9), (13.190), and (13.200), one arrives at d for the boost and buck-boost converters,

$$d = -\frac{D}{\left(1 + \dfrac{M_3}{M_1}\right) V_I} v_i = K_i v_i, \tag{13.204}$$

where the input feedforward gain is

$$K_i \equiv \frac{d}{v_i}|_{v_c=0} = -\frac{D}{\left(1 + \dfrac{M_3}{M_1}\right) V_I} \tag{13.205}$$

and the output feedforward gain is $K_o = 0$. For the boost converter, $V_I = (1 - D)V_O$ and (13.205) becomes

$$K_i = -\frac{D}{\left(1 + \dfrac{M_3}{M_1}\right)(1 - D)V_O}. \tag{13.206}$$

For the buck-boost converter, $V_I = V_O(1 - D)/D$ and (13.205) becomes

$$K_i = -\frac{D^2}{\left(1 + \dfrac{M_3}{M_1}\right)(1 - D)V_O}. \tag{13.207}$$

Figure 13.52 shows a control block diagram of a PWM converter with current-mode control, in which feedforward gains K_i and K_o are included.

13.11 Closed-loop Transfer Functions with Feedforward Gains

The loop gains are $T_c T_{ms} T_p \beta$, $T_{ms} T_{pi} R_s$, and $K_o T_p$. For the buck converter, the closed-loop transfer functions with feedforward gains are

$$T_{cl}\frac{v_o}{v_r} = \frac{T_c T_{icl} T_p}{1 + T_c T_{icl} T_p \beta + K_o T_p}, \tag{13.208}$$

$$M_{vcl} = \frac{v_o}{v_i} = \frac{M_v + K_i T_p}{1 + T_i + T_v + K_o T_p}, \tag{13.209}$$

and

$$Z_{ocl} = \frac{v_o}{-i_o} = \frac{Z_o(1 + T_i) + R_s T_{ms} A_i T_p}{1 + T_i + T_v + K_o T_p}. \tag{13.210}$$

Since $|K_o T_p| \ll |T_i|$, $K_o T_p$ in the denominator of the above equations can be neglected.

For the boost and buck-boost converters, $K_o = 0$ and the transfer functions with feedforward gains are

$$T_{icl} = \frac{v_o}{v_i} = \frac{T_c T_{cl} T_p}{1 + T_c T_{cl} T_p \beta}, \tag{13.211}$$

$$M_{vcl} = \frac{v_o}{v_i} = \frac{M_v + T_p T_i \left(\dfrac{M_v}{T_p} - \dfrac{M_{vi}}{T_{pi}} \right) + K_i T_p}{1 + T_i + T_v}, \tag{13.212}$$

and

$$Z_{ocl} = \frac{v_o}{-i_o} = \frac{Z_o(1 + T_i) + R_s T_{ms} A_i T_p}{1 + T_i + T_v}. \tag{13.213}$$

Thus, only M_{vcl} is affected by the feedforward gains for the boost and buck-boost converters.

13.12 Slope Compensation by Adding a Ramp to Inductor Current

Slope compensation can also be accomplished by adding an external periodic ramp current waveform to the inductor current waveform, as shown in Figure 13.53. It can be seen that both slopes of the waveform $i_L + i_A$ are changed. Figure 13.53 shows steady-state and perturbed waveforms of $i_L + i_A$ in PWM converters with slope compensation obtained by adding a ramp to the inductor current. The slopes of the waveform $i_L + i_A$ are

$$M_1 + M_3 = \tan\alpha = \frac{\Delta(i_{L0} + i_A)}{dT_s} \tag{13.214}$$

and

$$M_2 - M_3 = \tan\beta = \frac{\Delta(i_{L1} + i_A)}{dT_s}, \tag{13.215}$$

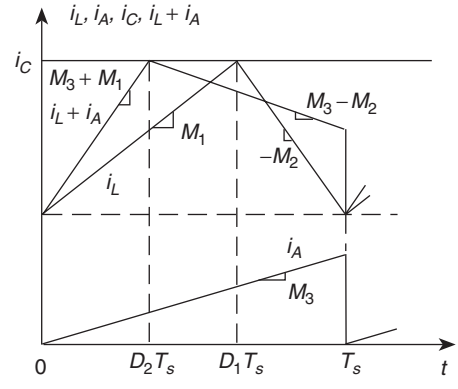


Figure 13.53 Slope compensation by adding an external periodic ramp current i_A to the inductor current waveform i_L.

resulting in the current gain

$$a \equiv \frac{\Delta(i_{L1} + i_A)}{\Delta(i_{L0} + i_A)} = \frac{M_2 - M_3}{M_1 + M_3}. \tag{13.216}$$

This equation is the same as (13.33).

13.13 Relationships for Constant-frequency Current-mode On-time Control

A similar analysis reveals that, in the constant-frequency current-mode scheme, where the clock initiates the switch on-time, and the control and inductor current intersection initiates the switch off-time, the relation

$$a = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_1}{M_2} = \frac{1 - D}{D} \tag{13.217}$$

holds for a circuit without slope compensation. In this case, the inner current loop is stable for $D > 0.5$ and is unstable for $D < 0.5$. If slope compensation is used,

$$a = \frac{|\Delta i_{L1}|}{|\Delta i_{L0}|} = \frac{M_1 - M_3}{M_1 + M_3} \tag{13.218}$$

and

$$T_m = \frac{1}{(M_2 + M_3)T_s}. \tag{13.219}$$

13.14 Summary

- PWM converters with current-mode control are nonlinear, time-varying circuits.
- Modeling current-mode-controlled converters involves discrete-time signals.
- The current-mode-control scheme contains two loops: a current inner loop and a voltage outer loop.
- In the current-mode-control architecture, the peak inductor current is controlled along with the output voltage.
- In current-mode control, the peak inductor current and the peak switch current are equal to the instantaneous control current i_C.
- PWM converters with current-mode control inherently have short-circuit protection and over-current protection. Since the peak and average current of the inductor is proportional to the control voltage, the output current can be limited by clamping the control voltage.
- Since the inductor current is controlled by sensing the peak current in the power switch or the inductor, the current can be limited on a cycle-by-cycle basis, resulting in a fast response of the current loop.
- The inner current loop is unstable for $D > 0.5$ for CCM. This instability of the current loop does not occur for DCM.
- Slope compensation may be used to achieve stability of the inner current loop. One method of slope compensation is to subtract a ramp voltage from the control voltage. Another method is to add a ramp to the sensed inductor or switch current.

- As the compensating ramp slope M_3 increases, the range of the duty cycle, in which the inner loop is stable, is increased above 0.5.
- The inner current loop is stable at any duty cycle D for $M_3 > 0.5M_2$.
- The inner current loop recovers from a perturbation within one cycle if $M_3 = M_2$ (i.e., for dead-beat control).
- Current-mode control offers several advantages, such as ease of compensation of the voltage loop, fast dynamic response, inherent line feedforward, low audio susceptibility, good line regulation, automatic overload and short-circuit protection, and easy paralleling of multiple converters.
- As a increases from 0 to 1, f_{ci}/f_s increases from 0.3 to 0.5.
- The current loop is wide band with the crossover frequency $f_{ci} \approx 0.4\, f_s$ at $PM \approx 60^\circ$.
- The current loop acts like a partial lead compensator for the voltage loop.
- Due to sensing the instantaneous inductor current or switch current, the peak-current-mode control scheme is susceptible to noise, especially when the inductor current ripple is low or when the duty cycle is low.
- Voltage-mode control is more immune to noise than current-mode control.
- The constant-off-time current-mode control has many advantages.
- Current-mode control can be used in constant-current dc–dc converters.

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13.16 Review Questions

13.1. What is the basic topology of a current-mode-control system?

13.2. Explain the principle of operation of current-mode control.

13.3. What event turns the transistor on in PWM converters with current-mode control?

13.4. What event turns the transistor off in PWM converters with current-mode control?

13.5. How many loops are there in the current-mode control scheme?

13.6. What are the advantages of current-mode control?

13.7. When is the current loop without slope compensation stable?

13.8. Explain the principle of slope compensation.

13.9. When is the current loop with slope compensation stable?

13.10. What amount of slope compensation will guarantee stability of the current loop under any conditions?

13.11. What amount of slope compensation will guarantee optimum compensation of the current loop?

13.12. What is the oscillation frequency of the unstable current loop?

13.13. Is peak-current-mode control susceptible to noise?

13.17 Problems

13.1. A lossless buck converter with constant-frequency peak-current-mode control and without slope compensation has $V_O = 5\,\text{V}$. What is the range of the input voltage V_I in which the inner loop is stable?

13.2. A lossy buck converter with constant-frequency peak-current-mode control and without slope compensation has $V_O = 5\,\text{V}$ and efficiency $\eta = 0.9$. What is the range of the input voltage V_I in which the converter is stable?

13.3. A lossy buck converter with constant-frequency peak-current-mode control and with slope compensation has $V_I = 28\,\text{V}$, $V_O = 5\,\text{V}$, $L = 301\,\mu\text{H}$, the switching frequency $f_s = 100\,\text{kHz}$, and efficiency $\eta = 0.9$. Is the converter stable? Does the converter

require slope compensation? What is the slope of the rising inductor current waveform?

13.4. A buck converter with constant-frequency peak-current-mode control has $V_I = 28 \pm 4\,\text{V}$, $V_O = 2\,\text{V}$, $L = 301\,\mu\text{H}$, $f_s = 100\,\text{kHz}$, and efficiency $\eta = 1$. Is slope compensation required in this converter?

13.5. A buck converter with constant-frequency peak-current-mode control has $V_{Inom} = 28\,\text{V}$, $V_O = 20\,\text{V}$, $L = 301\,\mu\text{H}$, $f_s = 100\,\text{kHz}$, and efficiency $\eta = 1$. Find the ramp slope for the optimum compensation and the peak compensating voltage.

13.6. A buck-boost converter with constant-frequency peak-current-mode control has $V_{Inom} = 42\,\text{V}$, $V_O = -28\,\text{V}$, $L = 334\,\mu\text{H}$, $f_s = 100\,\text{kHz}$, and efficiency $\eta = 0.85$. Find M_{3nom} and the peak value of the compensation ramp slope at which $a = 0.3$.

13.7. A PWM converter with constant-frequency peak-current-mode control has $R_s = 0.1\,\Omega$, $a = 0.3$, and $f_s = 100\,\text{kHz}$. Find $H_{icl}(z)$, $H_{icl}(s)$, and $T_i(s)$.

13.8. A buck-boost converter has $D = 0.407$, $V_O = -28\,\text{V}$, $M_1 = 0.144\,\text{A/s}$, $M_3 = 0.0983\,\text{A/s}$, and $\Delta V_I = 1\,\text{V}$. Find K_i and ΔD. Assuming that the voltage loop is open and the feedforward voltage is the only change in the circuit, calculate the output voltage V_O.

13.18 Appendix: Sample-and-hold Modeling

13.18.1 Sampler

An ideal sampler can be modeled as follows. The control voltage of the inner loop $v_c(t)$ is an analog, continuous-time function. The train of unit impulses $\delta(t - kT_s)$ with the period $T_s = 1/f_s$ is given by

$$\delta_T(t) = \sum_{k=-\infty}^{\infty} \delta(t - kT_s) = \cdots + \delta(t + T_s) + \delta(t) + \delta(t - T_s) + \cdots. \tag{13.220}$$

The sampler can be modeled by a multiplier of the analog, continuous-time control voltage $v_c(t)$ and the train of unit impulses $\delta_T(t)$, as shown in Figure 13.54. The sampled control

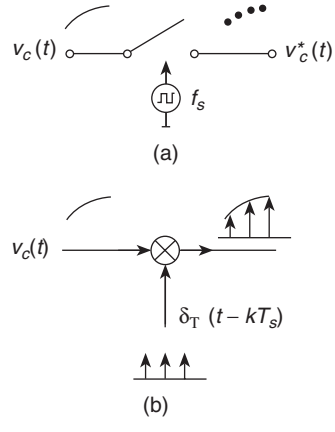


Figure 13.54 Sampler. (a) Circuit. (b) Model.

voltage at the sampler output can be represented by a sequence (i.e., a train) of amplitude-modulated impulses

$$v_c^*(t) = \sum_{k=0}^{\infty} v_c(kT_s)\delta(t - kT_s)$$
$$= v_c(0)\delta(t) + v_c(T_s)\delta(t - T_s) + v_c(2T_s)\delta(t - 2T_s) + \cdots. \quad (13.221)$$

Expression (13.221) can be simplified to the following discrete function of time

$$v_c^*(t) = \sum_{k=0}^{\infty} v_c(t)\delta(t - kT_s) = v_c(t)\sum_{k=0}^{\infty}\delta(t - kT_s) = v_c(t)\delta_T(t) \quad (13.222)$$

because $\delta(t - kT_s) = 0$ for $t \neq kT_s$ and $\delta(t - kT_s) = 1$ for $t = kT_s$. The impulse-sampled control voltage is represented by the product of the continuous-time control voltage $v_c(t)$ and the train of unit impulses $\delta_T(t - kT_s)$. The strength of each impulse is equal to the value of the control voltage at the sampling instant. Therefore, an ideal sampler can be regarded as an amplitude-modulated δ-modulator, in which the control voltage $v_c(t)$ is the modulating signal, the train of unit impulses $\delta_T(t)$ with frequency $f_s = 1/T_s$ is the carrier, and the sampler output is the train of the amplitude-modulated impulses. Since the train of unit impulses is a periodic function with angular frequency $\omega_s = 2\pi/T_s$, it can be represented by a exponential Fourier series

$$\delta_T(t) = \sum_{k=-\infty}^{\infty} C_k e^{jk\omega_s t}, \quad (13.223)$$

where the exponential Fourier series coefficients are

$$C_k = \frac{1}{T_s}\int_0^{T_s} \delta_T(t)e^{-jk\omega_s t}dt = \frac{1}{T_s}. \quad (13.224)$$

Hence,

$$\delta_T(t) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} e^{jk\omega_s t} = \cdots + \frac{1}{T_s}e^{-j\omega_s t} + \frac{1}{T_s} + \frac{1}{T_s}e^{j\omega_s t} + \frac{1}{T_s}e^{j2\omega_s t} + \cdots. \quad (13.225)$$

Thus, the sampled control voltage at the sampler output can be described by

$$v_c^*(t) = v_c(t)\delta_T(t) = v_c(t)\sum_{k=-\infty}^{\infty} C_k e^{jk\omega_s t} = \frac{v_c(t)}{T_s}\sum_{k=-\infty}^{\infty} e^{jk\omega_s t}. \quad (13.226)$$

Taking the Fourier transform of $v_c^*(t)$ and using the shifting theorem of the Fourier transform,

$$\mathcal{F}\{f(t)e^{j\omega_o t}\} = F(\omega - \omega_o), \quad (13.227)$$

we obtain the frequency spectrum of the sampled control voltage

$$v_c^*(j\omega) = \mathcal{F}\{v_c^*(t)\} = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} v_c(j\omega + jk\omega_s)$$
$$= \cdots + \frac{1}{T_s}v_c[j(\omega - \omega_s)] + \frac{1}{T_s}v_c(j\omega) + \frac{1}{T_s}v_c[j(\omega + \omega_s)] + \cdots. \quad (13.228)$$

The frequency spectrum of the impulse-sampled control voltage is amplified by a factor of $f_s = 1/T_s$ and reproduced an infinite number of times at dc, f_s, $2f_s$, $3f_s$, etc. The spectrum

of the sampled error voltage contains the components at $nf_s \pm f$, where $n = 1, 2, 3, \ldots$. The sampling process produces the replicas of the input-frequency spectrum centered at dc and the multiples of the switching frequency. The Laplace transform of (13.228) is

$$v_c^*(s) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} v_c(s + jk\omega_s). \tag{13.229}$$

If we assume that the spectrum of the control voltage v_c^* does not contain significant components above $f_s/2$ (i.e., $|v_{ei}(f)| \approx 0$ for $f > f_s/2$) and therefore there is no aliasing, then we can write

$$v_c^*(s) \approx \frac{1}{T_s} v_c(s). \tag{13.230}$$

Hence, the transfer function of an ideal sampler is

$$H_s(s) \equiv \frac{v_c^*(s)}{v_c(s)} \approx \frac{1}{T_s} = f_s. \tag{13.231}$$

For example, assume that the control voltage is a sine wave

$$v_c(t) = V_m \sin(2\pi ft). \tag{13.232}$$

The sampled control voltage is

$$v_c^*(t) = \sum_{k=-\infty}^{\infty} V_m \sin(2\pi fkT_s)\delta(t - kT_s). \tag{13.233}$$

The spectrum of the sampled control voltage is

$$v_c^*(f) = f_s V_m \sum_{k=-\infty}^{\infty} [\delta(kT_s - f) + \delta(kT_s + f)]. \tag{13.234}$$

Figure 13.55 shows the spectrum of a sine wave before and after sampling.

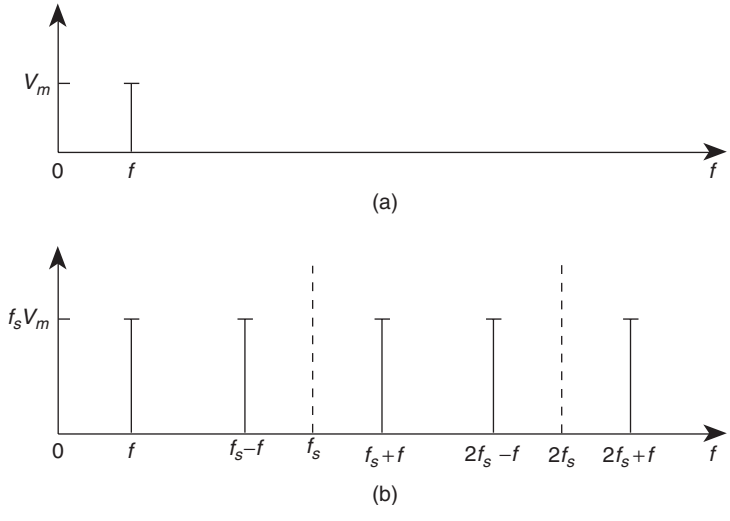


Figure 13.55 Spectrum of a sine wave. (a) Before sampling. (b) After sampling.

Zero-order-hold

The transfer function of the zero-order hold can be derived as follows. Assume that the control voltage $v_c(t) = 0$ for $t < 0$. The duty cycle at the output of the zero-order hold $i_l^0(t)$ is the step reconstruction and is related to the sample sequence $v_c(kT_s)$ by

$$\begin{aligned} v_c^0(t) &= v_c(0)[u(t) - u(t - T_s)] + v_c(T_s)[u(t - T_s) - u(t - 2T_s)] \\ &\quad + v_c(2T_s)[u(t - 2T_s) - u(t - 3T_s)] + \cdots \\ &= \sum_{k=0}^{\infty} v_c(kT_s)\{u(t - kT_s) - u[t - (k + 1)T_s]\}. \end{aligned} \tag{13.235}$$

The difference between the perturbed inductor current and the steady-state inductor current is a continuous-time function with a 'staircase' waveform. The Laplace transform of $v_c^0(t)$ is

$$\begin{aligned} v_c^0(s) = \mathcal{L}\{v_c^0(t)\} &= v_c(0)\left(\frac{1}{s} - \frac{e^{-sT_s}}{s}\right) + v_c(T_s)\left(\frac{e^{-sT_s}}{s} - \frac{e^{-s2T_s}}{s}\right) \\ &\quad + v_c(2T_s)\left(\frac{e^{-s2T_s}}{s} - \frac{e^{-s3T_s}}{s}\right) + \cdots \\ &= \frac{1 - e^{-sT_s}}{s}[v_c(0) + v_c(T_s)e^{-sT_s} + v_c(2T_s)e^{-2sT_s} + \cdots] \\ &= \left(\frac{1 - e^{-sT_s}}{s}\right)\sum_{k=0}^{\infty} v_c(kT_s)e^{-ksT_s} = \left(\frac{1 - e^{-sT_s}}{s}\right)v_c^*(s). \end{aligned} \tag{13.236}$$

Thus, the transfer function of the zero-order hold is given by

$$H_h(s) \equiv \frac{v_c^0(s)}{v_c^*(s)} = \frac{1 - e^{-sT_s}}{s}. \tag{13.237}$$

The transfer function of an ideal sampler and a zero-order hold is

$$H_{sh}(s) \equiv \frac{v_c^0(s)}{v_c(s)} = \frac{v_c^0(s)}{v_c^*(s)}\frac{v_c^*(s)}{v_c(s)} = H_s(s)H_h(s) = \frac{1 - e^{-sT_s}}{sT_s}. \tag{13.238}$$

The frequency response of the sampler and zero-order hold can be found as follows. Setting $s = j\omega$,

$$\begin{aligned} H_{sh}(j\omega) &= \frac{1 - e^{-j\omega T_s}}{j\omega T_s}\, e^{\frac{j\omega T_s}{2}} e^{-\frac{j\omega T_s}{2}} = \frac{e^{j\frac{\omega T_s}{2}} - e^{-j\frac{\omega T_s}{2}}}{2\,j\,\dfrac{\omega T_s}{2}} e^{-j\frac{\omega T_s}{2}} \\ &= \frac{\sin\dfrac{\omega T_s}{2}}{\dfrac{\omega T_s}{2}} e^{-j\frac{\omega T_s}{2}} = \frac{\sin\dfrac{\pi f}{f_s}}{\dfrac{\pi f}{f_s}} e^{-j\frac{\pi f}{f_s}} = |H_{sh}|e^{j\phi_{Hsh}}, \end{aligned} \tag{13.239}$$

where

$$|H_{sh}| = \left|\frac{\sin\dfrac{\pi f}{f_s}}{\dfrac{\pi f}{f_s}}\right| \tag{13.240}$$

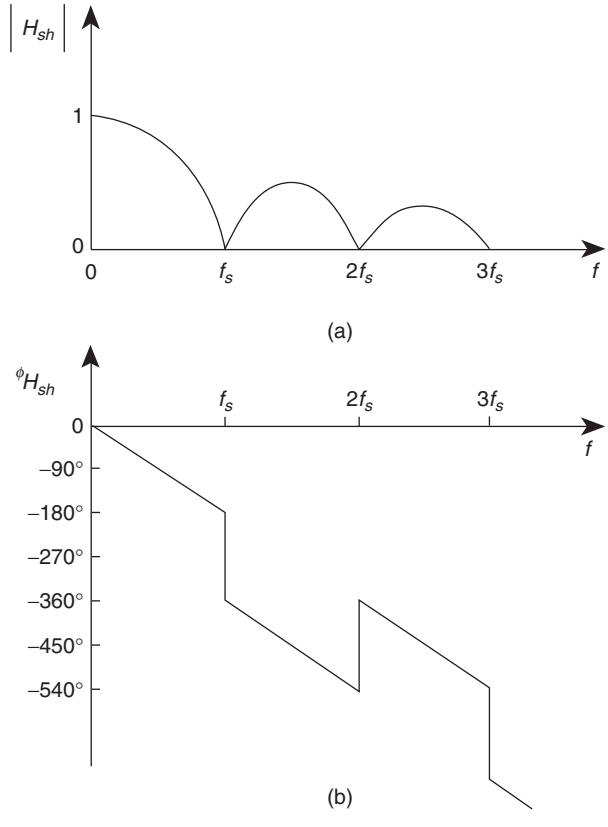


Figure 13.56 Bode plots of H_{sh}. (a) Magnitude $|H_{sh}|$. (b) Phase $\phi_{H_{sh}}$.

and

$$\phi_{H_{sh}} = -\frac{\pi f}{f_s} + \theta, \tag{13.241}$$

with

$$\theta = \begin{cases} 0, & \text{for } \sin\dfrac{\pi f}{f_s} \geq 0 \\ -\pi, & \text{for } \sin\dfrac{\pi f}{f_s} < 0. \end{cases} \tag{13.242}$$

Hence,

$$\left|H_{sh}\left(\frac{f_s}{2}\right)\right| = \frac{2}{\pi} \approx 0.6366 \tag{13.243}$$

and

$$\phi_{Hsh}\left(\frac{f_s}{2}\right) = -90^\circ. \tag{13.244}$$

Figure 13.56 shows Bode plots of $H_{sh}(s)$.

14

Current-mode Control of Boost Converter

14.1 Introduction

This chapter presents the open-loop small-signal duty cycle-to-inductor current transfer function, the input voltage-to-inductor current transfer function, and the inductor-to-output current transfer function for the boost converter operated in CCM. Also, responses of the inductor current to step changes of the duty cycle, the input voltage, and the load current are given for the open-loop boost converter. Finally, inner current closed-loop and outer voltage closed-loop Bode plots and step responses are presented. Current-mode control of the PWM boost converter has been studied in [1]–[2].

14.2 Open-loop Small-signal Transfer Functions

14.2.1 Open-loop Duty Cycle-to-inductor Current Transfer Function

A small-signal model of the PWM boost converter for CCM operation is shown in Figure 14.1(a). This model is obtained by replacing the switching network in the boost converter with a small-signal model. Figure 14.1(b) shows a block diagram of the open-loop boost converter. Setting $v_i = 0$ and $i_o = 0$ in Figure 14.1(a), one obtains a small-signal model of the boost converter for deriving the duty cycle-to-inductor current transfer function shown in Figure 14.2. By Kirchhoff's current law,

$$i_l = Di_l + I_L d + i_{Z_2} = Di_l + I_L d + \frac{v_o}{Z_2} \tag{14.1}$$

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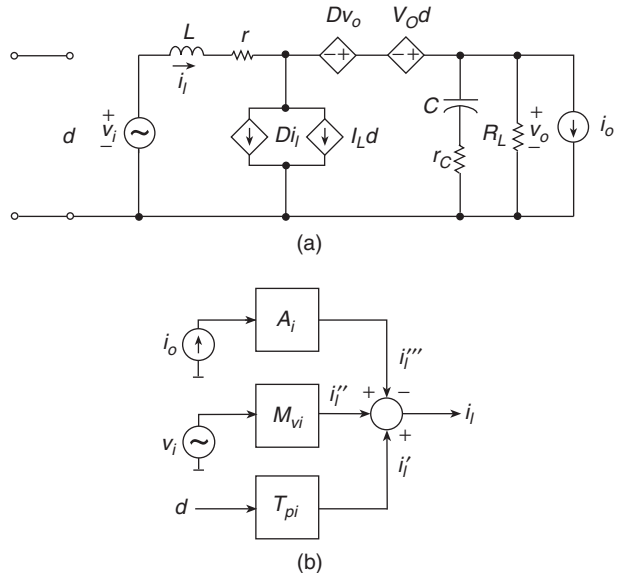


Figure 14.1 Small-signal model and block diagram of the PWM boost converter for CCM. (a) Small-signal model. (b) Block diagram.

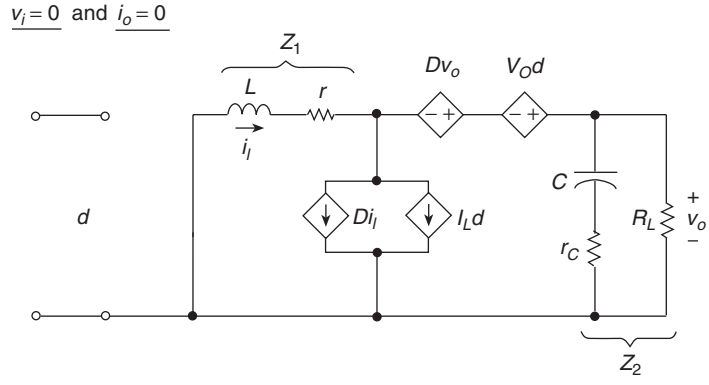


Figure 14.2 Small-signal model of the PWM boost converter used to derive the duty cycle-to-inductor current transfer function T_{pi}.

which, using relationship $I_L = I_O/(1-D) = V_O/(1-D)R_L$, becomes

$$v_o = (1-D)i_l Z_2 - I_L d Z_2 = (1-D)i_l Z_2 - \frac{V_O d Z_2}{(1-D)R_L}. \tag{14.2}$$

Using Kirchhoff's voltage law,

$$-i_l Z_1 + D v_o + V_O d - v_o = 0, \tag{14.3}$$

which gives

$$v_o = \frac{V_O d}{1-D} - \frac{i_l Z_1}{1-D}. \tag{14.4}$$

Equating the right-hand sides of (14.2) and (14.4),

$$i_l[Z_1 + (1-D)^2 Z_2] = d[V_O + (1-D)I_L Z_2] = dV_O\left(1 + \frac{Z_2}{R_L}\right). \tag{14.5}$$

Hence, one obtains the duty cycle-to-inductor current transfer function

$$T_{pi}(s) \equiv \left.\frac{i_l(s)}{d(s)}\right|_{v_i = i_o = 0} = V_O \frac{1 + \dfrac{Z_2}{R_L}}{Z_1 + (1-D)^2 Z_2}. \tag{14.6}$$

The impedances Z_1 and Z_2 are given by

$$Z_1 = r + sL \tag{14.7}$$

and

$$Z_2 = \frac{R_L\left(r_C + \dfrac{1}{sC}\right)}{R_L + r_C + \dfrac{1}{sC}} = \frac{R_L(1 + sCr_C)}{1 + sC(R_L + r_C)}. \tag{14.8}$$

Substituting (14.7) and (14.8) into (14.6), one arrives at the *duty cycle-to-inductor current transfer function* in the s-domain,

$$\begin{aligned}
T_{pi}(s) &\equiv \left.\frac{i_l(s)}{d(s)}\right|_{v_i = i_o = 0} \\
&= \frac{V_O(R_L + 2r_C)}{L(R_L + r_C)} \frac{s + \dfrac{1}{C(R_L/2 + r_C)}}{s^2 + s\dfrac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{(1-D)^2 R_L + r}{LC(R_L + r_C)}} \\
&= \frac{V_O(R_L + 2r_C)}{L(R_L + r_C)} \frac{(s - z_{i1})}{(s - p_1)(s - p_2)} = T_{pix} \frac{s + \omega_{zi1}}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\
&= \frac{V_O(R_L + 2r_C)\omega_{zi1}}{L(R_L + r_C)\omega_0^2} \frac{1 + \dfrac{s}{\omega_{zi1}}}{1 + \dfrac{2\xi}{\omega_0}s + \left(\dfrac{s}{\omega_0}\right)^2} = T_{pio} \frac{1 + \dfrac{s}{\omega_{zi1}}}{1 + \dfrac{s}{Q\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2},
\end{aligned} \tag{14.9}$$

where the magnitude of T_{pi} at $f = 0$ is

$$T_{pio} = T_{pi}(0) = \frac{2V_O}{(1-D)^2 R_L + r}, \tag{14.10}$$

$$T_{pix} = \frac{V_O(R_L + 2r_C)}{L(R_L + r_C)} \approx \frac{V_O}{L}, \tag{14.11}$$

the angular *corner frequency* or the angular *undamped natural frequency* is

$$\omega_0 = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_C)}}, \tag{14.12}$$

the *damping ratio* is

$$\xi = \frac{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}{2\sqrt{LC(R_L + r_C)[r + (1-D)^2 R_L]}}, \tag{14.13}$$

the *quality factor* is

$$Q = \frac{1}{2\xi} = \frac{\sqrt{LC(R_L + r_C)[r + (1-D)^2 R_L]}}{C[r(R_L + r_C) + (1-D)^2 R_L r_C] + L}, \tag{14.14}$$

the zero is

$$z_{i1} = -\omega_{zi1} = -\frac{1}{C(R_L/2 + r_C)}, \tag{14.15}$$

and the poles are

$$p_1, p_2 = -\xi\omega_0 \pm \omega_0\sqrt{\xi^2 - 1} = -\xi\omega_0 \pm j\omega_0\sqrt{1 - \xi^2} = -\sigma \pm j\omega_d. \tag{14.16}$$

The duty cycle-to-inductor current transfer function T_{pi} is a second-order low-pass function, which has two LHP poles and one LHP zero. The LHP zero z_{i1} is independent of D and the poles depend on D. When D is increased from 0 to 1, the corner frequency f_0 decreases and the damping factor ξ increases.

Example 14.1

The boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, and $r = 0.316\,\Omega$. Calculate r, z_{i1}, f_{zi1}, f_0, ξ, Q, p_1, p_2, and f_d at $R_{Lmin} = 40\,\Omega$.

Solution. The total parasitic resistance in series with the inductor at $D_{nom} = 0.5$ is

$$\begin{aligned} r &= D_{nom} r_{DS} + (1 - D_{nom}) R_F + r_L \\ &= 0.5 \times 0.18 + (1 - 0.5) \times 0.072 + 0.19 = 0.09 + 0.036 + 0.19 = 0.316\,\Omega. \end{aligned} \tag{14.17}$$

The duty ratio-to-inductor current transfer function at $f = 0$ is

$$\begin{aligned} T_{pio} = T_{pi}(0) &= \frac{2V_O}{(1 - D_{nom})^2 R_{Lmin} + r} = \frac{2 \times 20}{(1 - 0.5)^2 \times 40 + 0.316} \\ &= 3.8775\,\text{A} \;= 11.771\,\text{dBA} \end{aligned} \tag{14.18}$$

and

$$\begin{aligned} T_{pix} &= \frac{V_O(R_{Lmin} + 2r_C)}{L(R_{Lmin} + r_C)} = \frac{20 \times (40 + 2 \times 0.111)}{156 \times 10^{-6} \times (40 + 0.111)} \\ &= 128{,}559.9\,\text{A/s} \;= 102.182\,\text{dBA/s}. \end{aligned} \tag{14.19}$$

The LHP zero is

$$z_{i1} = -\frac{1}{C(R_{Lmin}/2 + r_C)} = -\frac{1}{68 \times 10^{-6} \times (40/2 + 0.111)} = -731.236\,\text{rad/s}, \tag{14.20}$$

and the frequency of the LHP zero is

$$f_{zi1} = \frac{1}{2\pi C(R_{Lmin}/2 + r_C)} = \frac{1}{2 \times \pi \times 68 \times 10^{-6} \times (40/2 + 0.111)} = 116.38\,\text{Hz}. \tag{14.21}$$

The corner frequency is

$$\begin{aligned} f_0 = \frac{1}{2\pi}\sqrt{\frac{(1 - D_{nom})^2 R_{Lmin} + r}{LC(R_{Lmin} + r_C)}} &= \frac{1}{2\pi}\sqrt{\frac{(1 - 0.5)^2 \times 40 + 0.316}{156 \times 10^{-6} \times 68 \times 10^{-6} \times (40 + 0.111)}} \\ &= 783.66\,\text{Hz}. \end{aligned} \tag{14.22}$$

The damping ratio is

$$\xi = \frac{C[r(R_{Lmin}+r_C)+(1-D_{nom})^2 R_{Lmin}r_C]+L}{2\sqrt{LC(R_{Lmin}+r_C)[r+(1-D_{nom})^2 R_{Lmin}]}}$$
$$= \frac{68\times10^{-6}[0.316\times(40+0.111)+(1-0.5)^2\times40\times0.111]+156\times10^{-6}}{2\sqrt{156\times10^{-6}\times68\times10^{-6}\times(40+0.111)[0.316+(1-0.5)^2\times40]}}$$
$$= \frac{1093.43\times10^{-6}}{4190.194\times10^{-6}} = 0.261, \tag{14.23}$$

and the quality factor is

$$Q = \frac{1}{2\xi} = \frac{1}{2\times0.261} = 1.916. \tag{14.24}$$

The poles are

$$p_1, p_2 = -\sigma \pm j\omega_d = -\xi\omega_0 \pm j\omega_0\sqrt{1-\xi^2}$$
$$= -0.261\times2\times\pi\times783.66 \pm j2\times\pi\times783.66\sqrt{1-0.261^2}$$
$$= -1285 \pm j4753\,(\text{rad/s}), \tag{14.25}$$

and the damped frequency is

$$f_d = f_0\sqrt{1-\xi^2} = 783.66\sqrt{1-0.261^2} = 756.5\,\text{Hz}. \tag{14.26}$$

Substituting $s = j\omega$ into (14.9),

$$T_{pi}(j\omega) = T_{pio}\frac{\left(1+j\dfrac{\omega}{\omega_{zi1}}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2+j2\xi\left(\dfrac{\omega}{\omega_0}\right)} = |T_{pi}|e^{j\phi_{Tpi}}, \tag{14.27}$$

where

$$|T_{pi}| = T_{pio}\sqrt{\frac{\left[1+\left(\dfrac{\omega}{\omega_{zi1}}\right)^2\right]}{\left[1-\left(\dfrac{\omega}{\omega_0}\right)^2\right]^2+4\xi^2\left(\dfrac{\omega}{\omega_0}\right)^2}} \tag{14.28}$$

and

$$\phi_{Tpi} = \arctan\left(\frac{\omega}{\omega_{zi1}}\right) - \arctan\left[\frac{2\xi\left(\dfrac{\omega}{\omega_0}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} \le 1, \tag{14.29}$$

or

$$\phi_{Tpi} = -180^\circ + \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left[\frac{2\xi\left(\dfrac{\omega}{\omega_0}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} > 1. \tag{14.30}$$

Figure 14.3 shows idealized Bode plots of the open-loop duty cycle-to-inductor current transfer function T_{pi} for the boost converter.

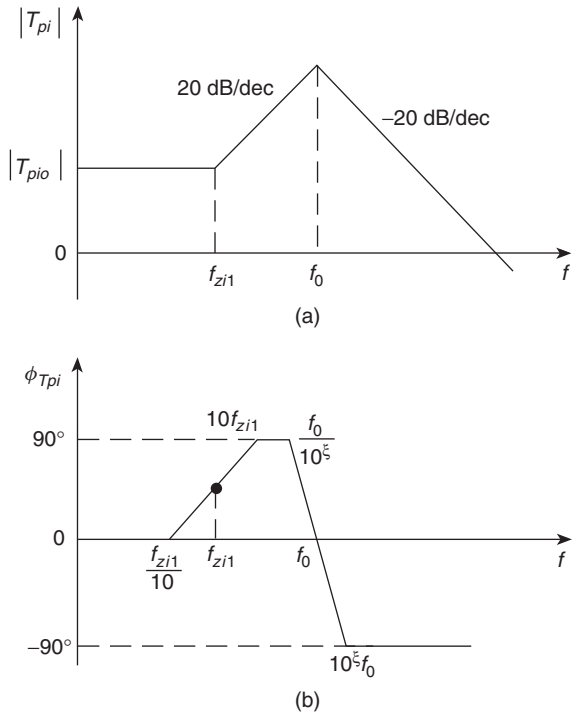


Figure 14.3 Idealized Bode plots of the open-loop duty cycle-to-inductor current transfer function T_{pi} for the boost converter (without the delay). (a) $|T_{pi}|$ versus f. (b) ϕ_{Tpi} versus f.

Example 14.2

For the boost converter with $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. Draw Bode plots of T_{pi} at $D = 0.5$.

Solution. Figures 14.4 and 14.5 show the Bode plots of T_{pi}.

The delay t_d introduced by the power transistor, its driver, and the set–reset flip-flop can be described by $T_d = e^{-st_d}$, which is not a rational function. This function can be described by a first-order Padé approximation valid for frequencies from dc to $f_s/2$,

$$T_d = e^{-st_d} \approx \frac{1 - \dfrac{st_d}{2}}{1 + \dfrac{st_d}{2}} = -\frac{s - \dfrac{2}{t_d}}{s + \dfrac{2}{t_d}} = -\frac{s - \omega_{zd}}{s + \omega_{pd}}, \tag{14.31}$$

where $\omega_{zd} = \omega_{pd} = 2/t_d$. The duty cycle-to-inductor current transfer function with the delay is given by

$$T_{pi}(s) = -T_{pix}\frac{s + \omega_{zi1}}{s^2 + 2\xi\omega_0 s + \omega_0^2}\frac{s - \omega_{zd}}{s + \omega_{pd}}. \tag{14.32}$$

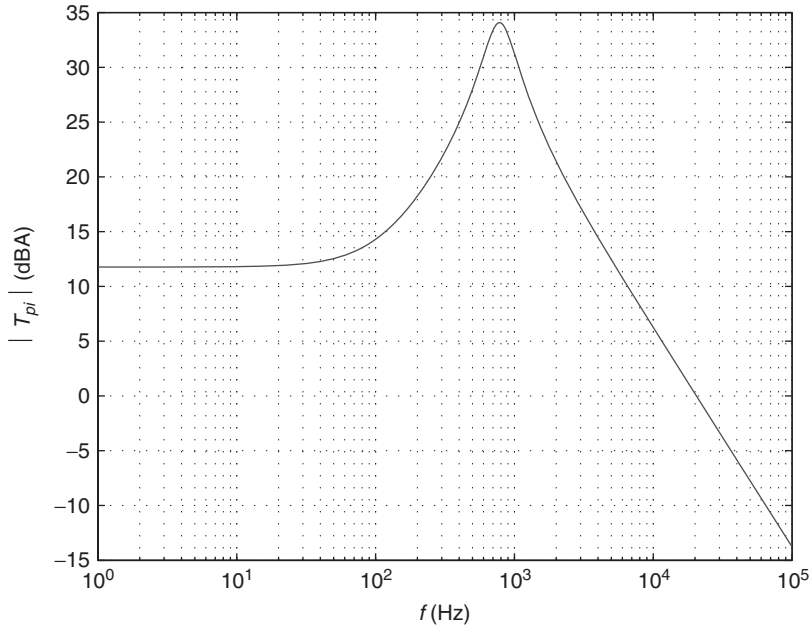


Figure 14.4 Bode plot of the magnitude of the open-loop duty cycle-to-inductor current transfer function.

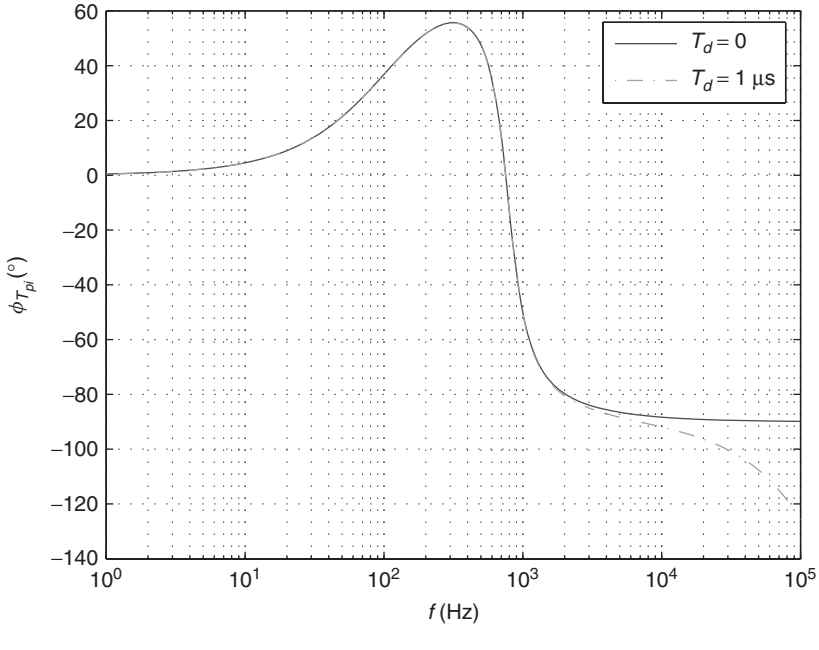


Figure 14.5 Bode plot of the phase of the open-loop duty cycle-to-inductor current transfer function for the boost converter without and with the delay $t_d = 1\,\mu s$.

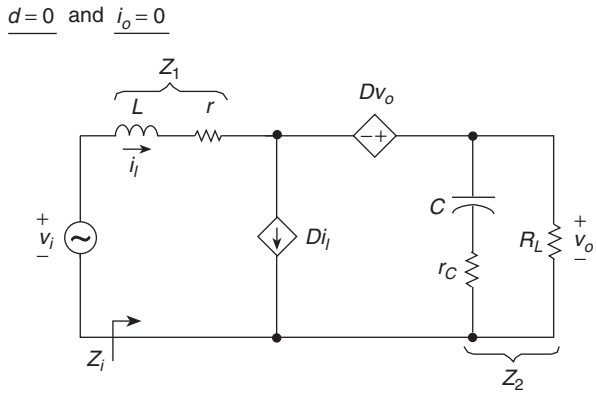


Figure 14.6 Small-signal model of the PWM boost converter for deriving the input voltage-to-inductor current transfer function M_{vi}.

14.2.2 Open-loop Input Voltage-to-inductor Current Transfer Function

Setting $d = 0$ and $i_o = 0$ in the small-signal model of the boost converter of Figure 14.1 gives a small-signal model, shown in Figure 14.6, that can be used for deriving the input voltage-to-inductor current transfer function M_{vi}. By Kirchhoff's current law,

$$i_l = Di_l + i_{Z_2} = Di_l + \frac{v_o}{Z_2}, \tag{14.33}$$

which can be rearranged as

$$v_o = (1 - D)i_l Z_2. \tag{14.34}$$

By Kirchhoff's voltage law,

$$v_i - i_l Z_1 + Dv_o - v_o = 0, \tag{14.35}$$

which gives

$$v_o = \frac{v_i}{1 - D} - \frac{i_l Z_1}{1 - D}. \tag{14.36}$$

Equating the right-hand sides of (14.34) and (14.36),

$$v_i = i_l[Z_1 + (1 - D)^2 Z_2]. \tag{14.37}$$

Hence, the open-loop input voltage-to-inductor current transfer function is obtained as

$$M_{vi}(s) \equiv \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{1}{Z_1 + (1 - D)^2 Z_2}. \tag{14.38}$$

Substituting (14.7) and (14.8) into (14.38), one obtains the *input voltage-to-inductor current transfer function*

$$M_{vi}(s) \equiv \left.\frac{i_l(s)}{v_i(s)}\right|_{d=i_o=0} = \frac{1}{L} \frac{s + \dfrac{1}{C(R_L + r_C)}}{s^2 + s\dfrac{C[r(R_L + r_C) + (1 - D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{(1 - D)^2 R_L + r}{LC(R_L + r_C)}}$$

$$= \frac{1}{L}\frac{s+\omega_{zi2}}{s^2+2\xi\omega_0 s+\omega_0^2} = \frac{1}{(1-D)^2R_L+r}\frac{1+\dfrac{s}{\omega_{zi2}}}{1+\dfrac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2}$$

$$= M_{vio}\frac{1+\dfrac{s}{\omega_{zi2}}}{1+\dfrac{2\xi s}{\omega_0}+\left(\dfrac{s}{\omega_0}\right)^2}, \tag{14.39}$$

where

$$\omega_{zi2} = \frac{1}{C(R_L+r_C)}. \tag{14.40}$$

For $s = 0$,

$$M_{vio} = M_{vi}(0) = \frac{1}{(1-D)^2R_L+r}. \tag{14.41}$$

For $s = j\omega$,

$$M_{vi}(j\omega) = M_{vio}\frac{\left(1+j\dfrac{\omega}{\omega_{zi2}}\right)}{1-\left(\dfrac{\omega}{\omega_0}\right)^2+j2\xi\left(\dfrac{\omega}{\omega_0}\right)} = |M_{vi}|e^{j\phi_{Mvi}}, \tag{14.42}$$

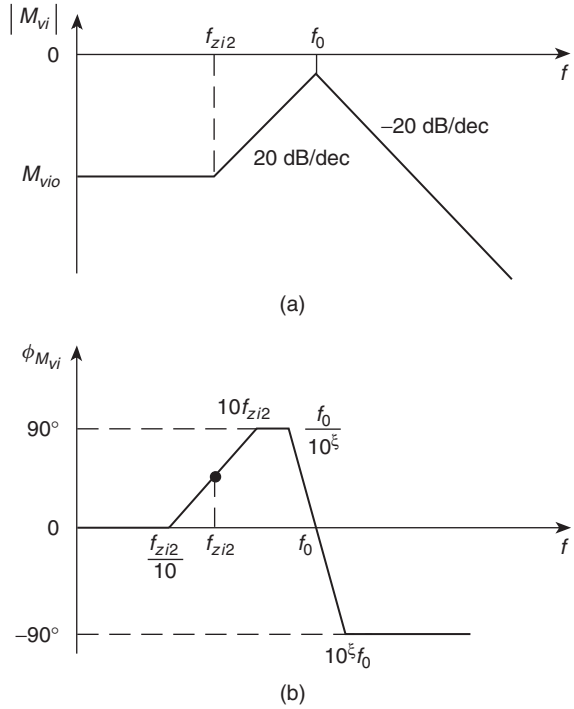


Figure 14.7 Idealized Bode plots of the open-loop input voltage-to-inductor current transfer function M_{vi} for the boost converter. (a) $|M_{vi}|$ versus f. (b) ϕ_{Mvi} versus f.

where

$$|M_{vi}| = M_{vio}\sqrt{\frac{\left[1+\left(\frac{\omega}{\omega_{zi2}}\right)^2\right]}{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2+4\xi^2\left(\frac{\omega}{\omega_0}\right)^2}} \tag{14.43}$$

and

$$\phi_{Mvi} = \arctan\left(\frac{\omega}{\omega_{zi2}}\right) - \arctan\left[\frac{2\xi\left(\frac{\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} \leq 1, \tag{14.44}$$

or

$$\phi_{Mvi} = -180^\circ + \arctan\left(\frac{\omega}{\omega_{zn}}\right) - \arctan\left[\frac{2\xi\left(\frac{\omega}{\omega_0}\right)}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right], \quad \text{for } \frac{\omega}{\omega_0} > 1. \tag{14.45}$$

Figure 14.7 shows idealized Bode plots of the open-loop input voltage-to-inductor current transfer function M_{vi} for the boost converter. Note that $M_{vi} = 1/Z_i$ for the boost converter.

Example 14.3

The boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. Calculate f_{zi2} and M_{vio} at $R_{Lmin} = 40\,\Omega$ and draw Bode plots of M_{vi} at $D_{nom} = 0.5$.

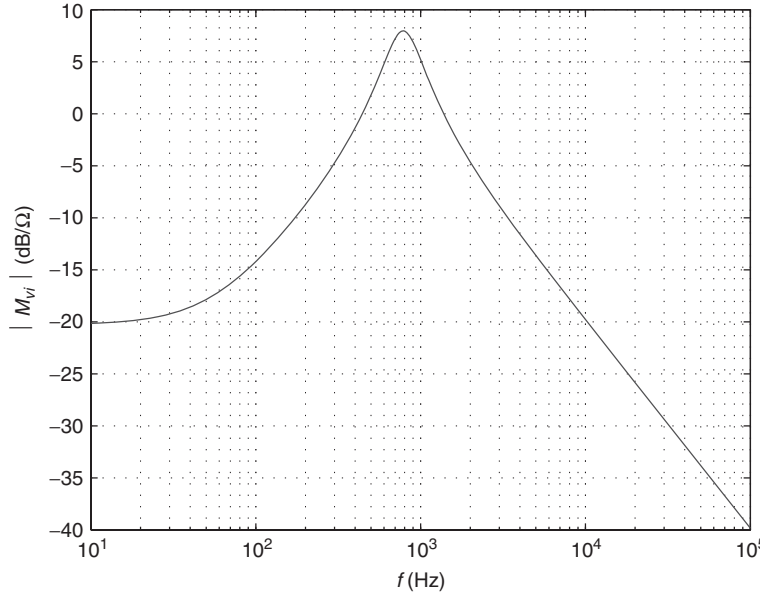


Figure 14.8 Bode plot of the magnitude of the open-loop input voltage-to-inductor current transfer function M_{vi} versus frequency for the boost converter.

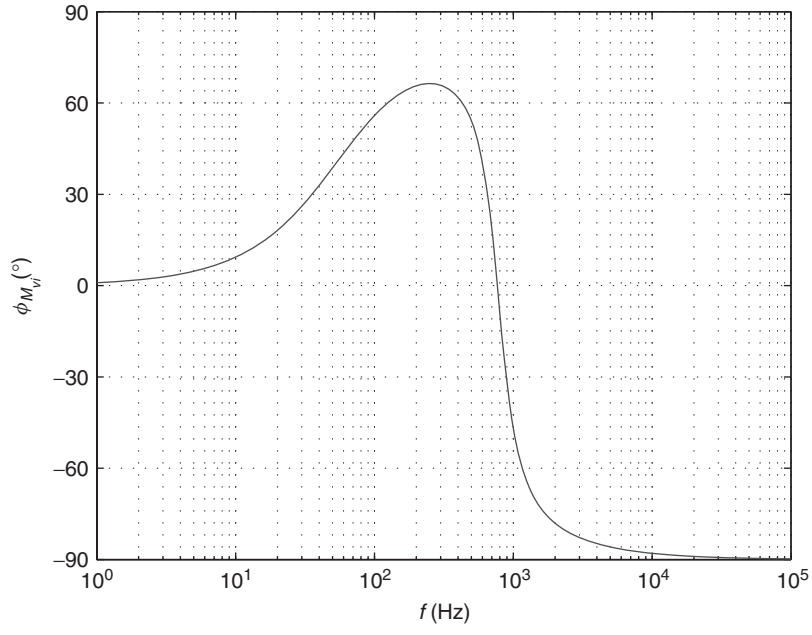


Figure 14.9 Bode plot of the phase of the open-loop input voltage-to-inductor current transfer function M_{vi} versus frequency for the boost converter.

Solution. The frequency of the zero is

$$f_{zi2} = \frac{1}{2\pi C(R_{Lmin} + r_C)} = \frac{1}{2\pi \times 68 \times 10^{-6} \times (40 + 0.111)} = 58.33\,\text{Hz}. \tag{14.46}$$

From (14.41),

$$M_{vio} = M_{vi}(0) = \frac{1}{(1 - D_{nom})^2 R_{Lmin} + r} = \frac{1}{(1 - 0.5)^2 \times 40 + 0.316}$$
$$= 0.09694\,\text{A/V} = -20.27\,\text{dBA/V}. \tag{14.47}$$

Figures 14.8 and 14.9 show the Bode plots of M_{vi}.

14.2.3 Open-loop Inductor-to-output Current Transfer Function

Figure 14.10 shows a small-signal model for deriving the open-loop inductor-to-output current transfer function for the boost converter. This model is obtained by setting $v_i = 0$ and $d = 0$ in the complete small-signal model depicted in Figure 14.1(a). By Kirchhoff's voltage law,

$$v_o - Dv_o + Z_1 i_l = 0, \tag{14.48}$$

which gives the output voltage

$$v_o = -\frac{i_l Z_1}{1 - D}. \tag{14.49}$$

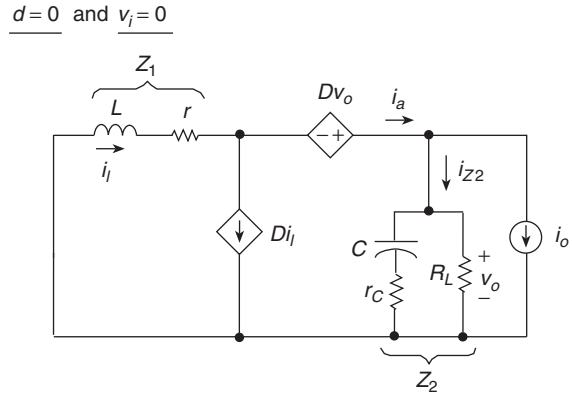


Figure 14.10 Small-signal model of the PWM boost converter for deriving the inductor-to-output current transfer function A_i.

By Kirchhoff's current law,

$$i_l - Di_l - i_a = 0, \tag{14.50}$$

from which

$$i_a = i_l(1 - D). \tag{14.51}$$

Likewise,

$$i_o + i_{Z2} - i_a = 0. \tag{14.52}$$

Using (14.49) gives

$$i_a = i_o + \frac{v_o}{Z_2} = i_o - \frac{i_l Z_1}{(1 - D)Z_2}. \tag{14.53}$$

Equating the right-hand sides of (14.51) and (14.53), one obtains

$$i_o = i_l \left[1 - D + \frac{Z_1}{(1 - D)Z_2}\right] = i_l \left[\frac{(1 - D)^2 Z_2 + Z_1}{(1 - D)Z_2}\right], \tag{14.54}$$

resulting in the inductor-to-output current transfer function

$$A_i(s) \equiv \left.\frac{i_l(s)}{i_o(s)}\right|_{v_i = d = 0} = \frac{(1 - D)Z_2}{Z_1 + (1 - D)^2 Z_2}. \tag{14.55}$$

Substitution of (14.7) and (14.8) into (14.55) yields

$$\begin{aligned} A_i(s) &= \frac{(1 - D)R_L r_C (s + \dfrac{1}{r_C C})}{L(R_L + r_C)\left\{s^2 + s\dfrac{C[r(R_L + r_C) + (1 - D)^2 R_L r_C] + L}{LC(R_L + r_C)} + \dfrac{r + (1 - D)^2 R_L}{LC(R_L + r_C)}\right\}} \\ &= \frac{(1 - D)R_L r_C}{L(R_L + r_C)} \frac{s - z_n}{s^2 + 2\xi\omega_0 s + \omega_0^2} = A_{ix} \frac{s + \omega_{zn}}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ &= A_{io} \frac{1 + \dfrac{s}{\omega_{zn}}}{1 + \dfrac{2\xi s}{\omega_0} + \left(\dfrac{s}{\omega_0}\right)^2}, \end{aligned} \tag{14.56}$$

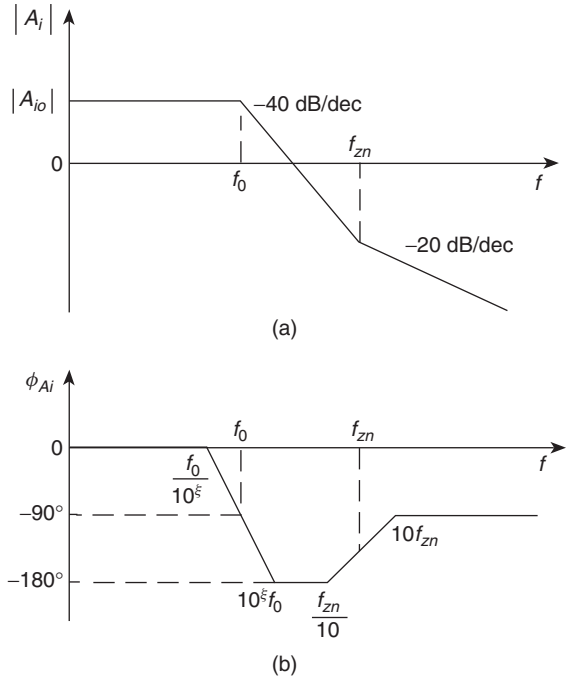


Figure 14.11 Idealized Bode plots of the open-loop input voltage-to-inductor current transfer function A_i for the boost converter. (a) $|A_i|$ versus f. (b) ϕ_{Ai} versus f.

where

$$\omega_{zn} = -z_n = \frac{1}{r_C C}, \tag{14.57}$$

$$A_{ix} = \frac{(1-D)R_L r_C}{L(R_L + r_C)}, \tag{14.58}$$

and

$$A_{io} = A_{io}(0) = \frac{(1-D)R_L r_C \omega_{zn}}{L(R_L + r_C)\omega_0^2} = \frac{(1-D)R_L}{(1-D)^2 R_L + r} \approx \frac{1}{1-D}. \tag{14.59}$$

Figure 14.11 depicts idealized Bode plots of A_i.

Example 14.4

The boost converter has $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. Calculate f_{zn} and A_{io} at $R_{Lmin} = 40\,\Omega$ and draw Bode plots of A_i at $D_{nom} = 0.5$.

Solution. The zero frequency is

$$f_{zn} = \frac{1}{2\pi C r_C} = \frac{1}{2\pi \times 68 \times 10^{-6} \times 0.111} = 21.09\,\text{kHz}. \tag{14.60}$$

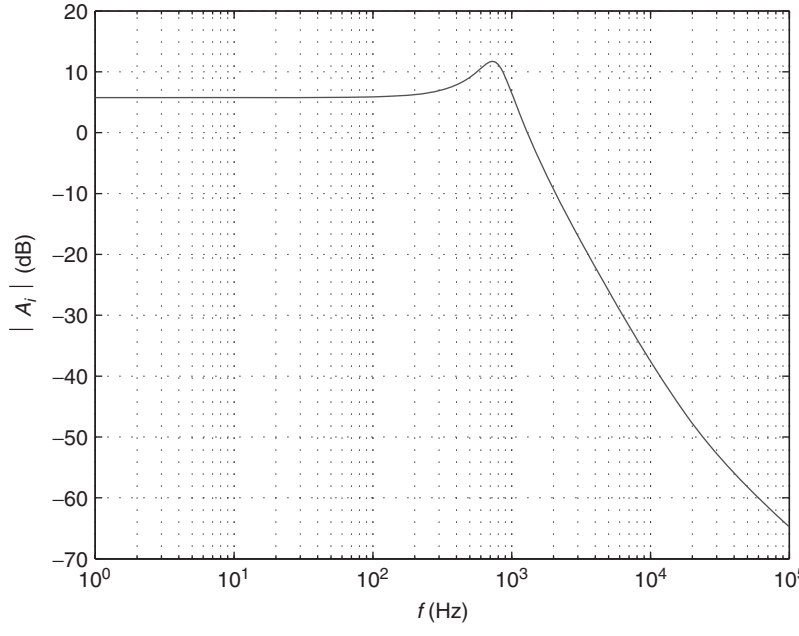


Figure 14.12 Bode plot of the magnitude of the open-loop inductor-to-output current transfer function A_i versus frequency for the boost converter.

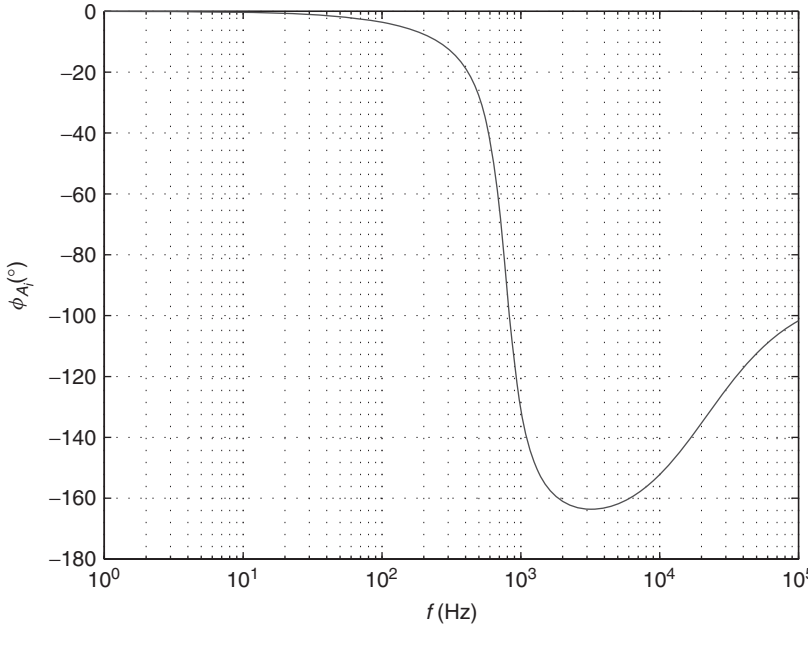


Figure 14.13 Bode plot of the phase of the open-loop inductor-to-output current transfer function A_i versus frequency for the boost converter.

From (14.41),

$$A_{io} = A_{io}(0) = \frac{(1 - D_{nom})R_{Lmin}}{(1 - D_{nom})^2 R_{Lmin} + r} = \frac{(1 - 0.5) \times 40}{(1 - 0.5)^2 \times 40 + 0.316} = 1.939 = 5.75\,\text{dB}. \tag{14.61}$$

Figures 14.12 and 14.13 show the Bode plots of A_i.

14.3 Open-loop Step Responses of Inductor Current

14.3.1 Open-loop Response of Inductor Current to Step Change in Input Voltage

Consider a step change in the input voltage of magnitude ΔV_I at time $t = 0$. The total input voltage is given by

$$v_I(t) = V_I(0^-) + \Delta V_I u(t), \tag{14.62}$$

where $u(t)$ is the unit step function and $V_I(0^-)$ is the steady-state input voltage before the step change. The step change in the input voltage in the time domain is expressed by

$$v_i(t) = v_I(t) - V_I(0^-) = \Delta V_I u(t), \tag{14.63}$$

which gives the step change of the input voltage in the s-domain,

$$v_i(s) = \frac{\Delta V_I}{s}. \tag{14.64}$$

From (14.39) and (14.64), the transient component of the inductor current of the open-loop boost converter in the s-domain is obtained as

$$i_l(s) = M_{vi}(s)v_i(s) = \frac{\Delta V_I M_{vi}(s)}{s} = \Delta V_I M_{vio} \frac{\omega_0^2}{\omega_{zi2}} \frac{s + \omega_{zi2}}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}. \tag{14.65}$$

Hence, one obtains the transient component of the inductor current of the open-loop boost converter in the time domain,

$$\begin{aligned} i_l(t) &= \mathcal{L}^{-1}\{i_l(s)\} \\ &= \Delta V_I M_{vio} \left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zi2}} + \left(\frac{\omega_0}{\omega_{zi2}}\right)^2} \frac{e^{-\xi\omega_0 t}}{\sqrt{1 - \xi^2}} \sin(\sqrt{1 - \xi^2}\omega_0 t + \phi) \right], \end{aligned} \tag{14.66}$$

where

$$\phi = \pi + \tan^{-1}\left(\frac{\sqrt{1 - \xi^2}}{\frac{\omega_{zi2}}{\omega_0} - \xi} \right) + \tan^{-1}\left(\frac{\sqrt{1 - \xi^2}}{\xi} \right), \qquad \text{for } \frac{f_{zi2}}{f_0} \geq \xi, \tag{14.67}$$

and

$$\phi = 2\pi + \tan^{-1}\left(\frac{\sqrt{1 - \xi^2}}{\frac{\omega_{zi2}}{\omega_0} - \xi} \right) + \tan^{-1}\left(\frac{\sqrt{1 - \xi^2}}{\xi} \right), \qquad \text{for } \frac{f_{zi2}}{f_0} < \xi. \tag{14.68}$$

Thus, the total inductor current is

$$i_L(t) = I_L(0^-) + i_l(t), \qquad \text{for } t \geq 0, \tag{14.69}$$

where $I_L(0^-)$ is the inductor current at time $t = 0^-$.

Setting the derivative of (14.84) to zero, one obtains the time instant at which the first and the highest maximum of i_l occurs,

$$\omega_0 t_m = \frac{1}{\sqrt{1-\xi^2}}\left[arctan\left(\frac{\sqrt{1-\xi^2}}{\xi - \dfrac{\omega_{zi2}}{\omega_0}}\right)\right], \quad \text{for } \frac{f_{zi2}}{f_0} < \xi. \tag{14.70}$$

The first maximum value of i_l is the highest one and occurs for $n = 1$. The highest maximum value of i_l is given by

$$i_{lmax} = \Delta V_I M_{vio}\left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zi2}} + \left(\frac{\omega_0}{\omega_{zi2}}\right)^2} e^{-\xi\omega_o t_m}\right], \tag{14.71}$$

resulting in the *maximum overshoot* of the transient component of the inductor current i_l,

$$\begin{aligned} S_{max} &\equiv \frac{i_{lmax} - i_l(\infty)}{i_l(\infty)} = \frac{i_{lmax}}{i_l(\infty)} - 1 = \frac{i_{lmax}}{\Delta V_I M_{vio}} - 1 \\ &= \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zi2}} + \left(\frac{\omega_0}{\omega_{zi2}}\right)^2} e^{-\xi\omega_0 t_m}, \end{aligned} \tag{14.72}$$

where $i_L(\infty) = M_{vio}\Delta V_I$ is the steady-state value of the transient component of the inductor current i_l after the transition.

The *maximum relative transient ripple* of the total inductor current is defined as

$$\delta_{max} \equiv \frac{i_{lmax} - i_l(\infty)}{i_L(\infty)} = \frac{i_{Lmax} - i_L(\infty)}{i_L(\infty)}, \tag{14.73}$$

where $i_L(\infty) = I_L(0^-) + i_l(\infty)$ is the steady-state value of the total inductor current after the transition.

Example 14.5

For the open-loop boost converter specified in Example 14.1, draw the waveform of the inductor current that is the response to the step change in the input voltage v_I from 12 to 13 V. Calculate (a) the maximum overshoot of the transient component of the inductor current, (b) the steady-state values of the transient component and the total inductor current, (c) the maximum relative transient ripple of the total inductor current.

Solution. Figure 14.14 shows the step response of the transient component of the inductor current i_L to a step change in the input voltage v_I from 12 to 13 V, which corresponds to a step change in v_i from 0 to 1 V, for the boost converter without feedback at $D_{nom} = 0.5$, $V_O = 20\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. The inductor current increases from 1 A to its peak value of 2 A and then reaches its steady-state value of $i_L(\infty) = 1.1\,\text{A}$ after approximately 3 ms.

From Examples 14.1 and 14.3, $\xi = 0.261$, $f_{zi2} = 58.35\,\text{Hz}$, $f_0 = 783.66\,\text{Hz}$, and $M_{vo} = 0.09694\,\text{A/V}$. The load current is $I_{Omax} = V_O/R_{Lmin} = 20/40 = 0.5\,\text{A}$ and the dc inductor current is $I_L = I_{Omax}/(1 - D_{nom}) = 0.5/(1 - 0.5) = 1\,\text{A}$. The steady-state value of the transient component of the inductor current is

$$i_l(\infty) = M_{vio}\Delta V_I = 0.09694 \times 1 = 0.09694\,\text{A}, \tag{14.74}$$

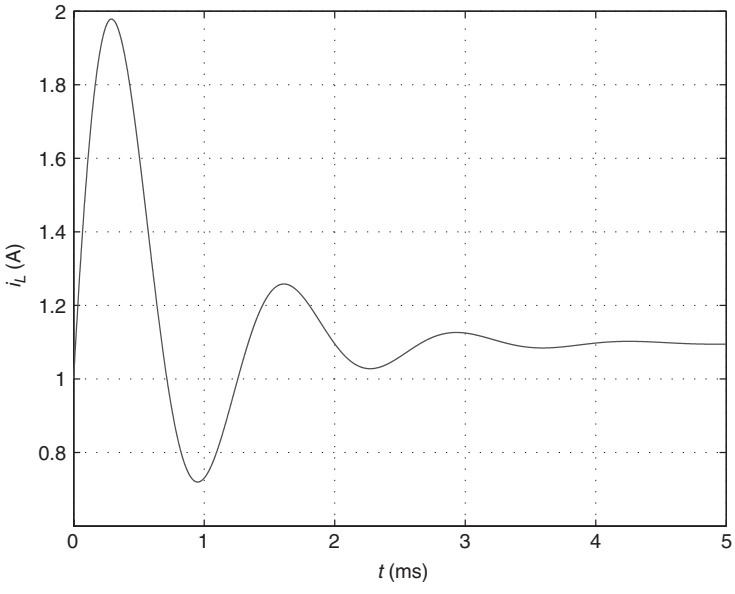


Figure 14.14 Response of the transient component of the inductor current i_L to a step change of v_I from 12 to 13 V for the boost converter without feedback for $D_{nom} = 0.5$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$.

resulting in the steady-state value of the total inductor current

$$i_L(\infty) = I_L(0^-) + i_l(\infty) = 1 + 0.09694 = 1.09694\,\text{A}. \tag{14.75}$$

Since $f_{zi1}/f_0 < \xi$, the first maximum of i_l is given by

$$\omega_0 t_m = \frac{1}{\sqrt{1-\xi^2}}\left[\arctan\left(\frac{\sqrt{1-\xi^2}}{\xi - \dfrac{f_{zi2}}{f_0}}\right)\right] = \frac{1}{\sqrt{1-0.261^2}}\left[\arctan\left(\frac{\sqrt{1-0.261^2}}{0.261 - \dfrac{58.35}{783.66}}\right)\right]$$
$$= 1.429\,\text{rad} = 81.9^\circ \tag{14.76}$$

resulting in $t_m = \omega_0 t_m/(2\pi f_0) = 1.429/(2\pi \times 783.66) = 0.29\,\text{ms}$. Using (14.72), one can compute the maximum overshoot of the transient component of the inductor current i_l

$$S_{max} = \sqrt{1 - \frac{2\xi f_0}{f_{zi2}} + \left(\frac{f_0}{f_{zi2}}\right)^2}\, e^{-\xi\omega_0 t_m}$$
$$= \sqrt{1 - \frac{2 \times 0.261 \times 783.66}{58.35} + \left(\frac{783.66}{58.35}\right)^2}\, e^{-0.261\times 1.429}$$
$$= 909.35\,\%. \tag{14.77}$$

Hence, the maximum value of the transient component of the inductor current is

$$i_{lmax} = (1 + S_{max})i_l(\infty) = (1 + 9.0935) \times 0.09694 = 0.9785\,\text{A}, \tag{14.78}$$

and the maximum relative transient ripple of the inductor current is

$$\delta_{max} = \frac{i_{lmax} - i_l(\infty)}{i_L(\infty)} = \frac{0.9785 - 0.09694}{1.09694} = 80.36\,\%. \tag{14.79}$$

14.3.2 Open-loop Response of Inductor Current to Step Change in Duty Cycle

Assume a step change in the duty cycle Δd_T at time $t = 0$. The total duty cycle is

$$d_T(t) = D + \Delta d_T u(t). \tag{14.80}$$

The step change in the duty cycle in the time domain is given by

$$d(t) = d_T(t) - D = \Delta d_T u(t), \tag{14.81}$$

which results in

$$d(s) = \frac{\Delta d_T}{s}. \tag{14.82}$$

Hence, using (14.9), the transient component of the inductor current of the open-loop boost converter in the s-domain is

$$i_l(s) = T_{pi}(s)d(s) = \frac{\Delta d_T T_{pi}(s)}{s} = \Delta d_T T_{pio}\frac{\omega_0^2}{\omega_{zi1}}\frac{s + \omega_{zi1}}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}. \tag{14.83}$$

The inverse Laplace transform of the inductor current of the open-loop boost converter in the time domain is

$$\begin{aligned} i_l(t) &= \mathcal{L}^{-1}\{i_l(s)\} \\ &= \Delta d_T T_{pio}\left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zi1}} + \left(\frac{\omega_0}{\omega_{zi1}}\right)^2}\frac{e^{-\xi\omega_0 t}}{\sqrt{1-\xi^2}}\sin(\sqrt{1-\xi^2}\omega_0 t + \phi)\right], \end{aligned} \tag{14.84}$$

where

$$\phi = \pi + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\frac{\omega_{zi1}}{\omega_0} - \xi}\right) + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right), \quad \text{for } \frac{\omega_{zi1}}{\omega_0} \geq \xi, \tag{14.85}$$

or

$$\phi = 2\pi + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\frac{\omega_{zi1}}{\omega_0} - \xi}\right) + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right), \quad \text{for } \frac{\omega_{zi1}}{\omega_0} < \xi. \tag{14.86}$$

Example 14.6

For the open-loop boost converter specified in Example 14.1, draw the waveform of the inductor current i_L that is the response to the step change in the duty cycle d_T from 0.5 to 0.6. Calculate the inductor current for the steady state after the transition and the maximum relative transient ripple.

Solution. Figure 14.15 shows the response of the transient component of the inductor current i_L to a step change in the duty cycle d_T from 0.5 to 0.6 for $d = 0.1$ for the boost converter without feedback at $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. The inductor current i_L increases from 1 A to a peak value of 3.1 A and then reaches a steady-state value of approximately 1.4 A after 3 ms.

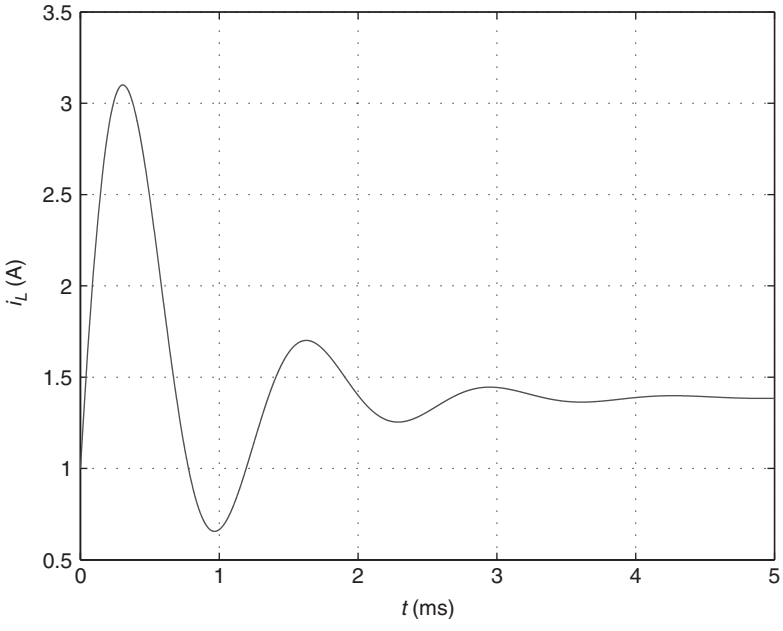


Figure 14.15 Response of the transient component of the inductor current i_L to a step change in the duty cycle d_T from 0.5 to 0.6 for the boost converter without feedback for $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.4\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$.

From Example 14.1, $T_{pio} = 3.8775\,\text{A}$, $\xi = 0.261$, $f_{zi1} = 116.38\,\text{Hz}$, and $f_0 = 783.66\,\text{Hz}$. The steady-state value of the transient component of the inductor current is

$$i_l(\infty) = T_{pio}\Delta d_T = 3.8775 \times 0.1 = 0.38775\,\text{A}. \tag{14.87}$$

Thus, the total steady-state inductor current is

$$i_L(\infty) = I_L(0^-) + i_l(\infty) = 1 + 0.38775 = 1.38775\,\text{A}. \tag{14.88}$$

Since $f_{zi1}/f_0 < \xi$, the first maximum of i_l occurs at

$$\omega_0 t_m = \frac{1}{\sqrt{1-\xi^2}}\left[\arctan\left(\frac{\sqrt{1-\xi^2}}{\xi - \dfrac{\omega_{zi1}}{\omega_0}}\right)\right] = \frac{1}{\sqrt{1-0.261^2}}\left[\arctan\left(\frac{\sqrt{1-0.261^2}}{0.261 - \dfrac{116.38}{783.66}}\right)\right]$$
$$= 1.507\,\text{rad} \ = 86.34^\circ, \tag{14.89}$$

from which $t_m = 1.507/(2\pi f_0) = 1.507/(2\pi \times 783.66) = 0.3059\,\text{ms}$. The maximum overshoot is

$$S_{max} = \sqrt{1 - \frac{2\xi f_0}{f_{zi1}} + \left(\frac{f_0}{f_{zi1}}\right)^2} e^{-\xi\omega_0 t_m}$$
$$= \sqrt{1 - \frac{2 \times 0.261 \times 783.66}{116.38} + \left(\frac{783.66}{116.38}\right)^2} e^{-0.261 \times 1.507} = 442.65\,\%, \tag{14.90}$$

yielding the maximum value of the transient component of the inductor current,

$$i_{lmax} = (1 + S_{max})i_l(\infty) = (1 + 4.4265) \times 0.38775 = 2.1\,\text{A}, \tag{14.91}$$

and the maximum relative transient ripple of the inductor current,

$$\delta_{max} = \frac{i_{lmax} - i_l(\infty)}{i_L(\infty)} = \frac{2.1 - 0.38775}{1.38775} = 123.38\,\%. \tag{14.92}$$

14.3.3 Open-loop Response of Inductor Current to Step Change in Load Current

The total load current with a step change ΔI_O at $t = 0$ is

$$i_O(t) = I_O + \Delta I_O u(t), \tag{14.93}$$

and the step change in the load current is

$$i_o(t) = i_O(t) - I_O = \Delta I_O u(t), \tag{14.94}$$

from which

$$i_o(s) = \frac{\Delta I_O}{s}. \tag{14.95}$$

Thus, the transient component of the inductor current is

$$i_l(s) = A_i(s) i_o(s) = \frac{\Delta I_O A_{io}(s)}{s} = \Delta I_O A_{io} \frac{\omega_0^2}{\omega_{zn}} \frac{s + \omega_{zn}}{s(s^2 + 2\xi\omega_0 s + \omega_0^2)}, \tag{14.96}$$

leading to

$$\begin{aligned} i_l(t) &= \mathcal{L}^{-1}\{i_l(s)\} \\ &= \Delta I_O A_{io} \left[1 + \sqrt{1 - \frac{2\xi\omega_0}{\omega_{zn}} + \left(\frac{\omega_0}{\omega_{zn}}\right)^2} \frac{e^{-\xi\omega_0 t}}{\sqrt{1-\xi^2}} \sin(\sqrt{1-\xi^2}\omega_0 t + \phi) \right], \end{aligned} \tag{14.97}$$

where

$$\phi = \pi + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\frac{\omega_{zn}}{\omega_0} - \xi} \right) + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi} \right), \qquad \text{for } \frac{\omega_{zn}}{\omega_0} \geq \xi \tag{14.98}$$

or

$$\phi = 2\pi + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\frac{\omega_{zn}}{\omega_0} - \xi} \right) + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi} \right), \qquad \text{for } \frac{\omega_{zn}}{\omega_0} < \xi. \tag{14.99}$$

Example 14.7

For the open-loop boost converter specified in Example 14.1, draw the waveform of the inductor current i_L that is a response to the step change in the load current ΔI_O from 0.5 to 0.6 A. Calculate the inductor current for steady state after the transition and the maximum relative transient ripple.

Solution. Figure 14.16 shows the response of the transient component of the inductor current i_L to a step change in the load current ΔI_O from 0.5 to 0.6 A for $\Delta I_O = 0.1$ A for the boost converter without feedback at $V_{Inom} = 12$ V, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$,

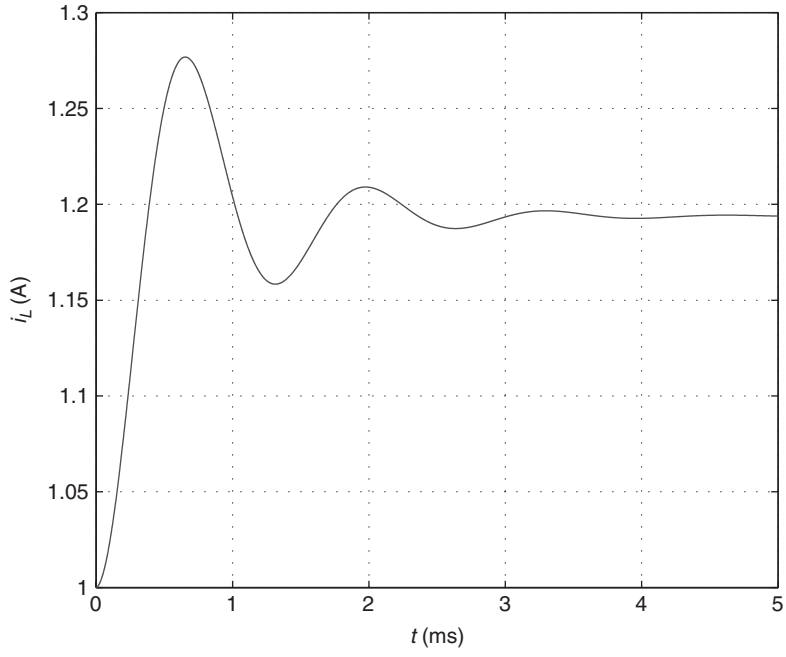


Figure 14.16 Response of the transient component of the inductor current i_L to a step change in the load current ΔI_O from 0.5 to 0.6 A for the boost converter without feedback for $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.4\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, and $r_C = 0.111\,\Omega$.

$R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, and $r_C = 0.111\,\Omega$. The inductor current i_L increases from 1 A to a peak value of 1.3 A and then reaches a steady-state value of approximately 1.2 A after 3 ms.

From Examples 14.1 and 14.4, $A_{io} = 1.939$, $\xi = 0.261$, $f_{zn} = 21.09\,\text{kHz}$, and $f_0 = 783.66\,\text{Hz}$. The transient component of the inductor current is

$$i_l(\infty) = A_{io}\,\Delta I_O = 1.939 \times 0.1 = 0.1939\,\text{A}. \tag{14.100}$$

Thus, the total steady-state inductor current is

$$i_L(\infty) = I_L(0^-) + i_l(\infty) = 1 + 0.1939 = 1.1939\,\text{A}. \tag{14.101}$$

Since $f_{zn}/f_0 = 21{,}090/783.66 = 26.9 \gg \xi = 0.261$,

$$\omega_0 t_m = \frac{\pi}{\sqrt{1-\xi^2}} == \frac{\pi}{\sqrt{1-0.261^2}} = 3.254\,\text{rad} \;= 186.44^\circ \tag{14.102}$$

producing $t_m = 3.254/(2\pi f_0) = 3.245/(2\pi \times 783.66) = 0.66\,\text{ms}$. Furthermore, the maximum overshoot is given by

$$S_{max} = \sqrt{1 - \frac{2\xi f_0}{f_{zn}} + \left(\frac{f_0}{f_{zn}}\right)^2}\, e^{-\pi\xi/\sqrt{1-\xi^2}}$$

$$= \sqrt{1 - \frac{2 \times 0.261 \times 0.784}{21.09} + \left(\frac{0.784}{21.09}\right)^2}\, e^{-\pi \times 0.261/\sqrt{1-0.261^2}} = 42.34\,\%, \tag{14.103}$$

giving the maximum value of the transient component of the inductor current,

$$i_{lmax} = (1 + S_{max}) i_l(\infty) = (1 + 0.4234) \times 0.1939 = 0.2759\,\text{A}, \tag{14.104}$$

and the maximum relative transient ripple of the inductor current,

$$\delta_{max} = \frac{i_{lmax} - i_l(\infty)}{i_L(\infty)} = \frac{0.2759 - 0.1939}{1.1939} = 6.8\,\%. \tag{14.105}$$

14.4 Closed-current-loop Transfer Functions

The transfer function of the current modulator is given by [16]

$$T_{ms}(s) = \frac{d(s)}{v_{ei}(s)} \approx \frac{12f_s^2}{R_s T_{pi} s\left(s + \dfrac{1-a}{1+a}6f_s\right)} = \frac{12f_s^2}{R_s T_{pi} s(s+\omega_{sh})}$$

$$= \frac{12f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix} s(s+\omega_{sh})(s+\omega_{zi1})} = T_{msx}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{s^3 + (\omega_{sh}+\omega_{zi1})s^2 + \omega_{sh}\omega_{zi1}s}, \tag{14.106}$$

where

$$a = \frac{M_2 - M_3}{M_1 + M_3} = \frac{\dfrac{D}{1-D} - \dfrac{M_3}{M_1}}{1 + \dfrac{M_3}{M_1}}, \tag{14.107}$$

$$\omega_{sh} = \frac{1-a}{1+a}6f_s, \tag{14.108}$$

and

$$T_{msx} = \frac{12f_s^2}{R_s T_{pix}}. \tag{14.109}$$

The transfer function T_{ms} depends on converter topology because it depends on T_{pi}, which is different for different converters.

The loop gain of the current loop is [16]

$$T_i(s) \equiv \frac{v_{fi}(s)}{v_{ei}(s)}|_{v_i = i_o = 0} = T_{ms}(s)T_{pi}(s)R_s \approx \frac{12f_s^2}{s\left(s + \dfrac{1-a}{1+a}6f_s\right)} = \frac{12f_s^2}{s(s+\omega_{sh})}$$

$$= 2f_s\frac{1+a}{1-a}\frac{1}{s\left(1 + \dfrac{s}{\omega sh}\right)} = \frac{\omega_1}{s}\frac{1}{1 + \dfrac{s}{\omega_{sh}}}. \tag{14.110}$$

The current loop gain T_i is independent of converter topology and the sense resistor R_s.

The closed-loop gain of the current loop is described by [16]

$$T_{icl}(s) = \frac{d(s)}{v_c(s)} = \frac{T_{ms}}{1 + T_{ms}T_{pi}R_s} = \frac{T_{ms}}{1+T_i} = \frac{T_{ms}s(s+\omega_{sh})}{s^2 + \omega_{sh}s + 12f_s^2}$$

$$= \frac{12f_s^2}{R_s T_{pi} s(s + \omega_{sh} + 12f_s^2)} = \frac{12f_s^2(s^2 + 2\xi\omega_0 s + \omega_0^2)}{R_s T_{pix}(s^2 + \omega_{sh}s + 12f_s^2)(s+\omega_{zi1})}$$

$$= T_{iclx}\frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{s^3 + (\omega_{sh}+\omega_{zi1})s^2 + (12f_s^2 + \omega_{sh}\omega_{zi1})s + 12f_s^2\omega_{zi1}}, \tag{14.111}$$

where

$$T_{iclx} = \frac{12f_s^2}{R_s T_{pix}}. \tag{14.112}$$

For $s = 0$,

$$T_{iclo} = T_{icl}(0) = \frac{\omega_0^2}{R_s T_{pix} \omega_{zi1}} = \frac{(1-D)^2 R_L + r}{2R_s V_O}. \tag{14.113}$$

The closed-loop control voltage-to-inductor current transfer function is given by

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{T_{ms} T_{pi}}{1 + T_i} = T_{icl} T_{pi} = \frac{12 f_s^2}{R_s \left(s^2 + \dfrac{1-\alpha}{1+\alpha} 6 f_s s + 12 f_s^2 \right)}. \tag{14.114}$$

Example 14.8

For the boost converter with $R_s = 1\,\Omega$, $V_{Inom} = 12\,\text{V}$, $V_O = 20\,\text{V}$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $r = 0.316\,\Omega$, $f_{zi1} = 116.38$ Hz, $f_0 = 783.66\,\text{Hz}$, $\xi = 0.261$, $\eta = 0.85$, and $f_s = 100\,\text{kHz}$, find the compensation slope M_{3nom}, which gives the phase margin of the inner loop $PM = 60^\circ$. Calculate T_{iclo} at $R_{Lmin} = 40\,\Omega$. Draw Bode plots of T_{ms}, T_i, T_{icl}, and H_{icl} and responses of d_T and i_L to a step change $\Delta V_c = 0.25\,\text{V}$.

Solution. The nominal duty cycle is

$$D_{nom} = 1 - \frac{\eta}{M_{V\,DCnom}} = 1 - \frac{\eta}{\dfrac{V_O}{V_{Inom}}} = 1 - \frac{0.85}{\dfrac{20}{12}} = 0.49 \approx 0.5. \tag{14.115}$$

The slope of the rising inductor current is

$$M_{1nom} = \frac{V_{Inom}}{L} = \frac{12}{156 \times 10^{-6}} = 76{,}923\,\text{V/s} \tag{14.116}$$

and the slope of the falling inductor current is

$$M_{2nom} = \frac{D_{nom}}{1 - D_{nom}} M_{1nom} = \frac{0.5}{1 - 0.5} \times 76{,}923 = 76{,}923\,\text{V/s}. \tag{14.117}$$

Next,

$$a = \frac{\sqrt[4]{9(1 + \tan^2 PM)} - \tan PM}{\sqrt[4]{9(1 + \tan^2 PM)} + \tan PM} = \frac{\sqrt[4]{9(1 + \tan^2 60^\circ)} - \tan 60^\circ}{\sqrt[4]{9(1 + \tan^2 60^\circ)} + \tan 60^\circ} = 0.1716. \tag{14.118}$$

From (14.107),

$$M_{3nom} = \frac{M_{2nom} - a M_{1nom}}{1 + a} = \frac{76{,}923 - 0.1716 \times 76{,}923}{1 + 0.1716} = 54{,}389.7\,\text{V/s}. \tag{14.119}$$

The amplitude of the compensating voltage is

$$V_{Am} = M_{3nom} T_s = \frac{M_{3nom}}{f_s} = \frac{54{,}389.7}{10^5} = 0.544\,\text{V}. \tag{14.120}$$

The damping factor is

$$\xi_i = \frac{\sqrt{3}}{2} \frac{1-a}{1+a} = \left(\frac{\sqrt{3}}{2} \right) \frac{1 - 0.1716}{1 + 0.1716} = 0.6123. \tag{14.121}$$

The corner frequency is

$$f_{sh} = \left(\frac{3}{\pi} \right) \frac{1-a}{1+a} f_s = \left(\frac{3}{\pi} \right) \frac{1 - 0.1716}{1 + 0.1716} \times 10^5 = 67.52\,\text{kHz}. \tag{14.122}$$

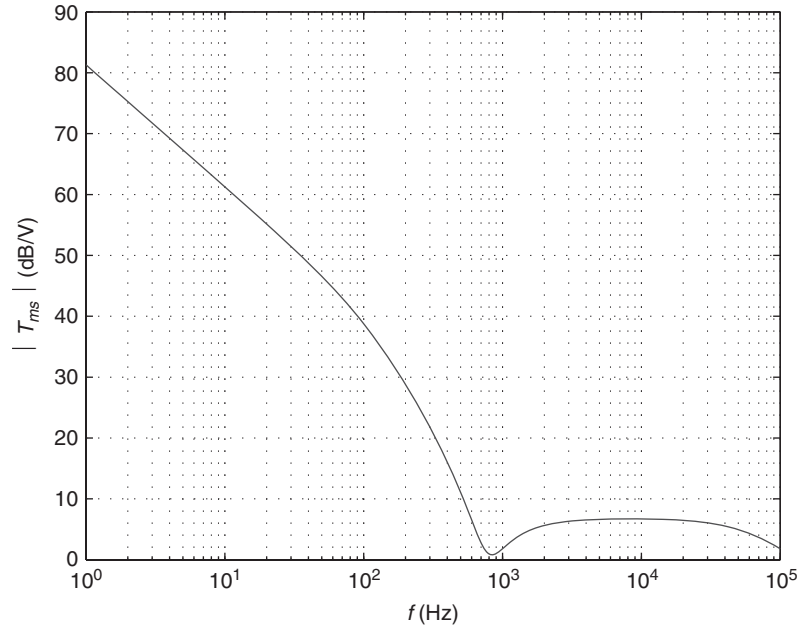


Figure 14.17 Bode plot of the magnitude of T_{ms} for the boost converter.

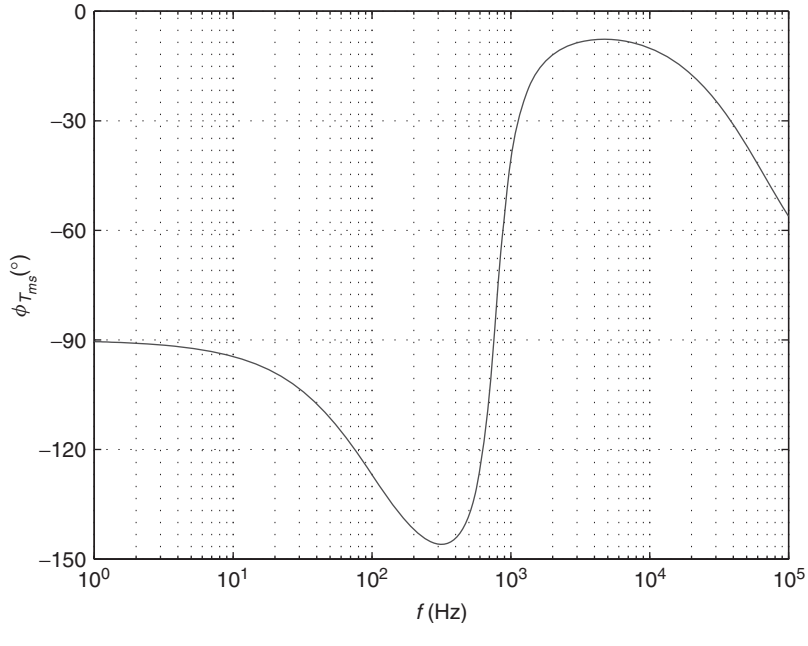


Figure 14.18 Bode plot of the phase of T_{ms} for the boost converter.

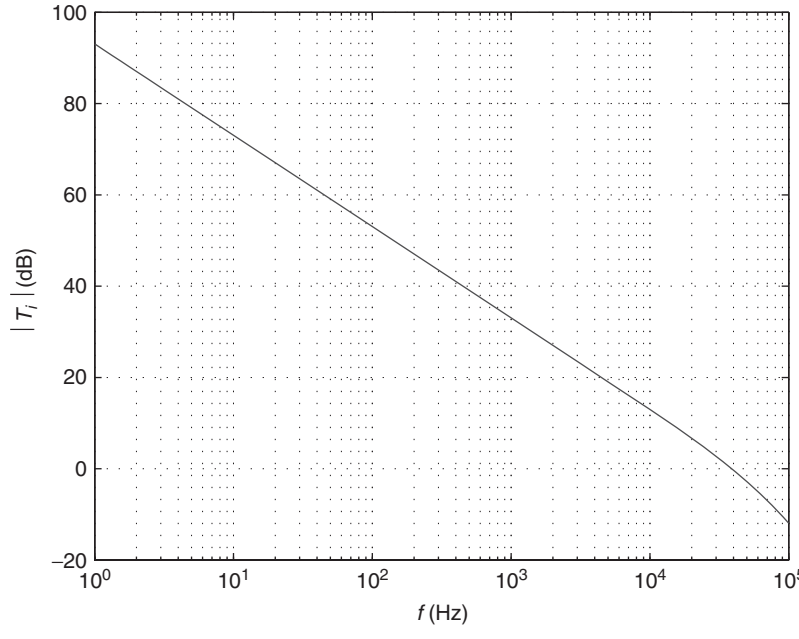


Figure 14.19 Bode plot of the magnitude of the current loop gain T_i for the boost converter.

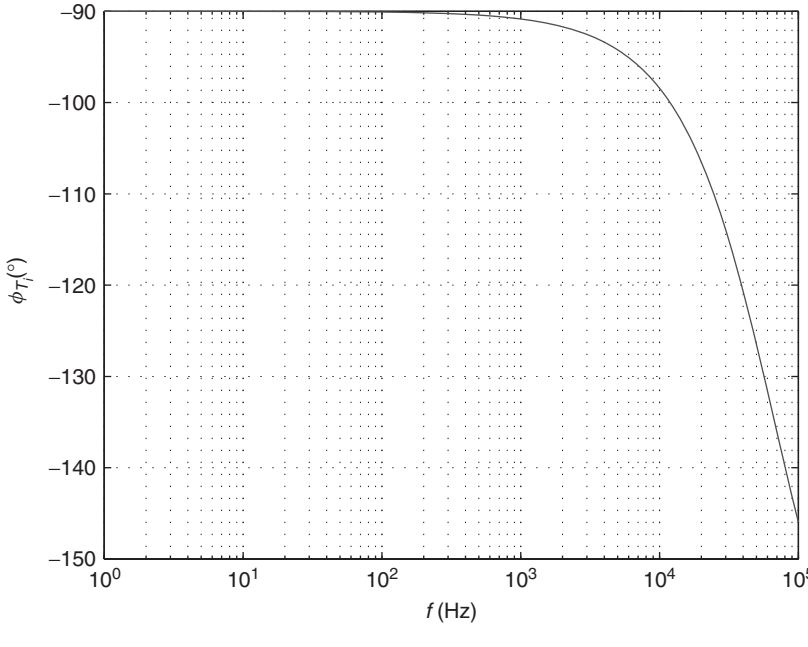


Figure 14.20 Bode plot of the phase of the current loop gain T_i for the boost converter.

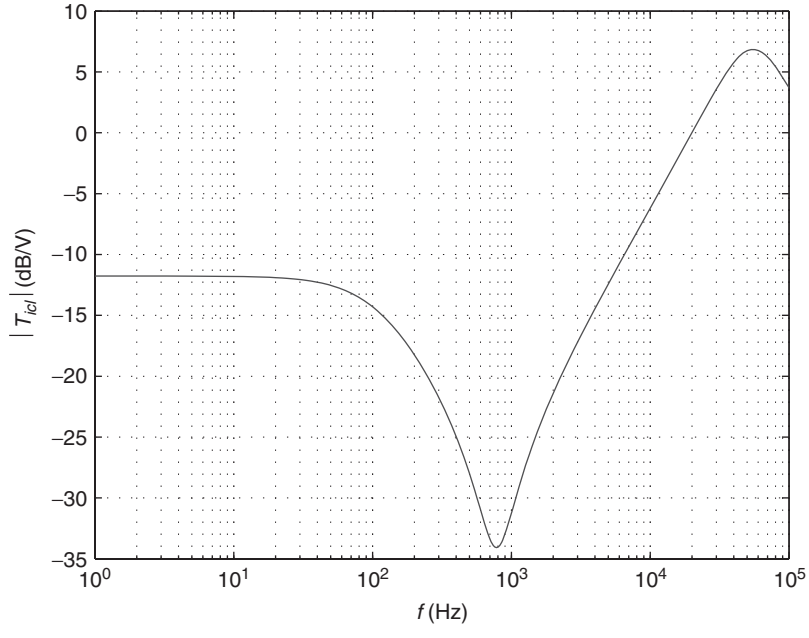


Figure 14.21 Bode plot of the magnitude of the closed-loop gain of the current loop T_{icl} for the boost converter.

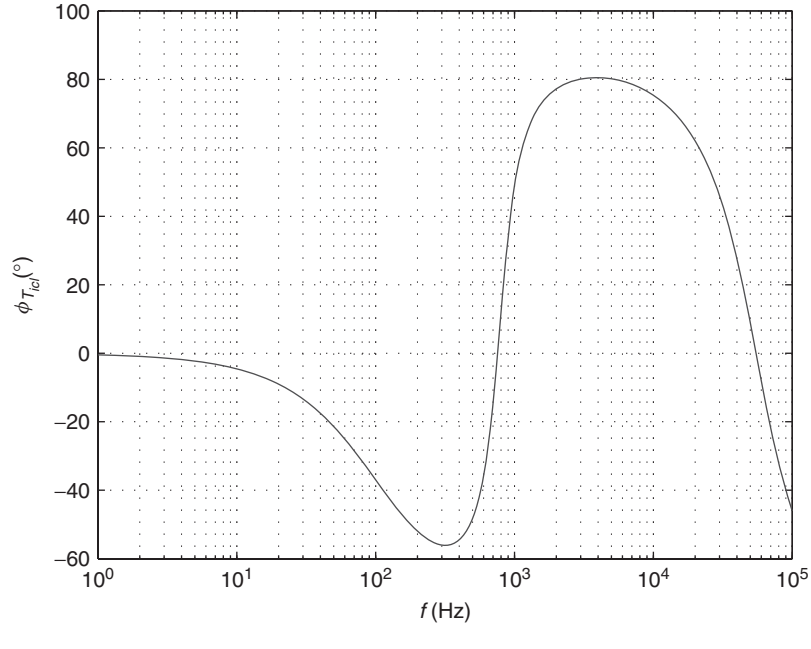


Figure 14.22 Bode plot of the phase of the closed-loop gain of the current loop T_{icl} for the boost converter.

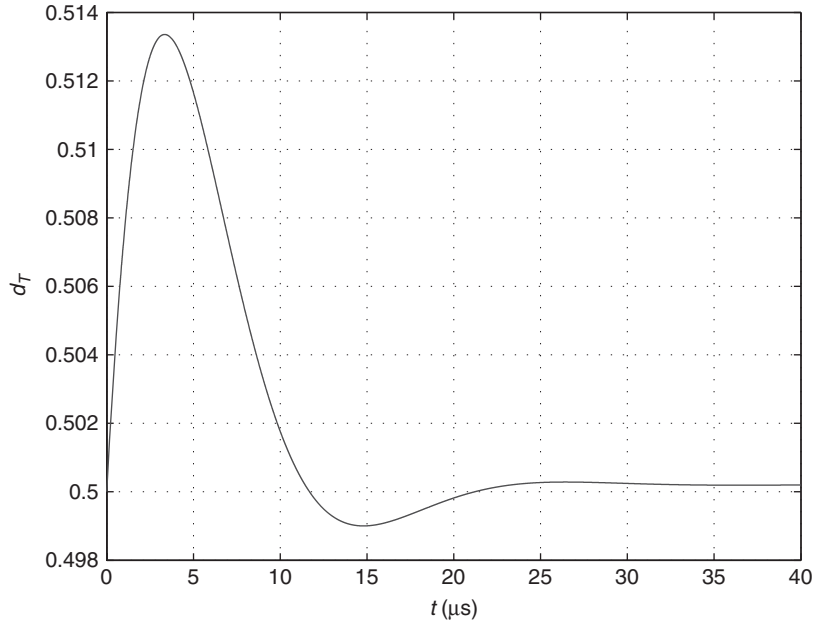


Figure 14.23 Response of the duty cycle d_T to a step change in the control voltage $v_c = 0.01\,\text{V}$ in the boost converter at $a = 0.1716$, $R_s = 1\,\Omega$, $V_O = 20\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, $r_C = 0.111\,\Omega$, $f_0 = 783.66\,\text{Hz}$, $f_{zi1} = 116.38\,\text{Hz}$, and $\xi = 0.261$.

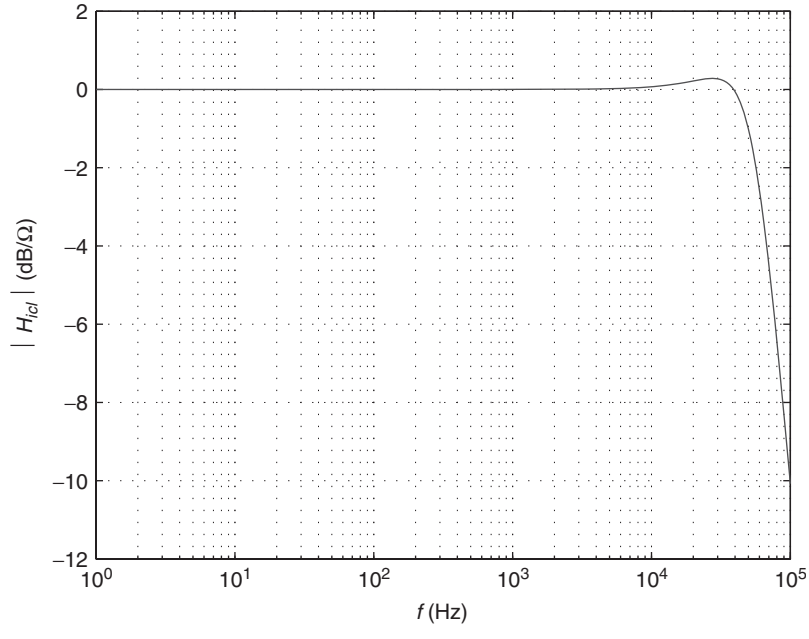


Figure 14.24 Bode plot of the magnitude of the closed-loop gain of the current loop H_{icl} for the boost converter.

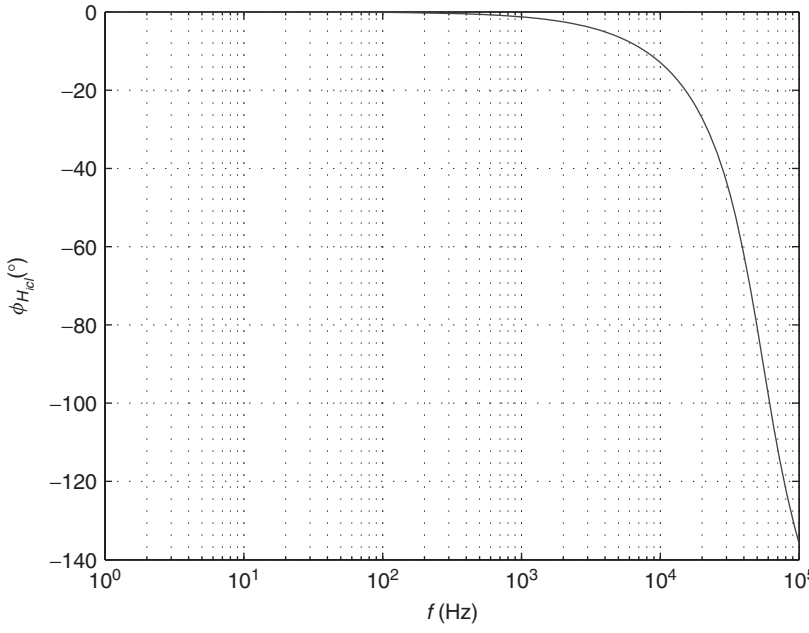


Figure 14.25 Bode plot of the phase of the closed-loop gain of the current loop H_{icl} for the boost converter.

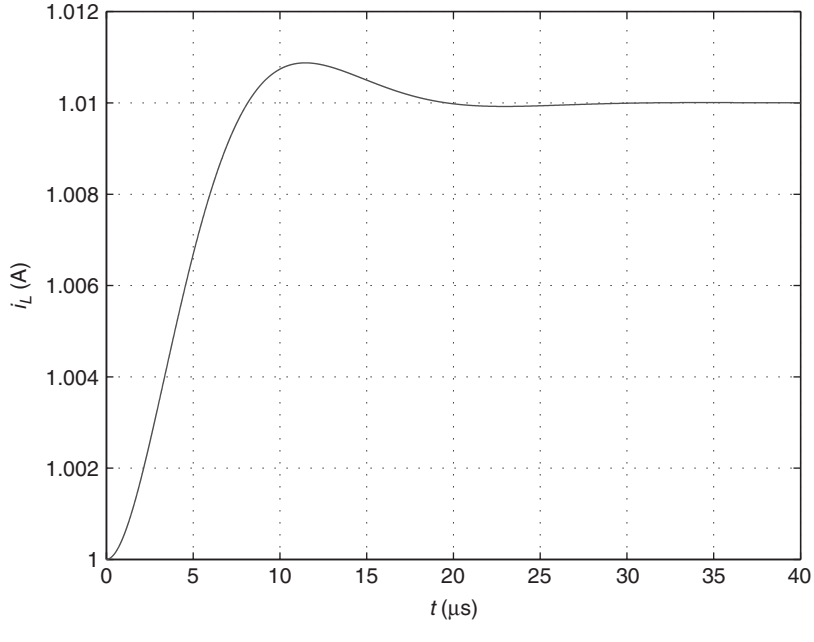


Figure 14.26 Response of the inductor current i_L to a step change in the control voltage $v_c = 0.01\,\text{V}$ in the boost converter at $a = 0.1716$, $R_s = 1\,\Omega$, $V_O = 20\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $D_{nom} = 0.5$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r = 0.316\,\Omega$, $r_C = 0.111\,\Omega$, $f_0 = 783.66\,\text{Hz}$, $f_{zi1} = 116.38\,\text{Hz}$, and $\xi = 0.261$.

The unity-gain frequency is

$$f_1 = \left(\frac{f_s}{\pi}\right)\frac{1+a}{1-a} = \left(\frac{10^5}{\pi}\right)\frac{1+0.1716}{1-0.1716} = 45\,\text{kHz}. \tag{14.123}$$

The closed-loop transfer function of the current loop at $f = 0$ is given by

$$T_{iclo} = T_{icl}(0) = \frac{(1-D_{nom})^2 R_{Lmin} + r}{2R_s V_O} = \frac{(1-0.5)^2 \times 40 + 0.316}{2 \times 1 \times 20}$$
$$= 0.25979\,\text{V}^{-1} = -11.708\,\text{dB/V}. \tag{14.124}$$

Figures 14.17 through 14.22 show Bode plots of T_{ms}, T_i, and T_{icl}. The Bode plots of T_i show that the crossover frequency is $f_{ci} = 38\,\text{kHz}$, $GM = \infty$, and $PM = 60^\circ$. Figure 14.23 depicts the response of the duty cycle to a step change in the control voltage v_c. The steady-state value of the total duty cycle is

$$d_T(\infty) = D(0^-) + T_{iclo}\Delta V_c = 0.5 + 0.25979 \times 0.01 \approx 0.5026. \tag{14.125}$$

Figures 14.24 and 14.25 show Bode plots of H_{icl}. The response of the inductor function i_L to a step change in the control voltage v_c at $a = 0.1716$ is depicted in Figure 14.26. The steady-state value of the inductor current is

$$i_L(\infty) = I_L(0^-) + \frac{\Delta V_c}{R_s} = 1 + \frac{0.01}{1} = 1.01\,\text{V}. \tag{14.126}$$

14.4.1 Input Voltage-to-duty Cycle Transfer Function

A block diagram for deriving the input voltage-to-duty cycle transfer function M_{vd} for the closed-current loop without feedforward gian K_i is shown in Figure 14.27. The inductor current is determined by

$$i_l = i_l' + i_l'' = T_{pi}d + M_{vi}i_o, \tag{14.127}$$

and the duty cycle is

$$d = T_{ms}(-R_s i_l) = -T_{ms}R_s T_{pi}d - T_{ms}R_s M_{vi}v_i, \tag{14.128}$$

leading to

$$d(1 + T_{ms}R_s T_{pi}) = -T_{ms}R_s M_{vi}v_i. \tag{14.129}$$

Thus, the input voltage-to-duty cycle transfer function for the closed-current loop is

$$M_{vd}(s) \equiv \left.\frac{d(s)}{v_i(s)}\right|_{v_c = i_o = 0} = -\frac{R_s T_{ms} M_{vi}}{1 + T_i} = -T_{icl}M_{vi}R_s$$
$$= -\frac{12 f_s^2 M_{vix}(s + \omega_{zi2})}{T_{pix}(s + \omega_{zi1})(s^2 + \omega_{sh}s + 12f_s^2)}. \tag{14.130}$$

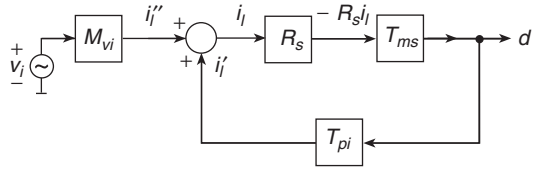


Figure 14.27 Block diagram for deriving the input voltage-to-duty cycle transfer function.

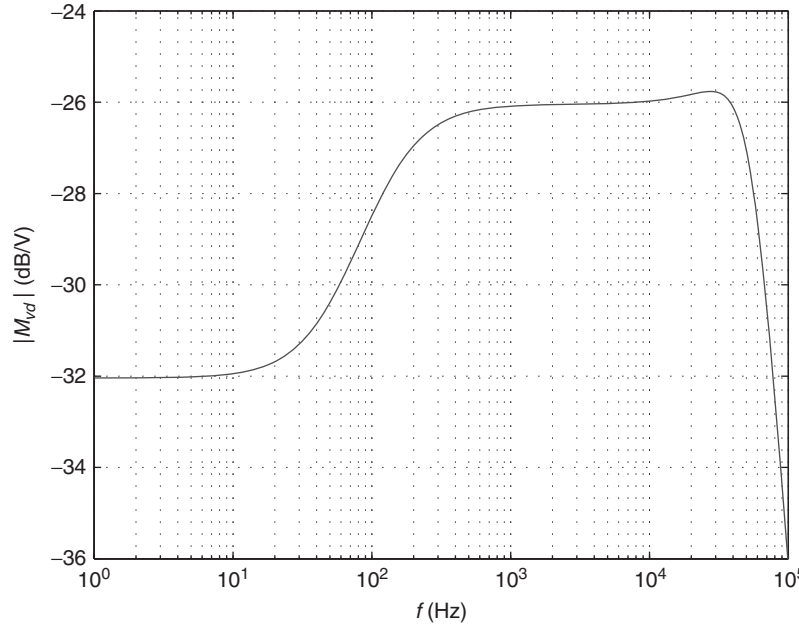


Figure 14.28 Bode plot of the magnitude of M_{vd} for the boost converter without feedforward gain K_i.

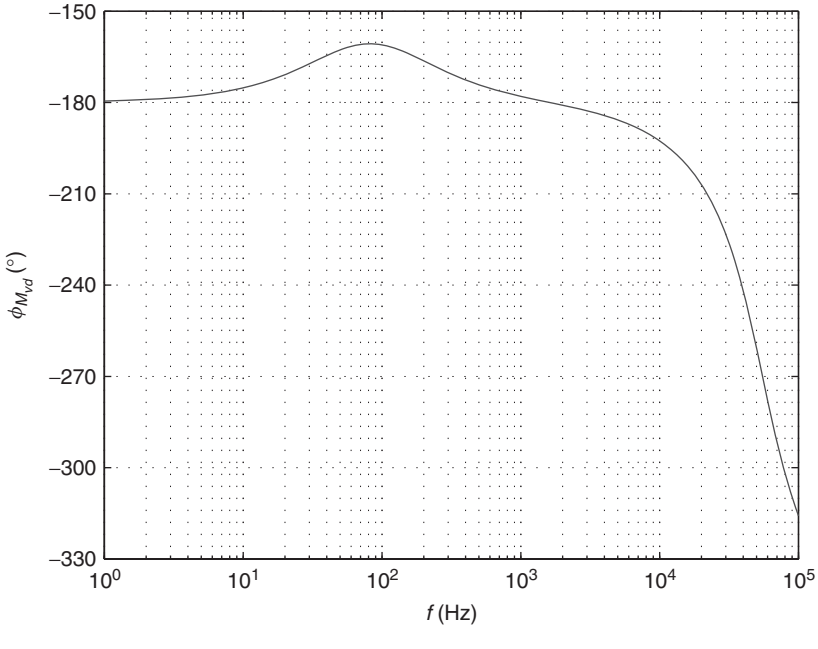


Figure 14.29 Bode plot of the phase of M_{vd} for the boost converter without feedforward gain K_i.

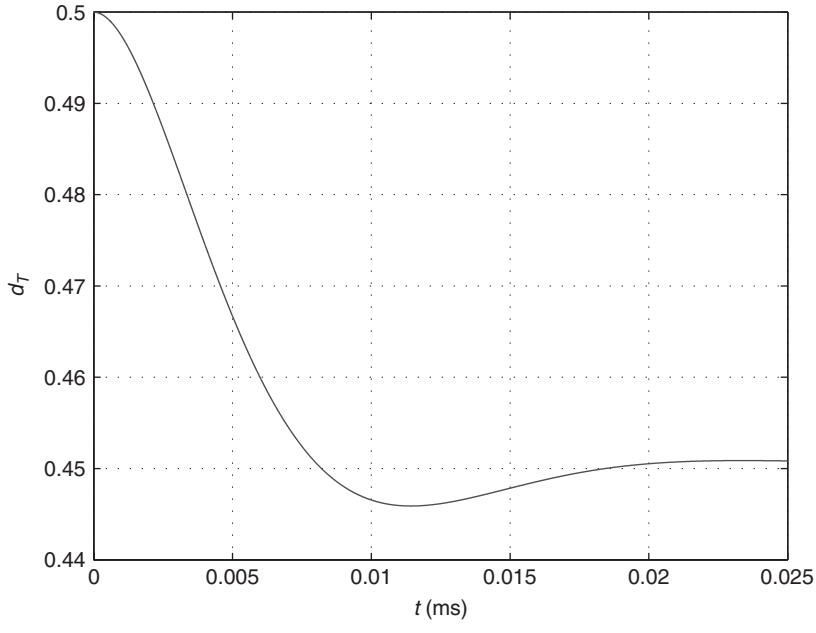


Figure 14.30 Response of d_T to a step change $\Delta V_I = 1$ V from 12 to 13 V for the boost converter without feedforward gain $K_i = 0.04167$.

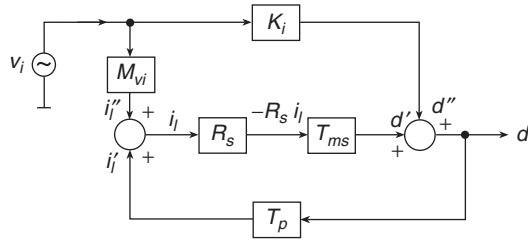


Figure 14.31 Block diagram for deriving the input voltage-to-duty cycle transfer function M_{vdf} with feedforward gain K_i.

For $s = 0$,

$$M_{vdo} = M_{vd}(0) = -\frac{M_{vix}\omega_{zi2}}{T_{pix}\omega_{zi1}} = \frac{R_L + r_C}{V_O(R_L + 2r_C)} \approx -\frac{1}{V_O} = -\frac{1}{20} = -0.05\,\text{V}^{-1} \quad (14.131)$$

which gives $|M_{vdo}| = -32$ dB/V. Figures 14.28 and 14.29 show Bode plots of M_{vi}. Figure 14.30 depicts the response of the duty cycle to a step change in the input voltage from 20 to 21 V. The steady-state value of the duty cycle is

$$d_T(0^-) = D(0^-) + M_{vdo}\Delta V_I = 0.5 - 0.05 \times 1 = 0.45. \quad (14.132)$$

Figure 14.31 shows a block diagram for finding the input voltage-to-duty cycle transfer function with feedforward control K_i when the outer voltage loop is open. The feedforward coefficients for the boost converter are given by

$$K_i = -\frac{D}{V_I} = \frac{D^2}{V_O(1-D)} = -\frac{0.5}{12} = -0.04167 \quad (14.133)$$

and

$$K_o = 0. \tag{14.134}$$

The inductor current is

$$i_l = i_l{}' + i_l{}'' = T_{pi} d + M_{vi} v_i . \tag{14.135}$$

The components of the duty cycle are

$$d' = -R_s T_{ms} i_l = -R_s T_{ms} (T_{pi} d + M_{vi} v_i) = -R_s T_{ms} d - R_s T_{ms} M_{vi} v_i) \tag{14.136}$$

and

$$d'' = K_i v_i , \tag{14.137}$$

giving the overall duty cycle

$$d = d' + d'' = -R_s T_{ms} T_{pi} d - R_s T_{ms} M_{vi} v_i + K_i v_i . \tag{14.138}$$

Hence,

$$d(1 + R_s T_{ms} T_{pi}) = v_i (K_i - R_s T_{ms} M_{vi}). \tag{14.139}$$

This leads to the input voltage-to-duty cycle transfer function with K_i

$$M_{vdf}(s) \equiv \left. \frac{d(s)}{v_i(s)} \right|_{v_c = i_o = 0} = \frac{K_i - R_s T_{ms} M_{vi}}{1 + R_s T_{ms} T_{pi}} = \frac{K_i}{1 + T_i} + M_{vd} . \tag{14.140}$$

Figures 14.32 and 14.33 depicts Bode plots of M_{dvf} for $K_i = -0.04167$. The response of the duty cycle d_T to a step change in the input voltage $\Delta V_I = 1\,\text{V}$ from 12 to 13 V is shown in Figure 14.34. At $t = 0$, there is a step change in d_T from 0.5 to 0.475.

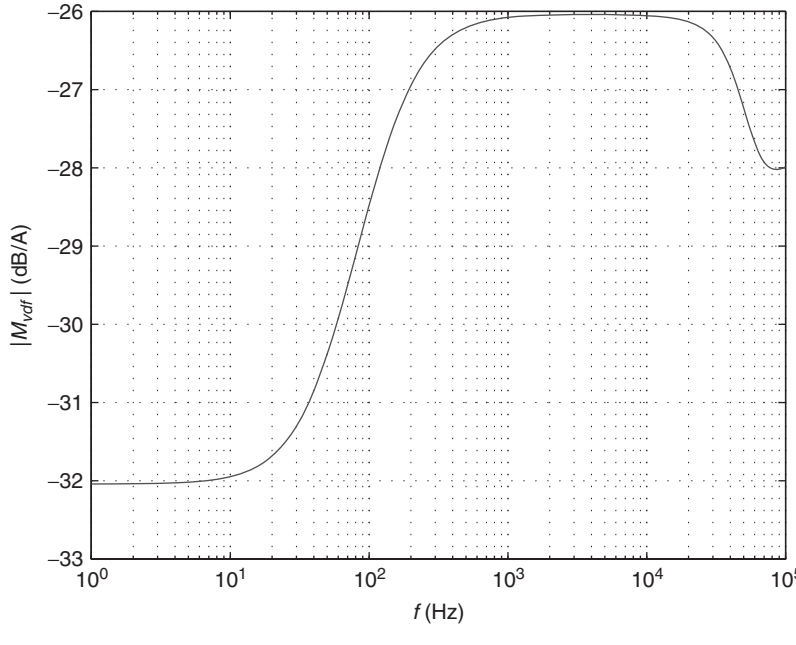


Figure 14.32 Bode plot of the magnitude of M_{vdf} for the boost converter with feedforward gain $K_i = -0.04167$.

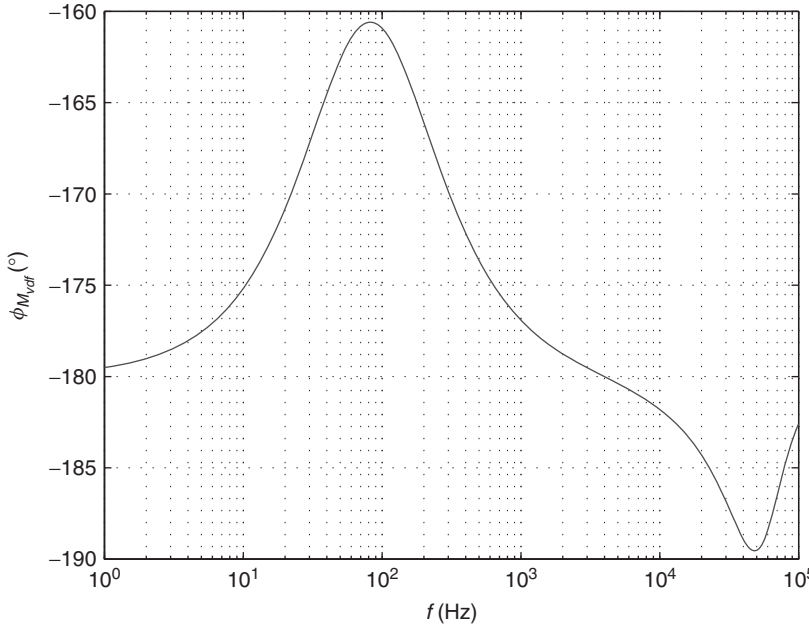


Figure 14.33 Bode plot of the phase of M_{vdf} for the boost converter with feedforward gain $K_i = -0.04167$.

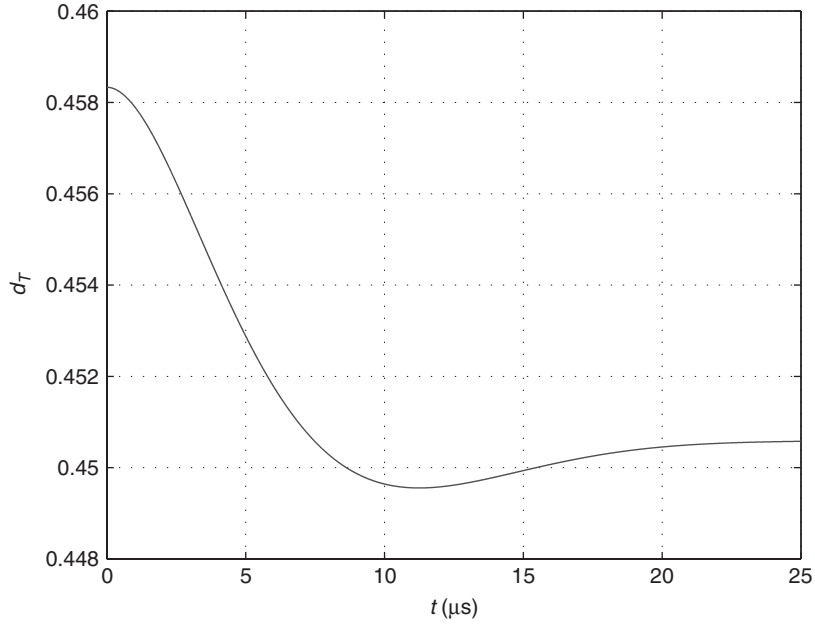


Figure 14.34 Response of d_T to a step change $\Delta V_I = 1$ V from 12 to 13 V for the boost converter with feedforward gain $K_i = -0.04167$.

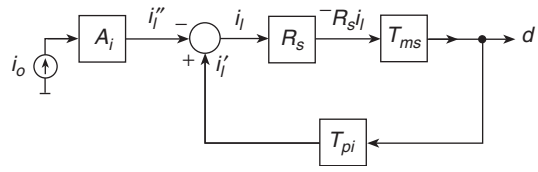


Figure 14.35 Block diagram for deriving the load current-to-duty cycle transfer function A_{id}.

14.4.2 Load Current-to-duty Cycle Transfer Function

A block diagram for deriving the input voltage-to-duty cycle transfer function M_{vd} for the closed-current loop is shown in Figure 14.35. The inductor current is determined by

$$i_l = i_l' - i_l'' = T_{pi} d - A_i i_o, \tag{14.141}$$

and the duty cycle is given by

$$d = -T_{ms} R_s i_l = -R_s T_{pi} T_{ms} d + R_s A_i T_{ms} i_o, \tag{14.142}$$

resulting in

$$d(1 + R_s T_{pi} T_{ms}) = R_s A_i T_{ms} i_o. \tag{14.143}$$

Hence, one obtains the input voltage-to-duty cycle transfer function for the current-closed loop,

$$A_{id}(s) \equiv \left.\frac{d(s)}{i_o(s)}\right|_{v_c = v_i = 0} = \frac{R_s T_{ms} A_i}{1 + T_i} = \frac{12 f_s^2 A_{ix}(s + \omega_{zn})}{T_{pix}(s + \omega_{zi1})(s^2 + \omega_{sh} s + 12 f_s^2)}. \tag{14.144}$$

For $s = 0$,

$$A_{ido} = A_{id}(0) = \frac{A_{ix}\omega_{zn}}{T_{pix}\omega_{zi1}} = \frac{(1 - D)R_L}{2V_O} = \frac{1 - 0.5}{2 \times 20} = 0.05 = -6\,\text{dB}. \tag{14.145}$$

Figures 14.36 and 14.37 show Bode plots for A_{id}. Figure 14.38 shows the response of the duty cycle d_T to a step change of the load current from 0.5 to 0.6 A. The steady-state value of the duty cycle is

$$d_T(\infty) = D(0^-) + A_{ido}\Delta I_O = 0.5 + 0.5 \times 0.1 = 0.55. \tag{14.146}$$

14.4.3 Output Impedance of Closed-current Loop

Figure 14.39 shows a block diagram for finding the output impedance of the closed-current loop with open voltage loop. The inductor current is given by

$$i_l = i_l' + i_l'' = T_{pi} d + A_i i_o, \tag{14.147}$$

and the duty cycle is

$$d = -R_s T_{ms} i_l = -R_s T_{ms} T_{pi} d - R_s T_{ms} A_i i_o. \tag{14.148}$$

Thus,

$$d(1 + R_s T_{ms} T_{pi}) d = -R_s T_{ms} A_i i_o, \tag{14.149}$$

yielding the duty cycle

$$d = -\frac{R_s T_{ms} A_i}{1 + T_i}. \tag{14.150}$$

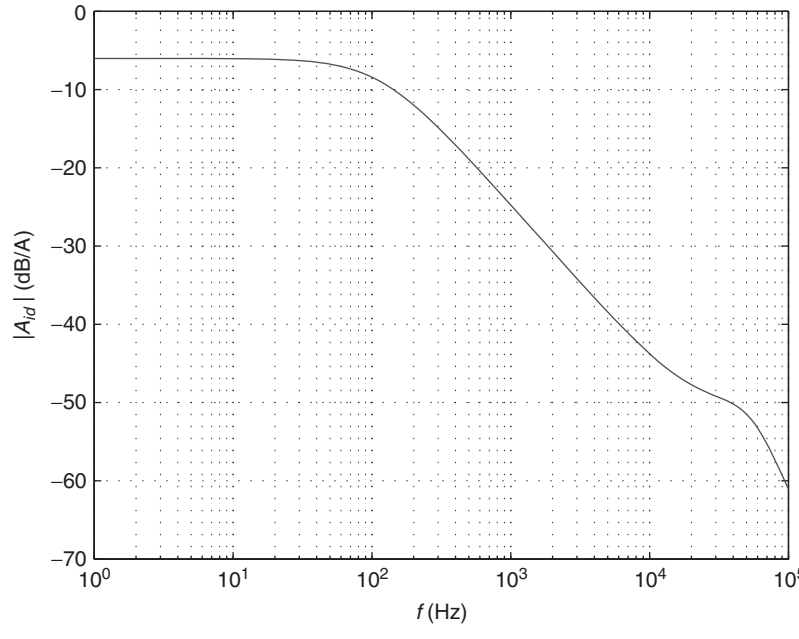


Figure 14.36 Bode plot of the magnitude of A_{id} for the boost converter.

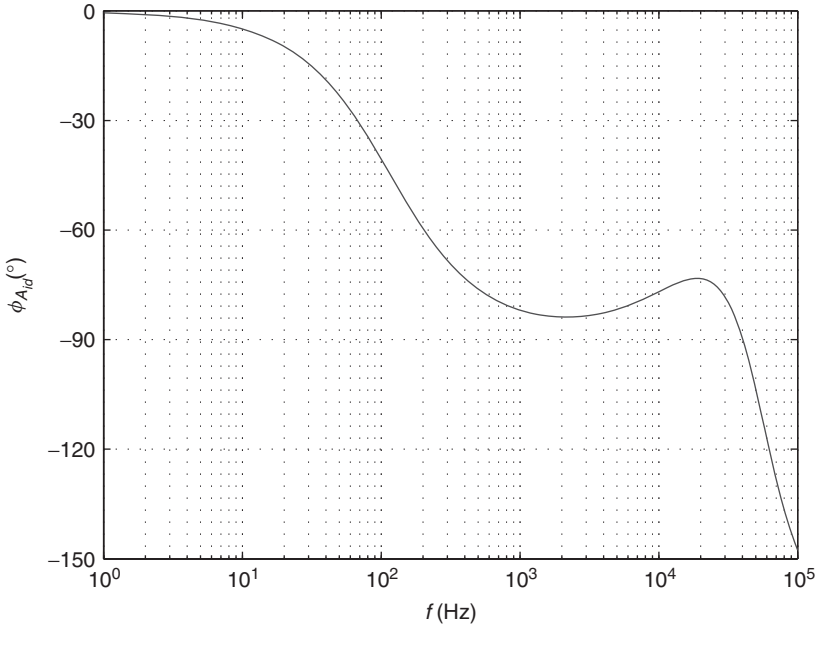


Figure 14.37 Bode plot of the phase of A_{id} for the boost converter.

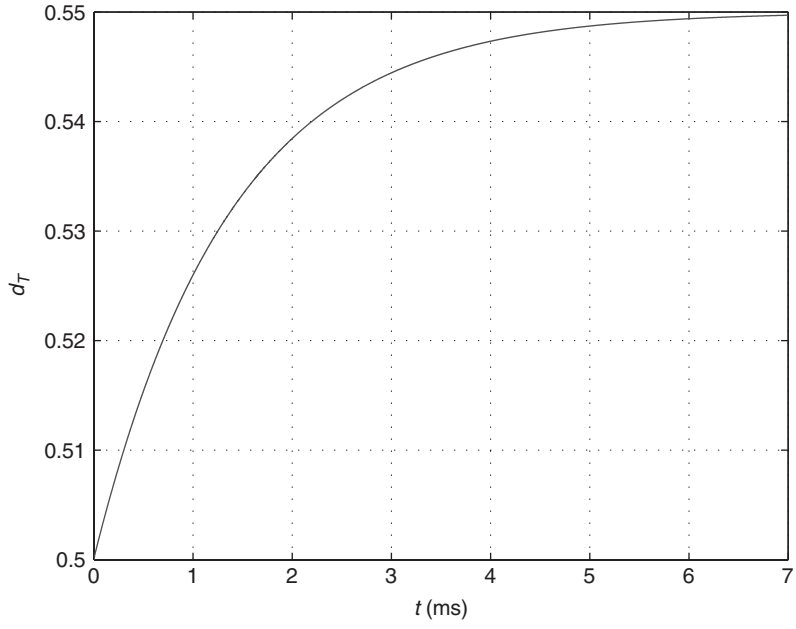


Figure 14.38 Response of d_T to a step change $\Delta I_O = 0.1\,\text{A}$ due to A_{id} for the boost converter with the current loop closed.

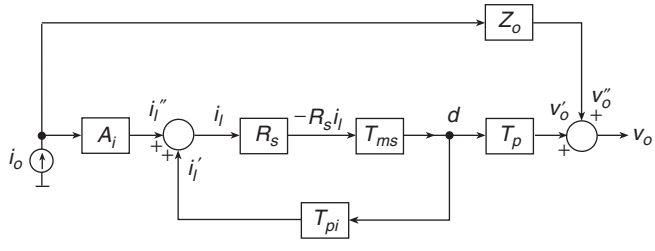


Figure 14.39 Block diagram for deriving the output impedance Z_{oi} of the closed-current loop.

The components of the output voltage are

$$v_o{}' = T_p d = -\frac{R_s T_{ms} A_i T_p}{1 + T_i} d \tag{14.151}$$

and

$$v_o{}'' = Z_o i_o, \tag{14.152}$$

resulting in the total output voltage

$$v_o = v_o{}' + v_o{}'' = -\frac{R_s T_{ms} A_i T_p}{1 + T_i} d + Z_o i_o. \tag{14.153}$$

This gives the output impedance of the closed-current loop,

$$Z_{oi} = -\frac{v_o}{i_o} = \frac{R_s T_{ms} A_i T_p}{1 + T_i} - Z_o = T_{icl} A_i T_p R_s - Z_o. \tag{14.154}$$

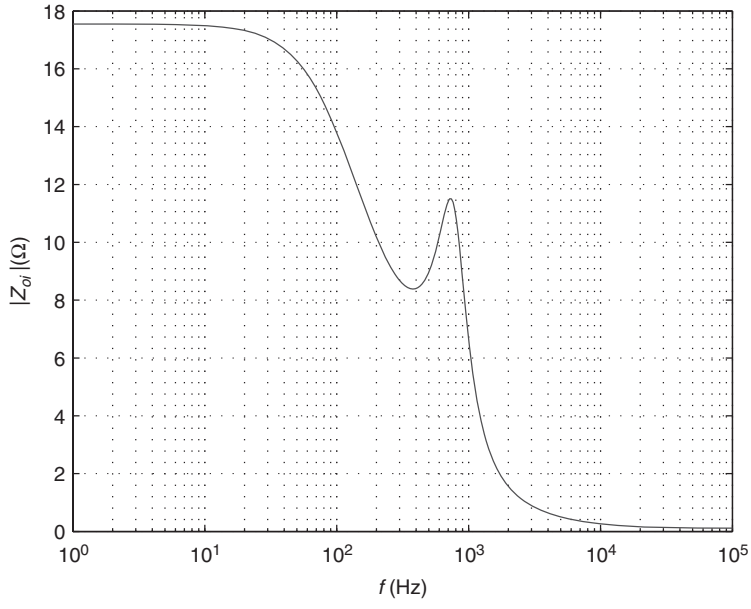


Figure 14.40 Magnitude of the output impedance Z_{oi} of the closed-current loop for the boost converter.

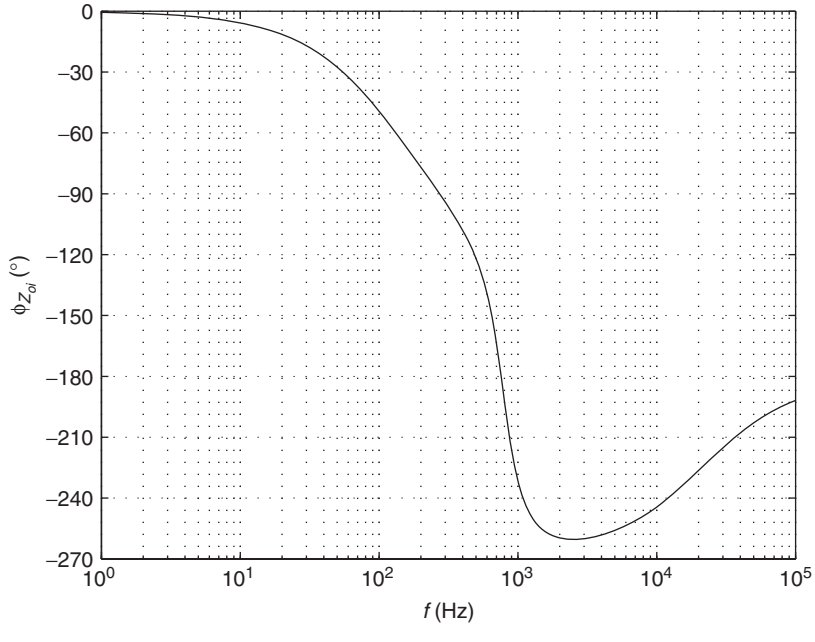


Figure 14.41 Phase of the output impedance ϕ_{Zoi} of the closed-current loop for the boost converter.

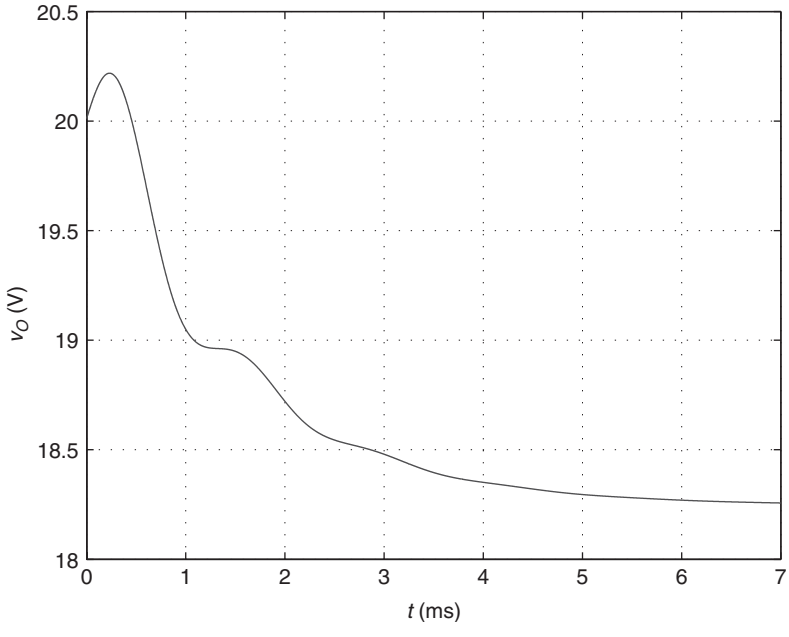


Figure 14.42 Response of v_o to a step change $\Delta I_O = 0.1\,\text{A}$ due to Z_{oi} with the current-loop closed for the boost converter.

At $s = 0$,

$$\begin{aligned} Z_{oio} = Z_{oi}(0) = R_{oi}(0) &= T_{iclo}A_{io}T_{po}R_s - Z_o(0) \\ &= \frac{R_L}{2}\frac{R_L(1-D)^2 - r}{(1-D)^2R_L + r} - \frac{R_L r}{(1-D)^2R_L + r} \\ &= \frac{R_L^2(1-D)^2 - 3rR_L}{2[(1-D)^2R_L + r]} \approx \frac{R_L}{2}. \end{aligned} \tag{14.155}$$

For example, for $D_{nom} = 0.5$ and $R_{Lmin} = 40\,\Omega$,

$$Z_{oio} = \frac{R_{Lmin}^2(1-D_{nom})^2 - 3rR_L}{2[(1-D_{nom})^2R_{Lmin} + r]} = \frac{40^2 \times (1-0.5)^2 - 3 \times 0.316 \times 40]}{2[(1-0.5)^2 \times 40 + 0.316]} = 17.6\,\Omega. \tag{14.156}$$

Figures 14.40 and 14.41 depict the magnitude and the phase of the output impedance of the closed-current loop. Figure 14.42 shows the response of the output voltage to a step change in the load current $\Delta I_O = 0.1\,\text{A}$. The output voltage reaches its steady-state value after the transition,

$$V_O(\infty) = V_O(0^-) - Z_{oio}\Delta I_O = 20 - 17.6 \times 0.1 = 18.24\,\text{V}. \tag{14.157}$$

14.5 Closed-voltage-loop Transfer Functions

14.5.1 Control Voltage-to-feedback Voltage Function

The open-loop duty cycle-to-output voltage transfer function for the boost converter is expressed by

$$T_p \equiv \frac{v_o}{d}|_{v_i=i_o=0} = T_{px}\frac{(s+\omega_{zn})(s-\omega_{zp})}{s^2+2\xi\omega_0 s+\omega_0^2}, \tag{14.158}$$

where

$$T_{px} = -\frac{V_O r_C}{(1-D)(R_L+r_C)}. \tag{14.159}$$

The product of (14.111) and (14.158) yields the control voltage-to-feedback voltage transfer function

$$\begin{aligned} T_k \equiv \frac{v_f}{v_c}|_{v_i=i_o=0} &= T_{icl}T_p\beta = \frac{12f_s^2\beta T_{px}(s+\omega_{zn})(s-\omega_{zp})}{R_s T_{pix}(s^2+\omega_{sh}s+12f_s^2)(s+\omega_{zi1})} \\ &= T_{kx}\frac{s^2+s(\omega_{zn}-\omega_{zp})-\omega_{zn}\omega_{zp}}{s^3+(\omega_{sh}+\omega_{zi1})s^2+(\omega_{sh}\omega_{zi1}+12f_s^2)s+12f_s^2\omega_{zi1}}, \end{aligned} \tag{14.160}$$

where

$$T_{kx} = \frac{12f_s^2\beta T_{px}}{R_s T_{pix}} \tag{14.161}$$

and

$$\beta = \frac{V_F}{V_O} \approx \frac{V_R}{V_O} = \frac{R_B}{R_A+R_B}. \tag{14.162}$$

For $s = 0$,

$$T_{ko} = T_k(0) = \frac{\beta T_{px} f_{zn} f_{zp}}{R_s T_{pix} f_{zi1}} = T_{iclo}T_{po}\beta. \tag{14.163}$$

Example 14.9

For the boost converter with $T_{iclo} = 0.25979\,\mathrm{V}^{-1}$, $T_{po} = 37.55\,\mathrm{V}$, $V_O = 20\,\mathrm{V}$, $V_R = 5\,\mathrm{V}$, $f_{zi1} = 116.38\,\mathrm{Hz}$, $f_0 = 783.66\,\mathrm{Hz}$, and $\xi = 0.261$, find β and T_{ko}. Draw Bode plots of T_k.

Solution. The voltage transfer function of the feedback network is

$$\beta = \frac{R_B}{R_A+R_B} = \frac{V_F}{V_O} \approx \frac{V_R}{V_O} = \frac{5}{20} = 0.25 = -12\,\mathrm{dB}. \tag{14.164}$$

Pick $R_B = 1.2\,\mathrm{k\Omega}$. Hence,

$$R_A = \left(\frac{1}{\beta}-1\right)R_B = \left(\frac{1}{0.25}-1\right)\times 1.2 = 3.6\,\mathrm{k\Omega}, \tag{14.165}$$

which gives

$$h_{11} = \frac{R_A R_B}{R_A+R_B} = \frac{1.2\times 3.6}{1.2+3.6} = 0.9\,\mathrm{k\Omega}. \tag{14.166}$$

For $f = 0$,

$$T_{ko} = T_{iclo}T_{po}\beta = 0.25979\times 37.55\times 0.25 = 2.4388 = 7.743\,\mathrm{dB}. \tag{14.167}$$

Figures 14.43 and 14.44 show Bode plots of T_k.

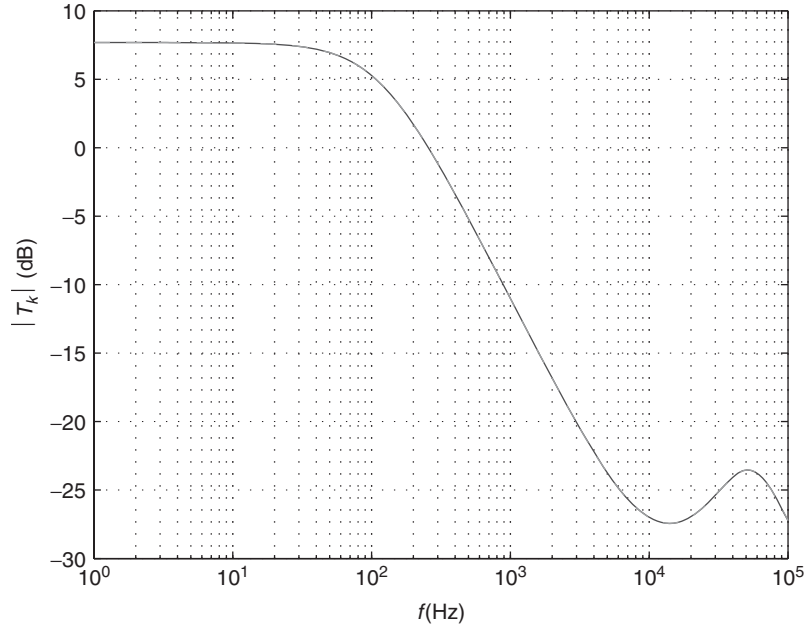


Figure 14.43 Bode plot of the magnitude of T_k for the boost converter.

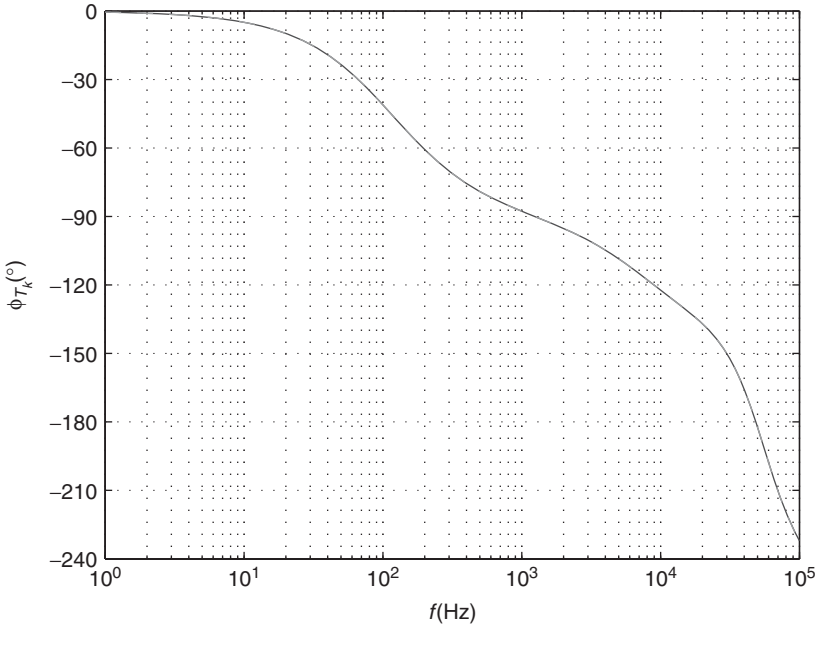


Figure 14.44 Bode plot of the phase of T_k for the boost converter.

14.5.2 Loop Gain of Voltage Loop

Consider the third-order integral-lead control circuit whose voltage transfer function is given by

$$T_c(s) = \frac{v_c}{v_e} = \frac{B(s+\omega_{zc})^2}{s(s+\omega_{pc})^2}, \tag{14.168}$$

where $B = (R_1 + R_3)/C_2[R_1R_3 + h_{11}(R_1 + R_3)]$. Hence, the loop gain of the outer voltage loop is described by

$$T \equiv \frac{v_f}{v_e}|_{v_i=i_o=0} = T_c T_{icl} T_p \beta = \frac{12f_s^2\beta T_{px} B(s+\omega_{zc})^2(s+\omega_{zn})(s-\omega_{zp})}{R_s T_{pix} s(s+\omega_{pc})^2(s^2+\omega_{sh}s+12f_s^2)(s+\omega_{zi1})}, \tag{14.169}$$

where

$$T_x = BT_{kx} = \frac{12f_s^2 B\beta T_{px}}{R_s T_{pix}} = \frac{12f_s^2 B\beta L r_C}{R_s(1-D)(R_L+2r_C)}. \tag{14.170}$$

Example 14.10

Design a controller for the boost converter such that the phase margin $PM \geq 60^\circ$ and the gain margin $GM \geq 10\,\text{dB}$. At $D_{nom} = 0.5$ and $R_{Lmin} = 40\,\Omega$, the converter has $\xi = 0.261$, $f_{zn} = 21.26\,\text{kHz}$, $f_{zp} = 9.88\,\text{kHz}$, $f_{zi1} = 116.38\,\text{Hz}$, and $f_0 = 783.66\,\text{Hz}$.

Solution. A third-order integral-lead control circuit (type III) will be used to compensate the voltage loop. Assume that $f_c = f_m = 3\,\text{kHz}$. From Bode plots of T_k, the phase of T_k at $f = f_c$, $D = D_{nom} = 0.5$, and $R_{Lmin} = 40\,\Omega$ is $\phi_{Tk}(f_c) = -100^\circ$.
Thus,

$$\phi_m = PM - \phi_{Tk}(f_c) - 90^\circ = 60^\circ - (-100^\circ) - 90^\circ = 70^\circ. \tag{14.171}$$

Hence, the K factor is calculated as

$$K = \tan^2\left(\frac{\phi_m}{4} + 45^\circ\right) = \tan^2\left(\frac{70^\circ}{4} + 45^\circ\right) = 3.69. \tag{14.172}$$

The frequencies of the zeros and poles of the control circuit using the K value are

$$f_{zc} = \frac{f_c}{\sqrt{K}} = \frac{3000}{\sqrt{3.69}} = 1.561\,\text{kHz} \tag{14.173}$$

and

$$f_{pc} = f_c\sqrt{K} = 3000\sqrt{3.69} = 5.7629\,\text{kHz}. \tag{14.174}$$

From Bode plots of T_k, $|T_k(f_c)| = -20\,\text{dB} = 0.1$. Hence,

$$|T_c(f_c)| = \frac{1}{|T_k(f_c)|} = \frac{1}{0.1} = 10 = 20\,\text{dB}. \tag{14.175}$$

Hence,

$$B = \omega_c K|T_c(f_c)| = 2\pi \times 3000 \times 3.69 \times 10 = 695.55 \times 10^3\,(\text{rad/s}). \tag{14.176}$$

Bode plots of the magnitude $|T_c|$ and the phase shift ϕ_{Tc} of the designed controller are shown in Figures 14.45 and 14.46.

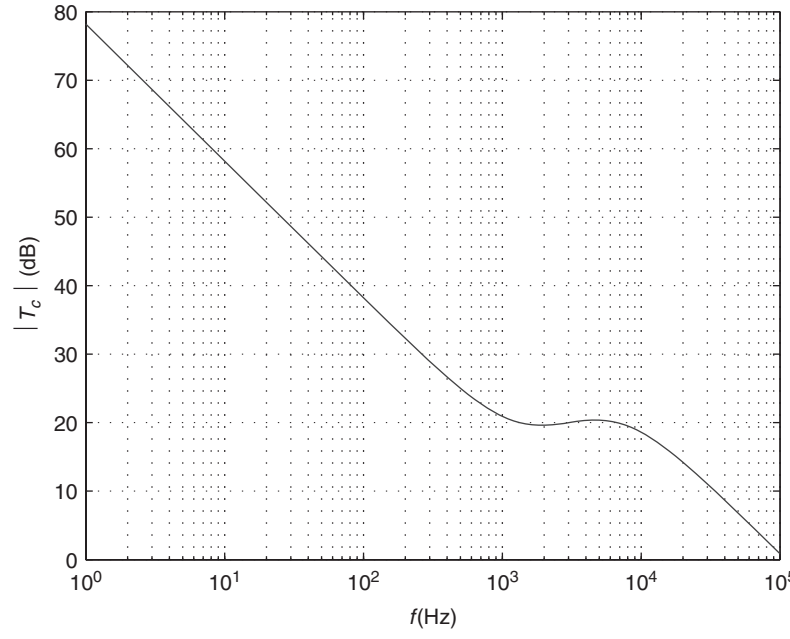


Figure 14.45 Bode plot of the magnitude of the third-order integral-lead controller (type III) voltage transfer function T_c.

Assuming $R_1 = 100\,\text{k}\Omega$,

$$C_2 = \frac{|T_k(f_c)|}{\omega_c(R_1 + h_{11})} = \frac{0.1}{2 \times \pi \times 3 \times 10^3 \times (100 + 0.9) \times 10^3} = 52.58\,\text{pF}. \tag{14.177}$$

Pick $C_2 = 56\,\text{pF}$. Then,

$$R_3 = \frac{R_1[R_1 - h_{11}(K-1)]}{(K-1)(R_1 + h_{11})} = \frac{100 \times [100 - 0.9 \times (3.69 - 1)]}{(3.69 - 1)(100 + 0.9)} = 35.95\,\text{k}\Omega. \tag{14.178}$$

Pick $R_3 = 36\,\text{k}\Omega$. Then,

$$C_1 = C_2(K - 1) = 56 \times (3.69 - 1) = 150.65\,\text{pF}. \tag{14.179}$$

Pick $C_1 = 150\,\text{pF}$. Next,

$$R_2 = \frac{\sqrt{K}}{\omega_c C_1} = \frac{\sqrt{3.69}}{2 \times \pi \times 3 \times 10^3 \times 150 \times 10^{-12}} = 679.4\,\text{k}\Omega \tag{14.180}$$

and

$$\begin{aligned} C_3 &= \frac{R_1 + h_{11}}{\sqrt{K}\omega_c[R_1R_3 + h_{11}(R_1 + R_3)]} \\ &= \frac{(100 + 0.9) \times 10^3}{\sqrt{3.69} \times 2 \times \pi \times 3 \times 10^3 \times [100 \times 36 + 0.9048 \times (100 + 36)] \times 10^6} \\ &= 0.7486\,\text{nF}. \end{aligned} \tag{14.181}$$

Pick $R_2 = 680\,\text{k}\Omega$ and $C_3 = 0.75\,\text{nF}$.

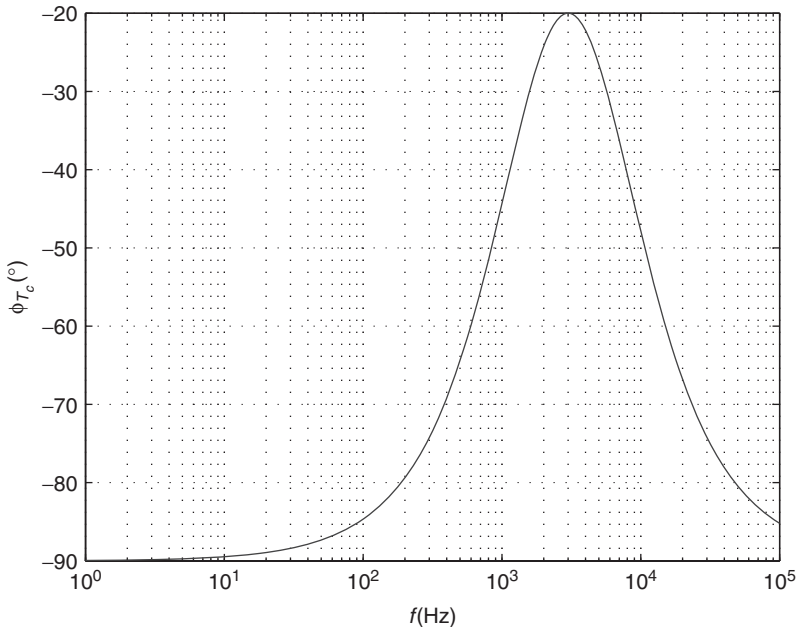


Figure 14.46 Bode plot of the phase of the third-order integral-lead controller (type III) voltage transfer function T_c.

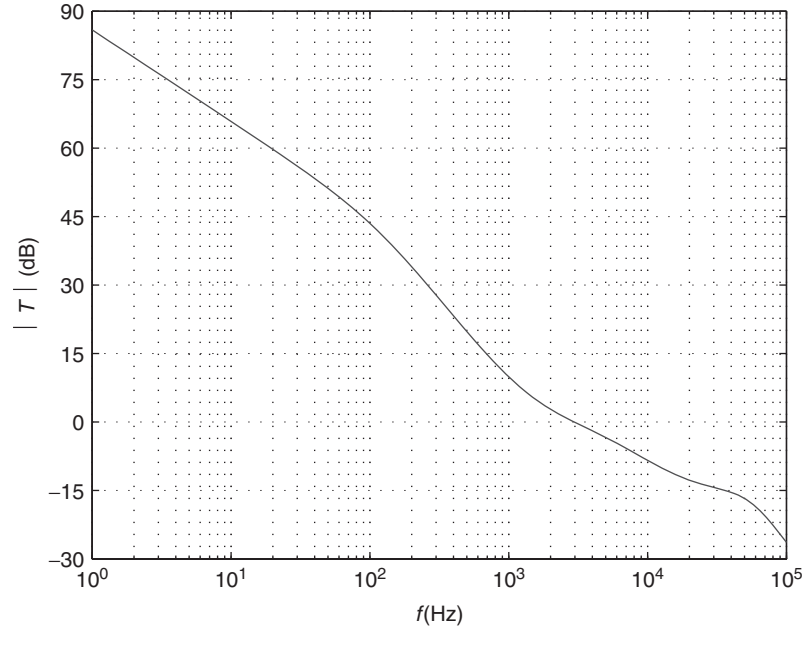


Figure 14.47 Bode plot of the magnitude of the loop gain of the voltage loop T for the boost converter with an integral-lead controller (type III).

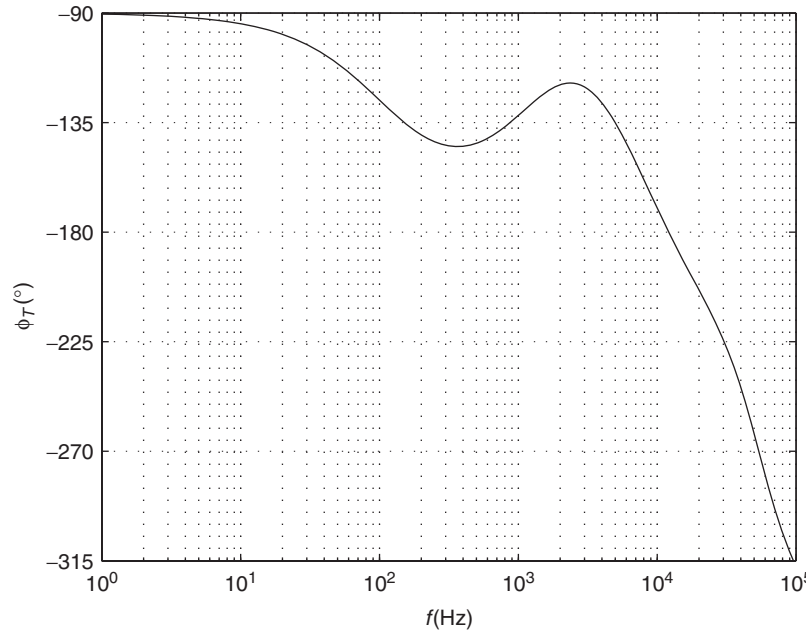


Figure 14.48 Bode plot of the phase of the loop gain of the voltage loop T for the boost converter with an integral-lead controller (type III).

The frequencies of the zeros and poles of the control circuit with the standard component values are

$$f_{zc1} = \frac{1}{2\pi R_2 C_1} = \frac{1}{2 \times \pi \times 680 \times 10^3 \times 150 \times 10^{-12}} = 1.56\,\text{kHz} \tag{14.182}$$

$$f_{zc2} = \frac{1}{2\pi C_3(R_1 + R_3)} = \frac{1}{2 \times \pi \times 0.75 \times 10^{-9}(100 + 36) \times 10^3} = 1.56\,\text{kHz} \tag{14.183}$$

$$f_{pc1} = f_{zc1}\left(\frac{C_1}{C_2} + 1\right) = 1.56\left(\frac{150}{56} + 1\right) = 5.739\,\text{kHz} \tag{14.184}$$

and

$$f_{pc2} = \frac{R_1 + h_{11}}{2\pi C_3[R_1 R_3 + h_{11}(R_1 + R_3)]}$$

$$= \frac{(100 + 0.9) \times 10^3}{2 \times \pi \times 0.75 \times 10^{-9}[100 \times 36 + 0.9(100 + 36)] \times 10^6} = 5.752\,\text{kHz}. \tag{14.185}$$

Figures 14.47 and 14.48 show Bode plots of T, from which $f_c = 3\,\text{kHz}$, $f_{-180} = 12\,\text{kHz}$, $GM = 10\,\text{dB}$, and $PM = 60^\circ$.

14.5.3 Closed-loop Gain of Voltage Loop

The closed-loop gain of the voltage loop with an integral-lead control circuit is given by

$$T_{cl} \equiv \frac{v_o}{v_r}|_{v_i = i_o = 0} = \frac{T_c T_{icl} T_p}{1 + T}. \tag{14.186}$$

Example 14.11

For the boost converter with $T_{iclo} = 0.25979\,\text{V}^{-1}$, $T_{po} = 37.55\,\text{V}$, $V_O = 20\,\text{V}$, $V_R = 5\,\text{V}$, $\beta = 0.25$, $f_{zi1} = 116.38\,\text{Hz}$, $f_0 = 783.66\,\text{Hz}$, and $\xi = 0.261$, find T_{clo} and draw Bode plots

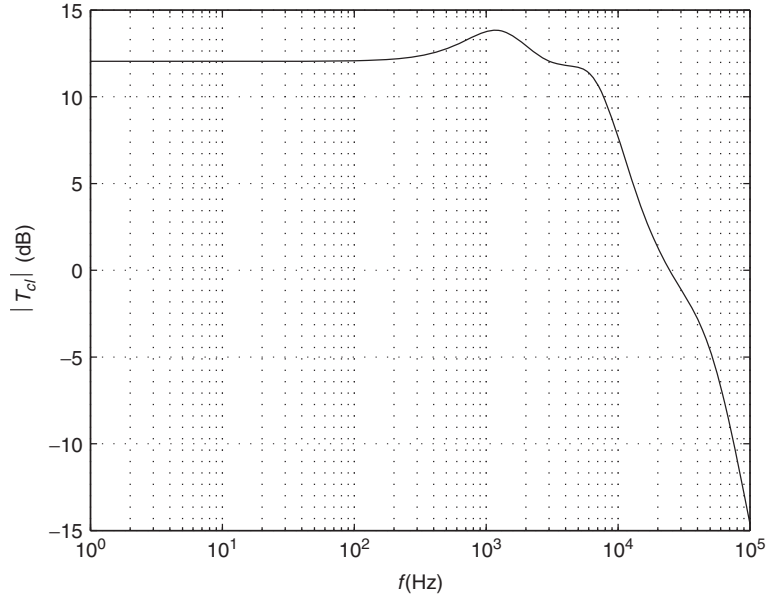


Figure 14.49 Bode plot of the magnitude of the closed-loop gain of the voltage loop T_{cl} for the boost converter with an integral-lead controller.

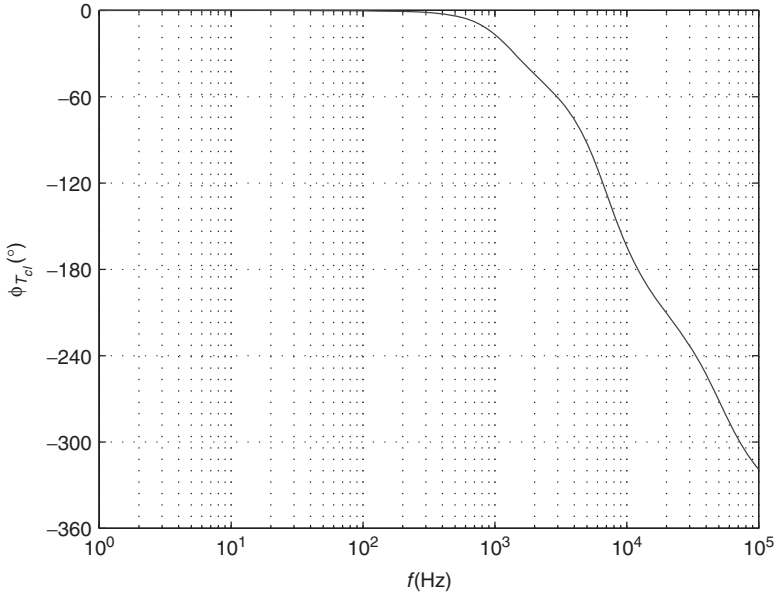


Figure 14.50 Bode plot of the phase of the closed-loop gain of the voltage loop T_{cl} for the boost converter with an integral-lead controller.

of T_{cl} for the boost converter with an integral-lead controller.

Solution. The low-frequency gain of the closed voltage loop is

$$T_{clo} \approx \frac{1}{\beta} = \frac{1}{0.25} = 4 = 12\,\text{dB}. \tag{14.187}$$

Figures 14.49 and 14.50 show Bode plots of T_{cl}. The bandwidth of the closed-loop converter is $BW = 8.5\,\text{kHz}$.

14.5.4 Closed-loop Audio Susceptibility with Integral Controller

The open-loop audio susceptibility of the boost converter is

$$M_v \equiv \frac{v_o}{v_i}|_{d=i_o=0} = M_{vx}\frac{s+\omega_{zn}}{s^2+2\xi\omega_0 s+\omega_0^2}, \tag{14.188}$$

where

$$M_{vx} = -\frac{(1-D)DR_L r_C}{L(R_L+r_C)}. \tag{14.189}$$

The closed-loop audio susceptibility is

$$M_{vcl} \equiv \frac{v_o}{v_i}|_{v_r=i_o=0} = \frac{M_v + T_i M_v - R_s T_{ms} T_p M_{vi}}{1+T_i+T_v} = \frac{M_v + T_i\left(M_v - \dfrac{M_{vi}T_p}{T_{pi}}\right)}{1+T_i+T_v}$$
$$= \frac{M_v + T_i T_p\left(\dfrac{M_v}{T_p} - \dfrac{M_{vi}}{T_{pi}}\right)}{1+T_i+T_v}, \tag{14.190}$$

where

$$T_v = T_c T_{ms} T_p \beta. \tag{14.191}$$

For the integral-lead controller,

$$T_v = T_{vx}\frac{(s+\omega_{zc})(s+\omega_{zn})(s-\omega_{zp})}{s^2(s+\omega_{pc})(s+\omega_{sh})(s+\omega_{zi1})} \tag{14.192}$$

where

$$T_{vx} = B\beta T_{msx} T_{px} = -\frac{12 f_s^2 \beta B V_O r_C}{R_s T_{pix}(1-D)(R_L+r_C)} = -\frac{12 f_s^2 \beta B r_C L}{R_s(R_L+2r_C)}. \tag{14.193}$$

It is interesting to note that $T = T_v/(1+T_i)$.

The ratios of the transfer functions for the boost converter are

$$\frac{M_v}{T_p} = -\frac{D(1-D)^2 R_L}{LV_O(s-\omega_{zp})} \tag{14.194}$$

and

$$\frac{M_{vi}}{T_{pi}} = \frac{M_{vix}}{T_{pix}}\frac{s+\omega_{zi2}}{s+\omega_{zi1}} = \frac{M_{vx}}{T_{px}(s-\omega_{zp})} = \frac{D^2(R_L+r_C)}{V_O[R_L+(1+D)r_C]}\frac{s+\omega_{zi2}}{s+\omega_{zi1}}. \tag{14.195}$$

Example 14.12

For the boost converter with $T_{iclo} = 0.25979\,\text{V}^{-1}$, $T_{po} = 37.55\,\text{V}$, $V_O = 20\,\text{V}$, $V_R = 5\,\text{V}$, $\beta = 0.25, f_{zi1} = 116.38\,\text{Hz}, f_0 = 783.66\,\text{Hz}$, and $\xi = 0.261$, draw Bode plots of T_v and M_{vcl}.

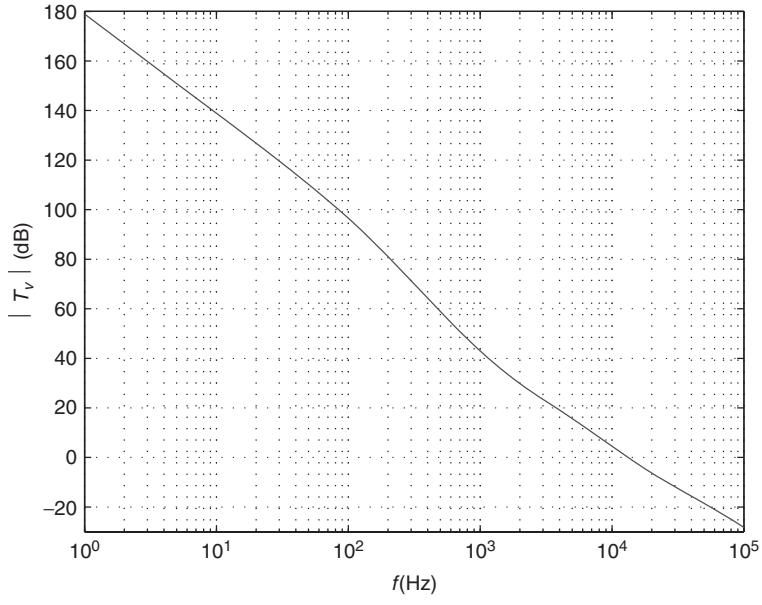


Figure 14.51 Bode plot of the magnitude of T_v for the boost converter with an integral-lead controller.

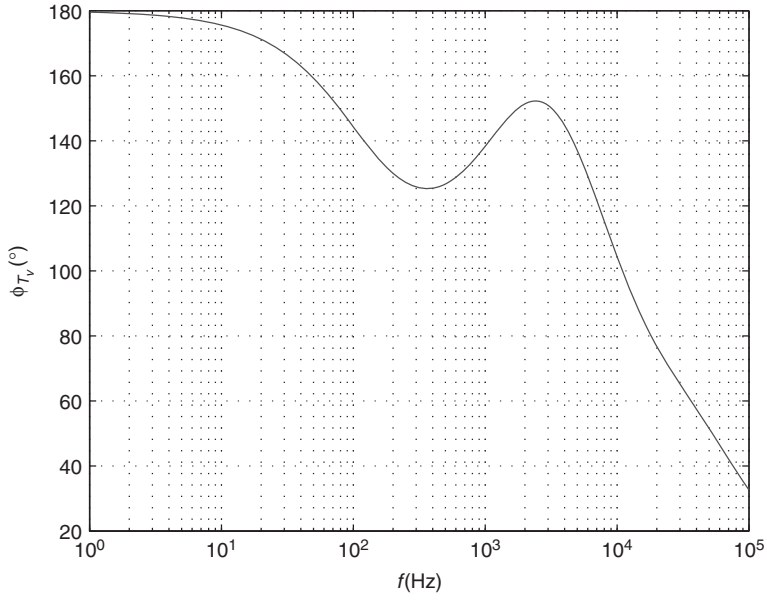


Figure 14.52 Bode plot of the phase of T_v for the boost converter with an integral-lead controller.

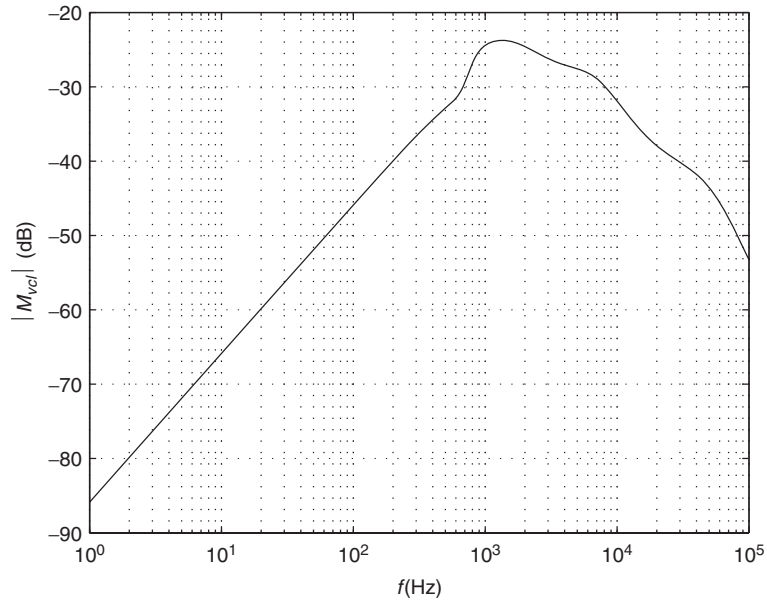


Figure 14.53 Bode plot of the magnitude of the closed-loop audio susceptibility M_{vcl} for the boost converter with an integral-lead controller.

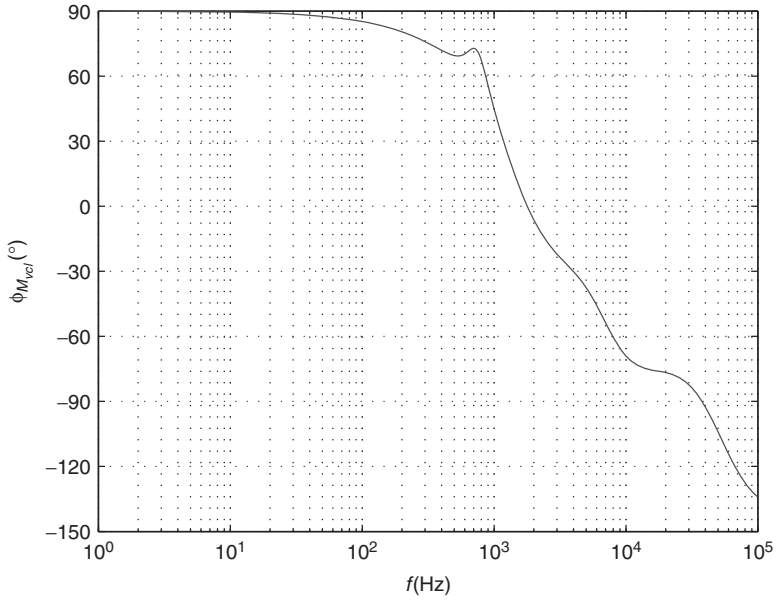


Figure 14.54 Bode plot of the phase of the closed-loop audio susceptibility M_{vcl} for the boost converter with an integral-lead controller.

Solution. Figures 14.51 and 14.52 depict Bode plots of T_v. Figures 14.53 and 14.54 show Bode plots of M_{vcl}.

14.5.5 Closed-loop Output Impedance with Integral Controller

The open-loop output impedance of the boost converter is

$$Z_o(s) \equiv \frac{v(s)}{i(s)}|_{d(s)=0 \text{ and } v_i(s)=0} = Z_{ox}\frac{(s+\omega_{zn})(s+\omega_{rl})}{s^2+2\xi\omega_0 s+\omega_0^2}, \tag{14.196}$$

where $\omega_{rl} = r/L$ and

$$Z_{ox} = \frac{R_L r_C}{R_L + r_C}. \tag{14.197}$$

The closed-loop output impedance is

$$Z_{ocl} \equiv \frac{v_t}{i_t}|_{v_r=i_o=0} = \frac{Z_o(1+T_i)+R_s T_{ms} A_i T_p}{1+T_v+T_i}. \tag{14.198}$$

Example 14.13

For the boost converter with $T_{iclo} = 0.25979\,\text{V}^{-1}$, $T_{po} = 37.55\,\text{V}$, $V_O = 20\,\text{V}$, $V_R = 5\,\text{V}$, $\beta = 0.25$, $f_{zi1} = 116.38\,\text{Hz}$, $f_0 = 783.66\,\text{Hz}$, and $\xi = 0.621$, draw plots of Z_{ocl} versus frequency.

Solution. Figures 14.55 and 14.56 show plots of Z_{ocl}. The magnitude of the closed-loop output impedance $|Z_{ocl}|$ is very low at low frequencies. However, at higher frequencies, $|Z_{ocl}|$ reaches quite high values.

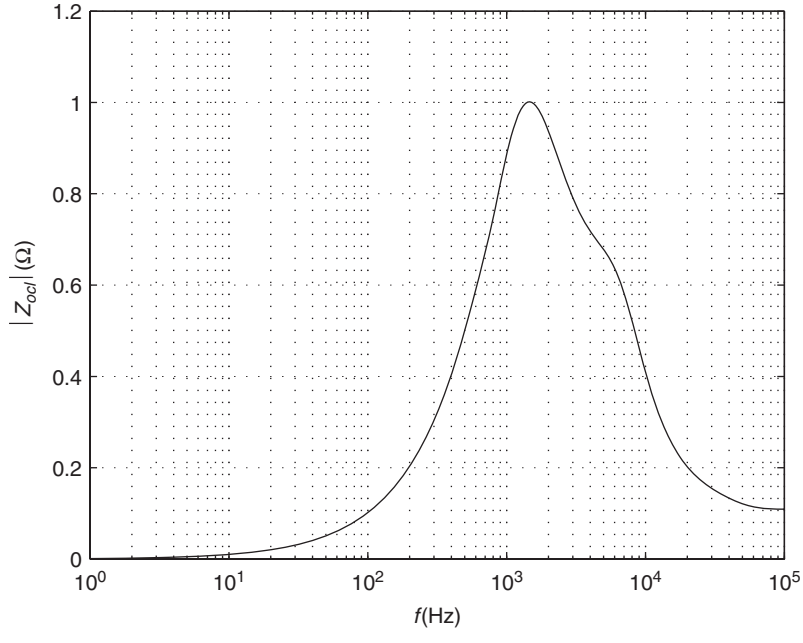


Figure 14.55 The magnitude of the closed-loop output impedance Z_{ocl} for the boost converter with an integral-lead controller.

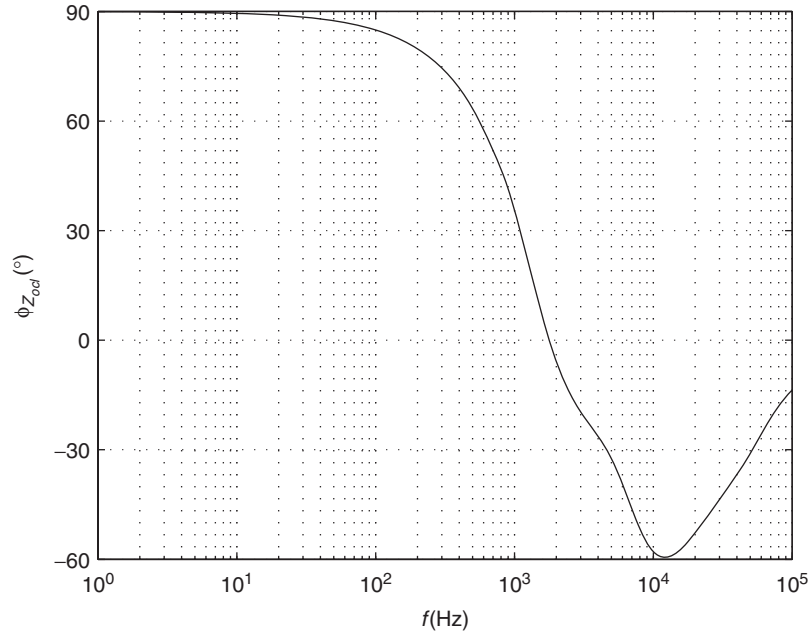


Figure 14.56 The phase of the closed-loop output impedance Z_{ocl} for the boost converter with an integral-lead controller.

14.6 Closed-loop Step Responses

14.6.1 Closed-loop Response of Output Voltage to Step Change in Input Voltage

Figure 14.57 shows the closed-loop response of v_O to a step change in the input voltage v_I from 12 to 13 V. The total output voltage v_O increases from 20 V to a maximum value of 20.043 V, and returns to a steady-state value of 20 V after 3 ms. It can be seen that negative feedback reduces the disturbance effect to nearly zero for steady state. The maximum relative transient ripple of the output voltage is

$$\delta_{max} = \frac{v_{Omax} - V_O(\infty)}{V_O(\infty)} = \frac{20.043 - 20}{20} = 0.215\,\%. \tag{14.199}$$

14.6.2 Closed-loop Response of Output Voltage to Step Change in Load Current

Figure 14.58 shows the closed-loop response of v_O to a step change in the load current $\Delta I_O = 0.25$ A from 1 to 1.25 A. The output voltage decreases from 20 V to 19.82 V, and reaches a steady-state value of 20 V after 5 ms. Thus, the effect of a step change in the load

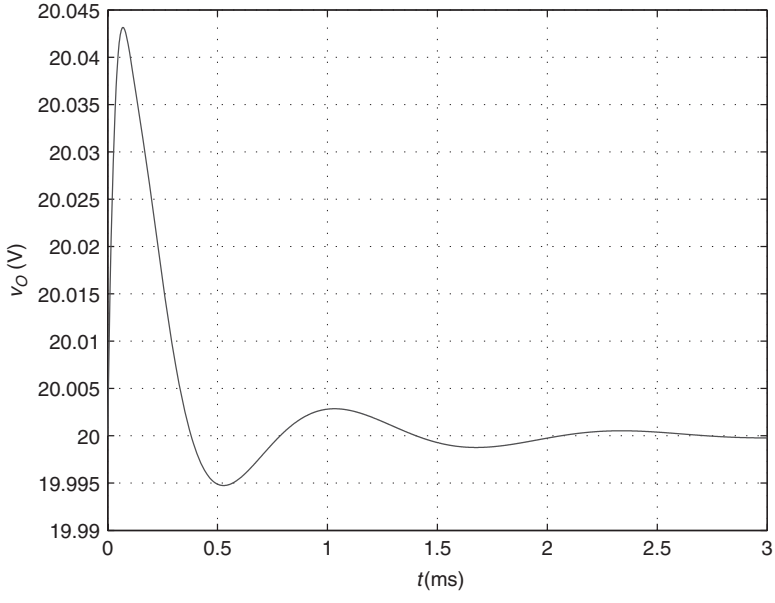


Figure 14.57 Closed-loop response of v_O to a step change in the input voltage v_I from 12 to 13 V for the boost converter with an integral-lead controller at $a = 0.1716$, $R_s = 1\,\Omega$, $V_O = 20\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $r = 0.316\,\Omega$, $f_{zi1} = 116.38\,\text{Hz}$, $f_0 = 783.66\,\text{Hz}$, $\xi = 0.261$, and $\beta = 0.25$ for $D_{nom} = 0.5$.

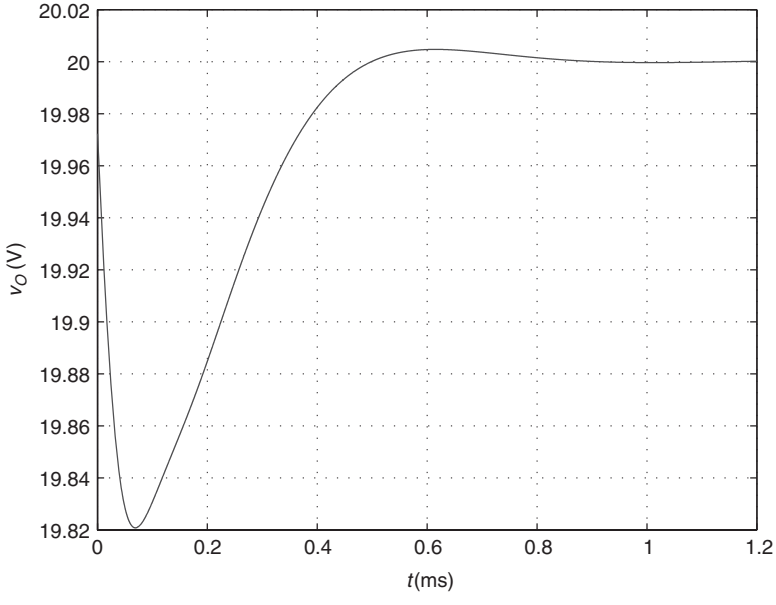


Figure 14.58 Closed-loop response of v_O to a step change in the load current $\Delta I_O = 0.25\,\text{A}$ from 1 to 1.25 A for the boost converter with an integral-lead controller at $a = 0.1716$, $R_s = 1\,\Omega$, $V_O = 20\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $r = 0.316\,\Omega$, $f_{zi1} = 116.38\,\text{Hz}$, $f_0 = 783.66\,\text{Hz}$, $\xi = 0.261$, and $\beta = 0.25$ for $D_{nom} = 0.5$.

current on the steady-state output voltage is nearly zero. The maximum relative transient ripple of the output voltage

$$\delta_{max} = \frac{|v_{omin} - v_o(\infty)|}{V_O(\infty)} = \frac{|19.82 - 20|}{20} = 0.9\,\%. \tag{14.200}$$

14.6.3 Closed-loop Response of Output Voltage to Step Change in Reference Voltage

Figure 14.59 shows the closed-loop response of v_O to a step change in the reference voltage V_R from 5 to 6 V. The output voltage v_O increases from 20 V to a maximum value of 24.54 V, and approaches a steady-state value of 24 V after 0.8 ms. The steady-state value of the transient component is

$$v_o(\infty) = T_{clo}\Delta V_R = 4 \times 1 = 4\,\text{V}, \tag{14.201}$$

yielding the steady-state value of the total output voltage,

$$V_O(\infty) = V_O(0^-) + v_o(\infty) = 20 + 4 = 24\,\text{V}. \tag{14.202}$$

The maximum overshoot of the transient component is

$$S_{max} = \frac{v_{omax} - v_o(\infty)}{v_o(\infty)} = \frac{0.54 - 0}{4} = 13.5\,\%, \tag{14.203}$$

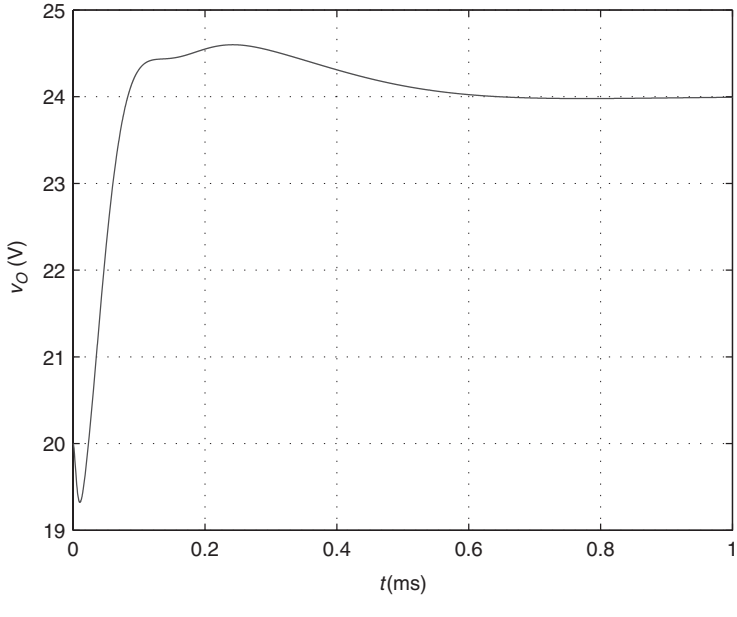


Figure 14.59 Closed-loop response of v_O to a step change in the reference voltage V_R from 5 to 6 V for the boost converter with an integral-lead controller at $a = 0.1716$, $R_s = 1\,\Omega$, $V_O = 20\,\text{V}$, $V_{Inom} = 12\,\text{V}$, $R_{Lmin} = 40\,\Omega$, $r_{DS} = 0.18\,\Omega$, $R_F = 0.072\,\Omega$, $L = 156\,\mu\text{H}$, $r_L = 0.19\,\Omega$, $C = 68\,\mu\text{F}$, $r_C = 0.111\,\Omega$, $r = 0.316\,\Omega$, $f_{zi1} = 116.38\,\text{Hz}$, $f_0 = 873.66\,\text{Hz}$, $\xi = 0.261$, and $\beta = 0.25$ for $D_{nom} = 0.5$.

resulting in the maximum relative transient ripple of the output voltage

$$\delta_{max} = \frac{v_{omax} - v_o(\infty)}{V_O(\infty)} = \frac{5.54 - 4}{24} = 2.25\,\%. \tag{14.204}$$

14.7 Closed-loop DC Transfer Functions

The dc voltage transfer function of the outer loop forward path is given by

$$A_o = A(0) = \frac{V_O}{V_E} = T_{co} T_{iclo} T_{po}, \tag{14.205}$$

and the dc loop gain of the outer loop is

$$T_o = T(0) = \frac{V_F}{V_E} = \beta A_o = \beta T_{co} T_{iclo} T_{po}. \tag{14.206}$$

The dc closed-loop gain of the outer loop is

$$T_{clo} = T_{cl}(0) = \frac{V_O}{V_R} = \frac{A_o}{1 + \beta A_o} \approx \frac{1}{\beta}. \tag{14.207}$$

The dc closed-loop audio susceptibility is

$$M_{vclo} = \frac{M_{vo} + T_{io} T_{po} \left(\dfrac{M_{vo}}{T_{po}} - \dfrac{M_{vio}}{T_{pio}} \right)}{1 + T_{vo} + T_{io}}, \tag{14.208}$$

and the dc closed-loop output impedance is

$$Z_{oclo} = \frac{Z_o(1 + T_{io} + R_s T_m H_{sh} A_{io} T_{po})}{1 + T_{vo} + T_{io}}. \tag{14.209}$$

Example 14.14

For the boost converter with $T_{co} = 1000$, $T_{iclo} = 0.25979\,\text{V}^{-1}$, $T_{po} = 37.55\,\text{V}$, $\beta = 0.25$, $M_{vo} = 1.939$, $Z_{oo} = 1.225\,\Omega$, $R_s = 0.1\,\Omega$, $A_{io} = 1.939$, $T_{pio} = 3.8775\,\text{A}$, $M_{vio} = 0.09694$ A/V, $V_O = 20\,\text{V}$, and $V_R = 5\,\text{V}$. Find T_{clo}, M_{vclo}, Z_{oclo}, V_O, and V_E.

Solution. Assuming that the dc voltage transfer function of the control circuit is $T_{co} = 1000$, the dc voltage transfer function of the outer loop forward path is given by

$$A_o = A(0) = \frac{V_O}{V_E} = T_{co} T_{iclo} T_{po} = 1000 \times 0.25979 \times 37.55 = 9755.1, \tag{14.210}$$

and the dc loop gain of the outer loop

$$T_o = T(0) = \frac{V_F}{V_E} = \beta A_o = \beta T_{co} T_{iclo} T_{po} = 0.25 \times 9755.1 = 2438.775. \tag{14.211}$$

The dc closed-loop gain of the outer loop is

$$T_{clo} = T_{cl}(0) = \frac{V_O}{V_R} = \frac{A_o}{1 + \beta A_o} = \frac{9755.1}{1 + 2438.775} = 3.999836. \tag{14.212}$$

Hence, the output, feedback, and error voltages are

$$V_O = T_{clo} V_R = 3.999836 \times 5 = 19.99918\,\text{V}, \tag{14.213}$$

$$V_F = \beta V_O = 0.25 \times 19.99918 = 4.99795\,\text{V}, \tag{14.214}$$

and

$$V_E = V_R - V_F = 5 - 4.99795 = 2.05\,\text{mV}. \tag{14.215}$$

Next,

$$T_{vo} = T_{co} T_{mso} T_{po} \beta = \infty. \tag{14.216}$$

The dc closed-loop audio susceptibility is

$$M_{vclo} = \frac{M_{vo} + T_{io} T_{po} \left(\dfrac{M_{vo}}{T_{po}} - \dfrac{M_{vio}}{T_{pio}} \right)}{1 + T_{vo} + T_{io}} = 0 \tag{14.217}$$

and the dc closed-loop output impedance is

$$Z_{oclo} = \frac{Z_{oo}(1 + T_{io}) + R_s T_{ms} A_i T_{po}}{1 + T_{vo} + T_{io}} = 0. \tag{14.218}$$

14.8 Summary

- The small-signal model of the boost converter for current-mode control has two inputs: the small-signal duty cycle d and the small-signal input voltage v_i. The small-signal duty cycle d is a control variable and the small-signal input voltage v_i is a disturbance.
- The small-signal model of the boost converter has one output, which is the small-signal component of the inductor current i_l.
- The open-loop duty cycle-to-inductor current transfer function T_{pi} of the boost converter is a second-order low-pass function with two poles and one zero.
- The zero of the open-loop duty cycle-to-inductor current transfer function T_{pi} is located in the LHP.
- The frequency of the zero of the open-loop duty cycle-to-inductor current transfer function T_{pi} is lower than the corner frequency f_0.
- The minimum value of the phase of the open-loop duty cycle-to-inductor current transfer function ϕ_{Tpi} is -90°.
- In boost and most isolated converters, the simplest way of implementing the switch current sensing is by adding a resistor in series with the MOSFET source. However, this causes additional power loss and requires a transistor with a larger current capability or a higher gate-to-source voltage [14].

14.9 References

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14.10 Review Questions

14.1 Draw a small-signal model for deriving the duty cycle-to-inductor current transfer function T_{pi} of the boost converter for CCM.

14.2 How many zeros does the transfer function T_{pi} have?

14.3 Where is the zero of T_{pi} located?

14.4 How does the value of the zero frequency of T_{pi} compare to the corner frequency f_0?

14.5 What is the minimum value of the phase ϕ_{Tpi}?

14.6 What can you say about the stability of the current loop?

14.11 Problems

14.1 The boost converter designed in Chapter 3 has $V_{Inom} = 156\,\text{V}$, $V_O = 400\,\text{V}$, $D_{nom} = 0.65$, $R_{Lmin} = 1.778\,\text{k}\Omega$, $r_{DS} = 1\,\Omega$, $V_F = 1.4\,\text{V}$, $R_F = 0.0171\,\Omega$, $L = 30\,\text{mH}$, $r_L = 2.1\,\Omega$, $C = 1\,\mu\text{F}$, and $r_C = 1\,\Omega$. Determine z_{i1} and f_{zi1}.

14.2 For the boost converter of Problem 14.1, determine T_{pio} and T_{pix}.

14.3 For the boost converter of Problem 14.1, determine M_{vio} and f_{zi2}.

14.4 For the boost converter of Problem 14.1, determine A_{io} and f_{zn}.

15

Silicon and Silicon Carbide Power Diodes

15.1 Introduction

Power diodes [1]–[14] play an important role in power electronics. In this chapter, we will study silicon and silicon carbide pn junction bipolar and Schottky power diodes. We will describe the physical structure of the diodes, explain the principle of operation, present the dc $I-V$ characteristic, analyze the breakdown voltage, describe the diode capacitances, consider the switching characteristics of pn junction and Schottky diodes, and study the diode SPICE large-signal model. An understanding of the diode physics that affects the key performance parameters will help in designing power electronics circuits.

15.2 Electronic Power Switches

Power diodes and power MOSFETs are the commonly used semiconductor devices in PWM converters. These devices are used as fast electronic switches to control the flow of power to the load. To ensure reliability of power circuits, the designer must pay careful attention to semiconductor ratings such as maximum voltages and currents and maximum junction temperature T_{Jmax}. Power semiconductor devices must handle high current densities when ON and must withstand high voltages when OFF. In the on-state, the switches should be capable of conducting sufficiently high current,

$$I_{DM\,(max)} < I_{DM(MAX)}. \tag{15.1}$$

In addition, the on-resistance r_{ON} and the on-voltage drop V_{ON} should be as low as possible to reduce the conduction losses. In the off-state, the switches should have a sufficiently high breakdown voltage V_{BD},

$$V_{DSM(max)} < V_{BD}. \tag{15.2}$$

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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For power diodes, V_{BD} is usually denoted by V_{RRM} or V_{BR}. For power MOSFETs, V_{BD} is usually denoted by V_{DSS}. The gate-to-source voltage V_{GS} must be lower than its breakdown voltage $V_{GS(BD)}$,

$$V_{GS} < V_{GS(BD)}. \tag{15.3}$$

The maximum gate-to-source voltage is usually 20 V. Finally, the junction temperature T_J must be less than the maximum junction temperature $T_{J(MAX)}$,

$$T_J < T_{J(MAX)}. \tag{15.4}$$

The turn-on and turn-off switching times t_{sw} of the off-to-on and on-to-off transitions should be as short as possible to reduce the switching losses. To reduce the switching losses, the device capacitances should be as low as possible.

15.3 Intrinsic Semiconductors

Electrical material can be divided into three categories: conductors, semiconductors, and insulators. The primary electrical parameter describing these materials is the resistivity ρ. For conductors, $\rho < 10^{-3}\ \Omega$m. For semiconductors, $10^{-3}\ \Omega\text{m} \leq \rho \leq 10^{5}\ \Omega$m. For insulators, $\rho > 10^{5}\ \Omega$m.

Atoms can bond together in single-crystal, polycrystalline, and amorphous forms. A single-crystal semiconductor is formed by covalent bonding of each atom with its nearest neighbors in a highly regular thee-dimensional structure. A polycrystalline material consists of small crystallites. An amorphous material has a disordered structure.

The atom is the smallest particle of an element that retains all the characteristics of the element. The atom consists of a *nucleus* at the center, surrounded by orbiting electrons. The nucleus consists of *neutrons* that are neutral and *protons* that carry positive charge. The orbiting electrons carry negative charge and are aligned in a structured manner consisting of *shells* and *subshells*. Shells are designated with upper-case letters K, L, M, N. Subshells are designated with lower case letters s, p, d, f. The nth shell can contain a maximum of $2n^2$ electrons, where n is the outermost shell number. Silicon has 2 electrons in the K shell, 8 electrons in the L shell, and 4 electrons in the M shell. The outermost shell is called the *valence shell*, and the electrons in the valence shell are called the *valence electrons*. The valence shell of an atom can contain up to eight electrons. The conductivity of a material depends on the number of electrons in the valence shell. When the atom has one valence electron, it is a very good conductor (e.g., copper). When the atom has eight valence electrons, it is an insulator. Semiconductors are materials that contain four valence electrons. A semiconductor is neither a good conductor nor a good insulator. Atoms in semiconductors tend to share their valence electrons with neighboring atoms, resulting in a complete subshell for every atom. The sharing of valence electrons is called *covalent bonding*, which produces a stable, tightly bound lattice structure called a *crystal*.

Semiconductors can be divided into two groups: elemental semiconductors and compound semiconductors. Elemental semiconductors are formed from atoms of a single type from column IV of the periodic table of elements, such as silicon. Silicon has four valence electrons in the outermost shell. Compound semiconductors are made up from combinations of elements from columns III and V, such gallium arsenide (GaAs) and indium phosphide (InP), or both from column IV, such as silicon carbide (SiC).

A pure semiconductor without doping is called an *intrinsic semiconductor*. At low temperatures, almost all valence electrons reside in the covalent bonds and nearly all covalent

bonds are intact. Therefore, very few free electrons are available to conduct current and the material behaves as an insulator. At room temperature, a small number of covalent bonds are broken by *thermal ionization* and some electrons are free to serve as charge carriers, that is, to conduct current. The amount of energy required to break a covalent bond is referred to as the *band gap energy* E_G. When a covalent bond is broken, two charge carriers are produced: an electron and a hole. In other words, an electron–hole pair is generated. A hole represents the absence of an electron in an atom. Thermal ionization generates identical number of electrons n and holes p. Ionization rate is a strong function of temperature. Recombination is a process when some of the electrons fill some of the holes. An electron–hole pair disappears when an electron fills the hole. The time between the generation of an electron–hole pair and the recombination the pair is called the lifetime τ of the electron–hole pair.

Electrons and holes move through the crystal structure by two mechanisms: *drift* and *diffusion*. Drift current is a result of charge carrier motion caused by an applied electric field E. Diffusion current is caused by gradients in electron and hole concentrations.

The concentration of free electrons n is the number of electrons per unit volume, usually per cm^3. The concentration of holes p is the number of holes per unit volume. Electrons and holes can be thermally excited into the conduction band. In intrinsic semiconductors, the concentration of free electrons n (electron density) and the concentration of holes p (hole density) are equal, $n = p = n_i$, where n_i is an intrinsic concentration. In a semiconductor in thermal equilibrium, the product of electron and hole concentrations is a constant given by the *law of mass action*,

$$np = n_i^2 = BT^3 e^{-E_G/kT}, \tag{15.5}$$

where B is the material-dependent parameter, $B = 27 \times 10^{30}\,\text{K}^{-3}\text{cm}^{-6}$ for Si and $B = 1.207 \times 10^{-16}\,\text{K}^{-3}\text{cm}^{-6}$ for SiC, $k = 8.62 \times 10^{-5}$ eV/K is Boltzmann's constant, and E_G is the band gap energy. The intrinsic carrier concentration n_i increases rapidly with increasing temperature T,

$$n_i = \sqrt{np} = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2} e^{-\frac{E_G}{2kT}} = 4.8266 \times 10^{15} T^{3/2} e^{-\frac{E_G}{2kT}}\ \text{carriers/cm}^3, \tag{15.6}$$

where $m_e = 9.11 \times 10^{-31}$ kg is the mass of an electron, and $h = 6.626 \times 10^{-34}$ Js is Planck's constant. The band gap energy E_G is the minimum thermal energy of vibrating atoms required to break the covalent bond. For silicon, $E_{G(Si)} = 1.12\,\text{eV} = 1.12 \times 1.6 \times 10^{-19} = 1.792 \times 10^{-19}$ J ($1\,\text{eV} = 1.6 \times 10^{-19}$ J). For silicon carbide, $E_{G(SiC)} = 3.26\,\text{eV} = 3.26 \times 1.6 \times 10^{-19} = 5.216 \times 10^{-19}$ J. In the vicinity of room temperature, the term $T^{3/2}$ varies slowly in comparison with the exponential term. Hence, the temperature dependence of n_i is approximately exponential. The different values of band gap energy E_G account for different values of the intrinsic concentration n_i for different semiconductors at the same temperature T. For silicon, $n_i = 1.5 \times 10^{10}\,\text{cm}^{-3}$ at $T = 27^\circ\text{C} = 300\,\text{K}$, $n_i = 9.0581 \times 10^{12}\,\text{cm}^{-3}$ at $T = 150^\circ\text{C} = 423\,\text{K}$, and $n_i = 2.325 \times 10^{13}\,\text{cm}^{-3}$ at $T = 175^\circ = 448\,\text{K}$. Usually, the maximum operating temperature of silicon power devices is 150°C or 175°C. For silicon carbide, $n_i = 1.0987 \times 10^{-8}\,\text{cm}^{-3}$ at $T = 27^\circ\text{C} = 300\,\text{K}$, $n_i = 21.8859\,\text{cm}^{-3}$ at $T = 150^\circ\text{C} = 423\,\text{K}$, and $n_i = 1.2135 \times 10^{10}\,\text{cm}^{-3}$ at $T = 600^\circ\text{C} = 873\,\text{K}$. The density of silicon atoms in the crystal lattice is approximately $5 \times 10^{22}\,\text{cm}^{-3}$. Thus, only one bond in approximately 3.33×10^{12} atoms is broken at $T = 300\,\text{K}$. An intrinsic semiconductor is a poor conductor at room temperature. Figure 15.1 shows the intrinsic carrier concentrations n_i for silicon and silicon carbide as functions of temperature T.

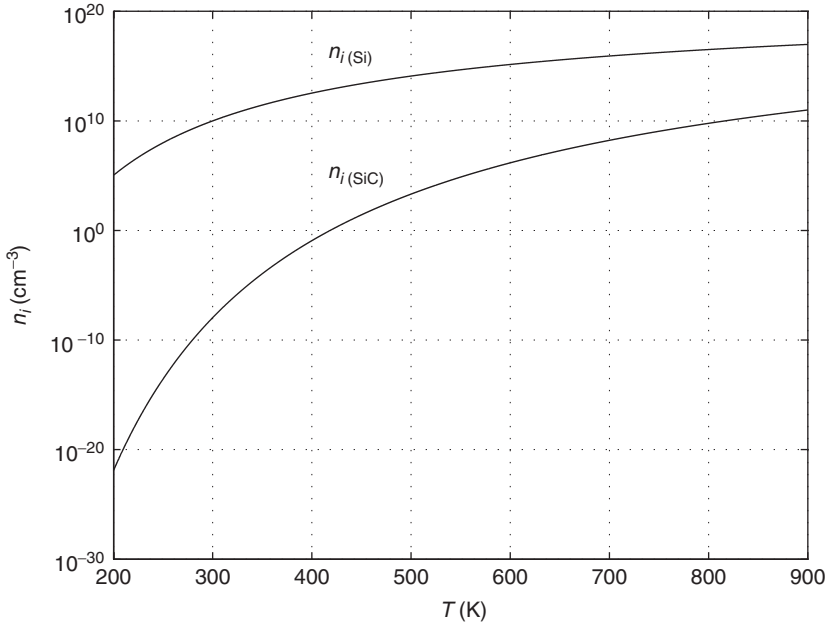


Figure 15.1 Intrinsic carrier concentrations n_i as a function of temperature T for silicon and silicon carbide.

15.4 Extrinsic Semiconductors

The electron and hole concentrations can be significantly altered by replacing a small number of atoms in the original crystal with impurity atoms, called *dopands*. In *extrinsic semiconductors*, the concentrations of electrons and holes are not equal ($n \neq p$). The ratio of the electron concentration to the hole concentration is changed by doping an intrinsic semiconductor (such as those from column IV of the periodic table) with elements from either column III (acceptors) or column V (donors). The n-type extrinsic semiconductor is produced when the intrinsic semiconductor is doped with the elements from column V that have five valence electrons, such as arsenic, antimony, and phosphorus. The n-type impurities donate electrons to intrinsic semiconductors. The electrons are the majority carriers and holes are the minority carriers. The concentration of the majority electrons is n_n and the concentration of the minority holes is p_n. For n-type semiconductors, the donor concentration N_D is usually several orders of magnitude higher than the intrinsic concentration n_i, $N_D \gg n_i$. The *charge neutrality* requires that the total negative charge is the same as the positive charge,

$$q(p + N_D^+ - n - N_A^-) = 0. \tag{15.7}$$

Hence, the majority free-electron concentration in the n-type semiconductors is approximately equal to the density of donor atoms,

$$n_n = N_D + p \approx N_D \neq f(T), \tag{15.8}$$

and the minority hole concentration is

$$p_n \approx \frac{n_i^2}{N_D} = f(T). \tag{15.9}$$

The conductivity of the n-type semiconductor is

$$\sigma_n = \frac{1}{\rho_n} = qN_D\mu_n, \tag{15.10}$$

where μ_n is the bulk mobility of electrons.

The p-type semiconductor is produced when the intrinsic semiconductor is doped with atoms from column III that have three valence electrons, such as boron, gallium, and aluminum. The p-type impurities accept electrons, thus producing holes. Holes are the majority carriers and electrons are the minority carriers. The concentration of the majority holes is p_p and the concentration of the minority electrons is n_p. For p-type semiconductors, the concentration of acceptors $N_A \gg n_i$ and the majority hole concentration is approximately equal to the acceptor density,

$$p_p = N_A + n \approx N_A \neq f(T), \tag{15.11}$$

and the minority electron concentration is

$$n_p \approx \frac{n_i^2}{N_A} = f(T). \tag{15.12}$$

The conductivity of the p-type semiconductor is

$$\sigma_p = \frac{1}{\rho_p} = qN_A\mu_p, \tag{15.13}$$

where μ_p is the bulk mobility of holes.

Both minority concentrations p_n and n_p are strongly dependent on temperature T because the intrinsic electron and hole concentrations n_i and p_i are strong functions of temperature. Therefore, the properties of minority (bipolar) devices are strongly dependent on temperature T. In contrast, the properties of majority (unipolar) devices are weakly dependent on temperature T. This is because the concentrations of ionized impurities are very close to the total impurity concentrations N_D and N_A at room temperature.

At sufficiently high temperatures, all extrinsic semiconductors become intrinsic because of the increase in n_i with temperature. Semiconductor devices do not operate properly above the upper limit of the extrinsic temperature at which $n = 0.1p$ resulting in $n_i = 0.35N_A$ for the p-region or $p = 0.1n$ resulting in $n_i = 0.35N_D$ for the n-region.

15.5 Silicon and Silicon Carbide

Two semiconductors are used to fabricate power devices: silicon and silicon carbide. Table 15.1 compares electrical and thermal properties of silicon (Si) and silicon carbide (4H-SiC). Silicon has low band gap energy E_G, low maximum operating junction temperature T_{Jmax}, low breakdown (or critical) electric field E_{BD} (also called dielectric strength), low saturation average carrier drift velocity, low thermal conductivity, high availability, low cost, and low melting point. Silicon dioxide (SiO_2) is a good insulator. Silicon is available as a natural mineral. The band gap energy E_G is the energy required to raise an electron from the valence band to the conduction band in a given semiconductor.

Silicon carbide has high band gap energy E_G, high breakdown electric field intensity E_{BD}, high operating junction temperature T_{Jmax}, high average carrier drift saturation velocity v_{sat}, high thermal conductivity, excellent thermal stability, high physical strength, and high chemical inertness. In large band gap semiconductors, the intrinsic carrier density n_i

Table 15.1 Properties of silicon and silicon carbide

Property	Symbol	Unit	Si	SiC
Band gap energy	E_G	eV	1.12	3.26
Band gap energy	E_G	J	1.792×10^{-19}	5.216×10^{-19}
Breakdown electric field	E_{BD}	V/cm	2×10^5	2.2×10^6
Dielectric constant	ϵ_r	–	11.9	9.7
Electron mobility at $T = 300\,\text{K}$	μ_n	cm^2/Vs	1360	900
Hole mobility at $T = 300\,\text{K}$	μ_p	cm^2/Vs	480	120
Surface μ_n at $T = 300\,\text{K}$	μ_n	cm^2/Vs	600	400
Saturation electron drift velocity	v_{sat}	cm/s	8×10^6	2.7×10^7
Intrinsic concentr. at $T = 300\,\text{K}$	n_i	cm^{-3}	1.5×10^{10}	1.0987×10^{-8}
Maximum junction temperature	T_{Jmax}	°C	200	600
Thermal conductivity	G_{th}	W/Kcm	1.5	4.56

is extremally small. For SiC, $n_i \approx 10^{-8}\,\text{cm}^{-3}$. Silicon carbide is capable of operating at high radiation levels in harsh environments. It makes natural SiO_2, which is used to form the most critical regions in the device structure, such as the gate oxide in a MOSFET. It is not available as a natural mineral. Silicon carbide is an excellent semiconductor to fabricate high-voltage, high-temperature, and high-frequency power devices. It is capable of operating at high radiation levels. A higher breakdown electric field E_{BD} allows for higher doping concentration, thinner drift region, lower specific on-resistance, and smaller die size for a given breakdown voltage V_{BD}. It also allows power devices to have higher breakdown voltages. A higher saturation carrier drift velocity yields higher operating frequencies suitable for high-power RF applications. SiC power devices are 30 times faster than Si power devices. High operating temperatures make SiC devices suitable for such applications as power supplies, electrical motor controls, car engine sensors, jet engine sensors, spacecraft electronics, energy storage, pulse power, utilities, intelligent machinery, locomotives, oil drilling equipment, chemical reaction monitoring, combustion control, and manufacturing. Thermal management for Sic devices is much easier than that of Si devices due to higher thermal conductivity and higher maximum junction temperature. Due to a wide SiC energy band gap – approximately 3 times wider than for Si – the maximum junction temperature T_{Jmax} for SiC is projected to be approximately 3 times higher than for Si. Silicon carbide has many polytypes, such as 3C-SiC, 4H-SiC, and 6H-SiC. However, the 4H-SiC polytype is preferred because of higher electron mobility. The mobility of 4H-SiC is twice that of 6H-SiC. Its much lower thermal minority carrier generation results in lower leakage currents. SiC is currently the most promising material for fabricating power semiconductor devices.

15.6 Physical Structure of Junction Diodes

There are two categories of power diodes:

- pn junction diodes (also called bipolar diodes),
- Schottky diodes (also called Schottky barrier diodes).

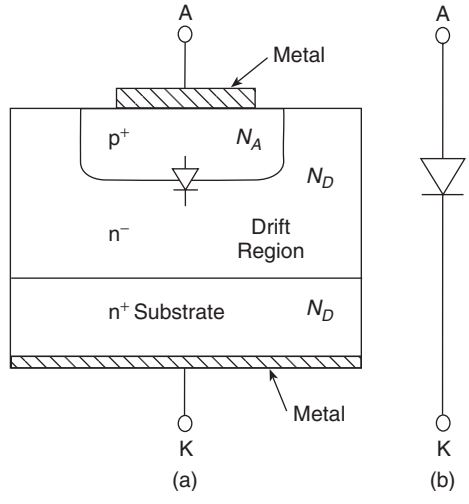


Figure 15.2 Cross section of *pn* junction diodes. (a) Cross section. (b) Electric symbol.

Power diodes are made of silicon or silicon carbide. The pn junction diode is formed within a single-crystal semiconductor by doping the n-region with donors N_D and an adjacent p-region with acceptors N_A. Donor atoms have five valence electrons and acceptor atoms have three valence electrons. The dopants commonly used for power device fabrication are phosphorus, arsenic, and antimony for the n-type region and boron, gallium, indium, and aluminum for the p-type region. A cross-section of a pn junction diode is depicted in Figure 15.2. The function of the low doped n^- drift region is to absorb the depletion region at high reverse voltages and prevent the diode voltage breakdown. Its thickness is between 10 and 200 μm. The thickness of the n^+ substrate is 150–300 μm to maintain the diode's mechanical integrity. Figure 15.3 shows a physical structure of a p^+n junction diode, along with the doping concentration N, space-charge density ρ, and electric field intensity E profiles. The p-side is doped with N_A acceptors/cm^3, and the n-side is doped with N_D donors/cm^3. Above 50 K, nearly all dopant atoms are ionized, resulting in constant values of N_D and N_A at all operating temperatures. Both n-type and p-type semiconductors are called *extrinsic* because their electrical properties are determined mainly by the dopants. For asymmetrically doped (or single-sided) p^+n junctions, $N_A \gg N_D$. For example, $N_A = 10^{17}\,\text{cm}^{-3}$ and $N_D = 10^{15}\,\text{cm}^{-3}$. The bulk of the n-side is electrically neutral because there are about the same number of electrons and positive donor ions. Similarly, the bulk of the p-side is electrically neutral because there are about the same number of holes and negative acceptor ions. However, the electrons that are near the junction will diffuse away from the region of high electron concentration on the n-side to the region of low electron concentration on the p-side. Likewise, the holes will diffuse from the region of the high hole concentration of the p-region to the region of the low hole concentration on the n-side. This will create a thin *depletion region*, also called the *depletion layer*. There is no mobile charge in the depletion region. There is no immobile charge and electric field outside the depletion region. The mobile carrier density is approximately zero in the depletion region (for $v_D \leq 0$). The electric field $\mathbf{E} = -\mathbf{i}_x E$ points from the n-side to the p-side. The electric field E is nonuniform in the depletion region, reaching its peak value E_m at the junction. The peak value must be kept below the breakdown value E_{BD}.

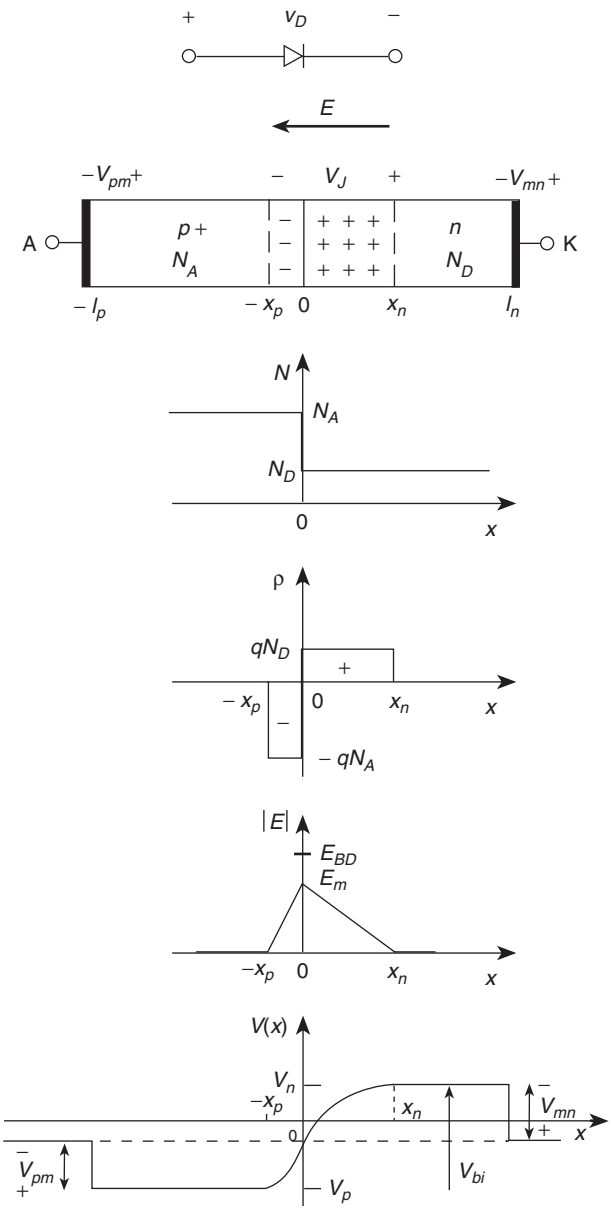


Figure 15.3 Physical structure of p^+n step junction diodes, doping concentration profile, space-charge density ρ, electric field intensity E, and voltage $V(x)$.

15.7 Static I–V Diode Characteristic

The diode characteristic consists of the forward-bias region, reverse-bias region, and breakdown region. The *ideal diode equation* for the forward- and reverse-bias regions is

$$I_D = I_S \left(e^{\frac{v_D}{nV_T}} - 1 \right), \tag{15.14}$$

where the *thermal voltage* is

$$V_T = \frac{kT}{q} = \frac{T}{11{,}609} \text{ (V)} \tag{15.15}$$

$V_T = 25.84\,\text{mV}$ at $T = 27^\circ\text{C}$, $k = 1.38 \times 10^{-23}\,\text{J/K}$ is Boltzmann's constant, $q = 1.602 \times 10^{-19}\,\text{C}$ is the magnitude of the electron charge, $T(\text{K}) = 273 + T(^\circ C)$ is the temperature, n is the emission coefficient, $n = 1$ for low-level injection and $n = 2$ for high-level injection, and I_S is the *reverse saturation current*. The reverse saturation current I_S increases with increasing temperature T and is given by

$$I_S(T) = A_J q \left(\frac{D_p}{L_p} p_{no} + \frac{D_n}{L_n} n_{po}\right) = A_J n_i^2 q \left(\frac{D_p}{N_D L_p} + \frac{D_n}{N_A L_n}\right) = bA_J n_i^2$$

$$= 2.322 \times 10^{31} bA_J T^3 e^{-\frac{E_G}{kT}} = aA_J T^3 e^{-\frac{E_G}{kT}}, \tag{15.16}$$

where a and b are constants, A_J is the junction cross-sectional area, $p_{no} = n_i^2/N_D$ is the concentration of holes in the n-region at the edge of the junction, $n_{po} = ni^2/N_A$ is the concentration of electrons in the p-region at the edge of the junction, L_n and L_p are diffusion lengths for electrons and holes, and D_n and D_p are diffusion coefficients for electrons and holes, respectively. For silicon, $D_n = 34\,\text{cm}^2/\text{s}$ and $D_p = 12\,\text{cm}^2/\text{s}$. For a diode with $I_S = 10^{-9}\,\text{A}$, $A_J = 1\,\text{cm}^2$, and $T = 300\,\text{K}$, we obtain $b = 4.444 \times 10^{-20}\,\text{A}$ and $a = 1.0319 \times 10^{12}\,\text{A}$. For example, $I_S = 10^{-14}\,\text{A}$ for small-signal silicon pn junction diodes, $I_S = 10^{-9}\,\text{A}$ for silicon pn junction power diodes, $I_S = 10^{-5}\,\text{A}$ for silicon Schottky power diodes, and $I_S = 10^{-20}\,\text{A}$ for silicon carbide diodes Schottky power diodes. The reverse saturation current I_S is proportional to the junction cross-sectional area A_J and to n_i^2.

The reverse saturation current I_S doubles for every 10°C increase in temperature. This dependence can be approximated by

$$I_S(T_2) = I_S(T_1) \times 2^{\frac{T_2 - T_1}{10}}. \tag{15.17}$$

As the temperature T increases from 20°C to 150°C, the saturation current I_S increases by a factor of 4096.

The threshold voltage V_F of silicon diodes decreases with increasing temperature T. The thermal coefficient of the threshold voltage for silicon pn junction diodes is given by

$$\delta_{T(Si)} = \frac{\Delta V_F}{\Delta T} = -2\,\text{mV}/^\circ\text{C}. \tag{15.18}$$

For every 1°C increase in temperature V_F decreases by approximately 2 mV. For silicon carbide diodes, the threshold voltage decreases with temperature at very low diode currents, but it increases with temperature at high currents. The threshold voltage is expressed as

$$V_F = V_{F0} + \delta_T (T - T_o), \tag{15.19}$$

where V_{F0} is the threshold voltage at $T = T_o$.

The neutral regions exhibit resistances determined by the doping level and dimensions. The resistance of the n^- region is R_n and the resistance of the p^+ region is R_p. The resistance of the n^+ substrate is R_{sub}. The resistance of the metal–semiconductor ohmic contacts is R_c. The resistivity of the substrate is high, but its thickness is large to maintain the mechanical integrity, usually of the order of 250–500 μm. The total series resistance is

$$R_S = R_n + R_p + R_{sub} + R_c. \tag{15.20}$$

At high diode currents, the voltage drop across the series resistance R_S reduces the voltage drop across the junction $V_J = V_D - R_S I_D$, as shown in Figure 15.4. Therefore, the diode

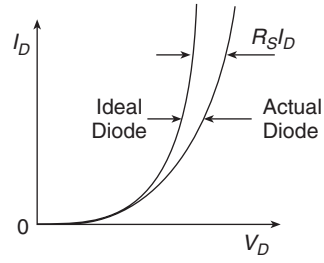


Figure 15.4 The effect of the voltage drop $R_S I_D$ across the neutral regions and the metal–semiconductor contacts on the diode characteristic at high currents.

characteristic for high currents is given by

$$I_D = I_S \left(e^{\frac{V_D - R_S I_D}{nV_T}} - 1 \right). \tag{15.21}$$

The reduction in junction voltage V_J lowers the excess carrier injection level and therefore the diode current increases more slowly with V_D. The emission coefficient is $n = 2$.

At high injection levels, high carrier concentrations reduce the resistivities of the neutral regions, reducing resistances R_n and R_p. The reduction of the resistivity resulting from high level of carrier injection is called *conductivity modulation*. This effect causes a significant reduction in the resistance of the drift region, reducing the conduction power loss. The diode equation for the high-injection range is

$$I_D = \frac{I_S}{1 + \dfrac{I_D}{I_H}} \left(e^{\frac{V_D - R_S I_D}{nV_T}} - 1 \right), \tag{15.22}$$

where I_H is the high-injection parameter.

The maximum diode forward current is

$$I_{Dmax} = A_J J_{Dmax}, \tag{15.23}$$

where the maximum forward current density typically is $J_{Dmax} = 100\,\text{A/cm}^2 = 1\,\text{A/mm}^2$. Typical values of the active junction area A_J are from 0.01 to $1\,\text{cm}^2$. For example, the junction area of the 15 A diode is $0.15\,\text{cm}^2$. To achieve high forward current density, all parasitic resistances must be minimized.

The static large-signal piecewise linear model of a diode consists of an ideal switch, a battery V_F, and a forward resistance R_F connected in series, as depicted in Figure 15.5. The voltage across the conducting diode is

$$V_D = V_F + R_F I_D. \tag{15.24}$$

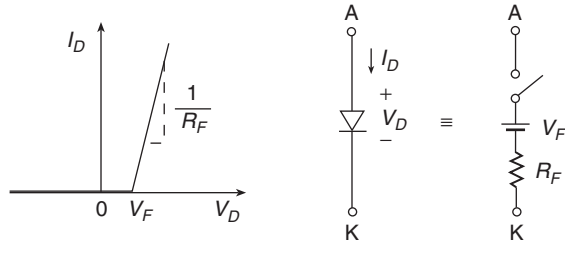


Figure 15.5 Piecewise linear large-signal model of a diode.

If a line is drawn along the linear high-current portion of the $I_D - V_D$ curve in the linear scale or in the semilog scale $\log I_D - V_D$ extending to the V_D-axis, the intercept on the V_D-axis is V_F and the slope is $1/R_F$, where $R_F = \Delta V_D / \Delta I_D$. At $T = 300\,\text{K}$, the threshold voltage V_F is typically 0.3 V for silicon Schottky diodes, 0.7 V for Si pn junction diodes, 1–1.5 V for silicon carbide Schottky diodes, and 2.5–2.8 V for SiC pn junction diodes. The forward resistance R_F ranges from 15 to 150 mΩ. As the temperature increases, the forward resistance R_F decreases for Si diodes and increases for SiC diodes.

15.8 Breakdown Voltage of Junction Diodes

A reverse-biased diode conducts a small reverse saturation current I_S due to thermally generated electron–hole pairs. A hole is a missing electron in a crystal structure. As the diode reverse voltage starts to approach the reverse breakdown voltage V_{BR}, the reverse current in the pn junction begins to increase. The breakdown is caused by two conduction mechanisms: *avalanche breakdown* and *Zener breakdown*. Avalanche voltage breakdown is caused by *impact ionization*, which results in *carrier multiplication*.

If either side of the junction is lightly doped, the breakdown mechanism involves impact ionization. A high reverse-biased junction voltage produces a high electric field E in the depletion region. The minority carriers that enter the depletion region from the neutral regions are strongly accelerated between the collisions by the electric field. During a collision, a carrier may have enough kinetic energy to break the covalent bond and release an electron, thus generating a free electron and a hole. The intense electric field E sweeps the electrons in one direction and the holes in the other. The newly generated carriers, before leaving the depletion region, are accelerated by the high electric field, collide with the fixed atoms, and generate new electron–hole pairs upon impact, which in turn generate further new electron–hole pairs. For a sufficiently intense electric field E, in the range of 2×10^5 V/cm for silicon, the impact-ionization process continues to the point where a high avalanche diode current is established, causing the *avalanche breakdown*. The avalanche effect causes junction breakdown at high voltages, usually for $V_{BR} \geq 8\,\text{V}$. Avalanche breakdown occurs in lightly doped pn junctions, where the depletion region is long and electrons are accelerated to high speeds and are able to knock out other electrons. The breakdown voltage V_{BR} increases as the doping decreases. The breakdown voltage V_{BR} also increases with the band gap energy E_G of the semiconductor because more energy is required for an ionizing collision.

The avalanche breakdown voltage V_{BR} increases as the junction temperature T_J increases, resulting in a positive temperature coefficient $\Delta V_{BR} / \Delta T$. For silicon, V_{BR} doubles for every 10°C increase in junction temperature T_J. At high temperatures, the atoms oscillate with larger amplitudes. Hence, the average distance between collisions (the mean free path of charge carriers) is shorter than at lower temperatures. For this reason, the rate of impact ionization is lower at higher temperatures, resulting in a higher avalanche breakdown voltage.

Zener breakdown occurs when both p- and n-regions are heavily doped, which results in a very thin depletion region. The layer is so thin that the carriers passing through it do not have enough collisions to produce a significant number of secondary carriers. Tunneling of electrons through the depletion layer from the p-side of valence band to the n-side of the conduction band constitutes a reverse diode current flowing from the n-side to the p-side of the junction. If either side of the junction is lightly doped, the depletion region is too wide for electron tunneling. The Zener effect causes the junction breakdown at low voltages, typically for $V_{BR} \leq 5\,\text{V}$. The Zener breakdown voltage V_{BR} decreases with

increasing junction temperature T_J, resulting in the negative temperature coefficient. For breakdown voltages between 5 and 8 V both avalanche and Zener effects may be significant.

The diode current in the vicinity of the breakdown voltage V_{BR} is described by an empirical relationship

$$I_D = MI_S = \frac{I_S}{1 - \left|\frac{V_D}{V_{BR}}\right|^p}, \quad \text{for } v_D \approx -V_{BR}, \tag{15.25}$$

where $M = 1/(1 - |V_D/V_{BR}|^p)$ is the multiplication factor and $p = 2$ to 6, depending on the type of material used for the junction. Neither of the two breakdown mechanisms is harmful to a junction. When taken out of breakdown, a diode behaves normally. However, a diode in the breakdown region is susceptible to damage due to overheating by the power loss $P_{BR} = I_D V_{BR}$. For silicon diodes, the breakdown voltage V_{BR} ranges from 2 to 2000 V. The avalanche process imposes an important limitation on the output voltage and output power of semiconductor devices. Therefore, wide band gap energy semiconductors have been intensively studied to develop high-voltage, high-power devices. Silicon carbide and gallium nitride are good semiconductors for fabricating such devices.

15.8.1 Width of Depletion Region

In the vicinity of the junction, mobile electrons move out of the n-type region and leave behind immobile ionized donor atoms with a positive charge. Similarly, mobile holes move out of the p-type semiconductor and leave behind immobile negatively charged acceptor atoms. Therefore, the region on both sides of the junction is depleted of mobile carriers and is called *depletion region*, *depletion layer*, or *space-charge region*. The n-side and p-side depletion layer widths are given by

$$x_n = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} - v_D)}{qN_D\left(1 + \frac{N_D}{N_A}\right)}} < l_n \tag{15.26}$$

and

$$x_p = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} - v_D)}{qN_A\left(1 + \frac{N_A}{N_D}\right)}} < l_p, \tag{15.27}$$

where l_n is the length of the n-region, l_p is the length of the p-region, $\epsilon_0 = 8.8542 \times 10^{-14}$ F/cm $= 8.8542 \times 10^{-12}$ F/m, ϵ_r is the semiconductor dielectric constant, $\epsilon_{r(\text{Si})} = 11.7$ for Si, $\epsilon_{r(\text{SiC})} = 9.7$ for SiC, and V_{bi} is the *built-in potential* expressed by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{15.28}$$

in which n_i is the intrinsic carrier concentration. The typical value of V_{bi} is 1 V for Si diodes and 10 V for SiC diodes. The junction voltage is $V_J = V_{bi} - v_D$. Hence, V_{bi} is the junction voltage drop at $v_D = 0$. The depletion layer width is given by

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} - v_D)}{q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}. \tag{15.29}$$

The depletion width W increases with increasing reverse-biased voltage $-v_D$ and is larger for lower doping concentrations. Figure 15.6 shows the depletion region width W as a function of the diode voltage v_D at selected doping concentrations N_D for $N_A = 10^{17}$ cm^{-3}.

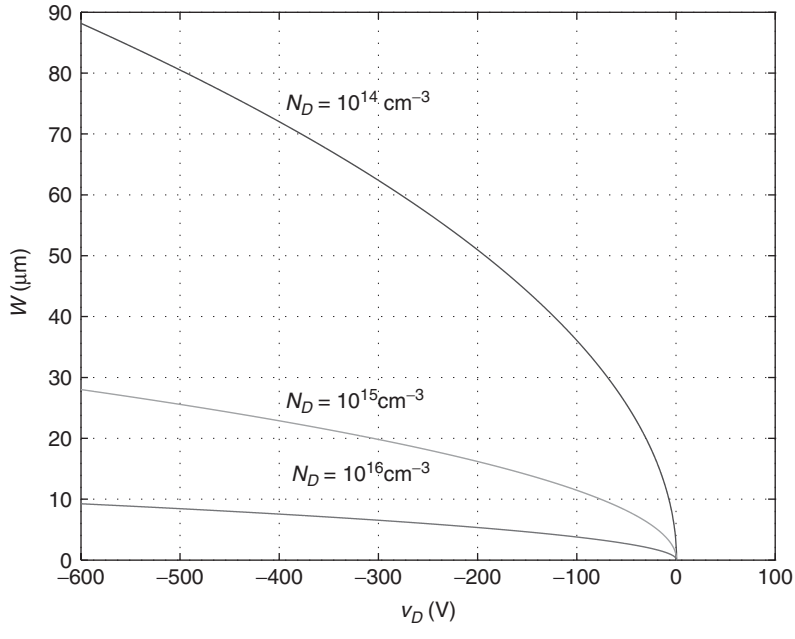


Figure 15.6 Depletion region width W as a function of the diode voltage v_D at selected doping concentrations N_D for $N_A = 10^{17}\,\text{cm}^{-3}$.

From the *charge-equity condition*, $qN_Dx_nA_J = qN_Ax_pA_J$, where A_J is the cross-sectional area of the junction. Hence,

$$\frac{x_n}{x_p} = \frac{N_A}{N_D}, \tag{15.30}$$

$$\frac{x_n}{W} = \frac{x_n}{x_n + x_p} = \frac{1}{1 + \dfrac{x_p}{x_n}} = \frac{1}{1 + \dfrac{N_D}{N_A}} = \frac{N_A}{N_D + N_A}, \tag{15.31}$$

and

$$\frac{x_p}{W} = \frac{x_p}{x_p + x_n} = \frac{1}{1 + \dfrac{x_n}{x_p}} = \frac{1}{1 + \dfrac{N_A}{N_D}} = \frac{N_D}{N_A + N_D}. \tag{15.32}$$

The depletion region extends further into a lightly doped semiconductor than it does into a heavily doped semiconductor. For p^+n junctions, $N_D \ll N_A$, $x_n \gg x_p$, i.e., the junction is one-sided, and therefore

$$W \approx x_n = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} - v_D)}{qN_D\left(1 + \dfrac{N_D}{N_A}\right)}} \approx \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} - v_D)}{qN_D}}. \tag{15.33}$$

15.8.2 Electric Field Distribution

Gauss's law in one dimension is

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_r\epsilon_0}. \tag{15.34}$$

For the step junction, the doping concentration in the n-type region N_D and the doping concentration in the p-type region N_A are constant, as illustrated in Figure 15.3. Therefore, the space charge

$$\rho = \begin{cases} 0, & \text{for } -l_p \le x \le -x_p, \\ -qN_A, & \text{for } -x_p \le x \le 0, \\ qN_D, & \text{for } 0 \le x \le x_n, \\ 0, & \text{for } x_n \le x \le l_n. \end{cases} \tag{15.35}$$

The electric field intensity distribution in the p-type region of the depletion layer is given by

$$E(x) = \frac{1}{\epsilon_r \epsilon_0} \int_{-x_p}^{x} \rho \, dx + E(-x_p) = \frac{1}{\epsilon_r \epsilon_0} \int_{-x_p}^{x} (-qN_A) \, dx + E(-x_p)$$

$$= -\frac{qN_A}{\epsilon_r \epsilon_0}(x + x_p), \quad \text{for} - x_p \le x \le 0, \tag{15.36}$$

where $E(-x_p) = 0$. Hence, the electric field intensity at the edge of the n-type region of the depletion layer is

$$E(x_n) = \frac{1}{\epsilon_r \epsilon_0} \int_{x}^{x_n} \rho \, dx + E(x) = \frac{1}{\epsilon_r \epsilon_0} \int_{x}^{x_n} (qN_D) \, dx + E(x) = \frac{qN_D}{\epsilon_r \epsilon_0}(x_n - x) + E(x) = 0. \tag{15.37}$$

Hence,

$$E(x) = \frac{qN_D}{\epsilon_r \epsilon_0}(x - x_n), \quad \text{for } 0 \le x \le x_n. \tag{15.38}$$

The electric field in the neutral regions is

$$E(x) = 0, \quad \text{for } x < -x_p \text{ and } x > x_n. \tag{15.39}$$

The maximum electric field strength E_m occurs at the interface between the p-region and the n-region,

$$E_m = -E(0) = \frac{qN_D x_n}{\epsilon_r \epsilon_0} = \frac{qN_A x_p}{\epsilon_r \epsilon_0} = \sqrt{\frac{2qN_D(V_{bi} - v_D)}{\epsilon_r \epsilon_0 \left(1 + \dfrac{N_D}{N_A}\right)}}. \tag{15.40}$$

The maximum electric field E_m increases with increasing reverse-biased voltage. For any applied voltage, E_m is lower for junctions with lower doping concentration. Figure 15.7 show the maximum electric field intensity E_m as a function of the diode voltage v_D at selected doping concentrations N_D for $N_A = 10^{17}\,\text{cm}^{-3}$.

Since the electric field intensity at any point x is the negative of the potential gradient at that point,

$$E(x) = -\frac{dV(x)}{dx}, \tag{15.41}$$

we have

$$dV(x) = -E(x)\,dx. \tag{15.42}$$

Integrating both sides of this equation, we obtain the voltage distribution in the depletion region. The voltage distribution in the p-type region of the depletion layer is given by

$$V(x) = -\int_{-x_p}^{x} E(x)\,dx + V(-x_p) = -\int_{-x_p}^{x} \left(\frac{-qN_A}{\epsilon_r \epsilon_0}\right)(x + x_p)\,dx + V(-x_p)$$

$$= \frac{qN_A}{2\epsilon_r \epsilon_0}(x + x_p)^2 + V_p, \quad \text{for} - x_p \le x \le 0, \tag{15.43}$$

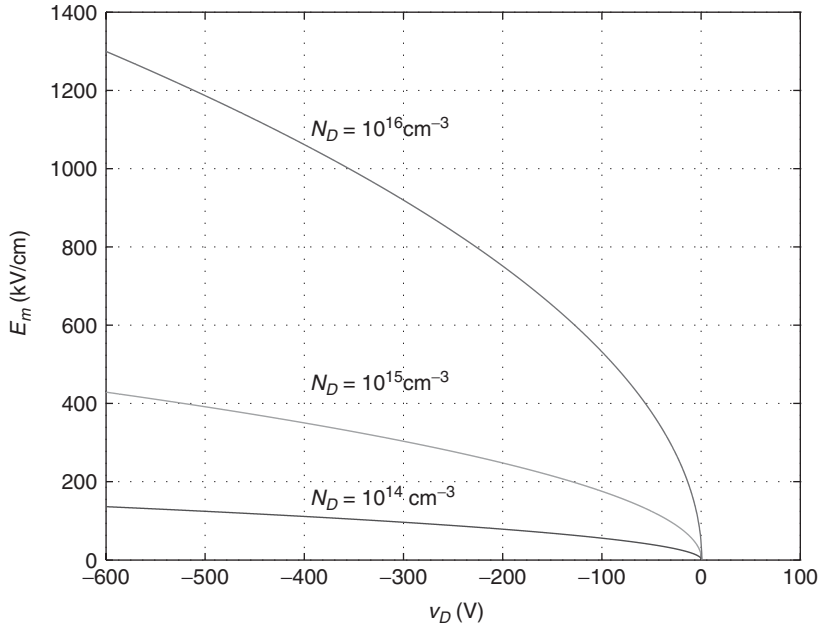


Figure 15.7 Maximum electric field intensity E_m as a function of the diode voltage v_D at selected doping concentrations N_D for $N_A = 10^{17}$ cm^{-3}.

where the potential of the p-type bulk region is

$$V_p = V(-x_p) = -V_T ln\left(\frac{N_A}{n_i}\right). \tag{15.44}$$

The voltage at the edge of the n-region of the depletion layer is

$$V(x_n) = -\int_x^{x_n} E(x)\,dx + V(x) = -\int_x^{x_n} \left(\frac{qN_D}{\epsilon_r\epsilon_0}\right)(x - x_n)\,dx + V(x)$$

$$= \frac{qN_D}{2\epsilon_r\epsilon_0}(x - x_n)^2 + V(x) = V_n. \tag{15.45}$$

Hence, the voltage distribution in the n-type region of the depletion layer is given by

$$V(x) = -\frac{qN_D}{2\epsilon_r\epsilon_0}(x - x_n)^2 + V_n, \quad \text{for } 0 \le x \le x_n, \tag{15.46}$$

where the potential of the n-type bulk region is

$$V_n = V(x_n) = V_T \ln\left(\frac{N_D}{n_i}\right). \tag{15.47}$$

The *built-in potential* is given by

$$V_{bi} = V_n - V_p = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right). \tag{15.48}$$

The contact potential occurs between any dissimilar pair of materials because of the difference in the potential energy of the conduction electrons, that is, the difference between their work functions. The metal–semiconductor structure can form an ohmic contact. The metal–semiconductor ohmic contact has no rectifying properties and behaves like a battery, whose potential drop is not a function of the forward or reverse current through it. It

presents no barrier to electron and hole flow in either direction. The metal–semiconductor ohmic contact has a constant potential and a very low resistance. It requires a heavy doping concentration in the semiconductor. The metal-to-p-type semiconductor ohmic contact voltage drop is V_{pm} and the n-type semiconductor-to-metal ohmic contact voltage drop is V_{mn}. For $v_D = 0$, the junction voltage is equal to the potential barrier height between the p- and n-regions,

$$V_J = V_{bi} = -(V_{pm} + V_{mn}). \tag{15.49}$$

When a diode voltage v_D is applied, the junction voltage is given by

$$V_J = V_{bi} - v_D = -(V_{pm} + V_{mn}) - v_D. \tag{15.50}$$

The metal–semiconductor ohmic contact potentials V_{pm} and V_{mn} are unaffected by the diode applied voltage v_D. The flow of diode current can be controlled by controlling the potential barrier height. When v_D is negative, the potential barrier height is high and the reverse diode current is very low. When v_D is positive and sufficiently high, the potential barrier height is low and the forward diode current is large.

15.8.3 Avalanche Breakdown Voltage

When E_m approaches the breakdown (or critical) electric field intensity E_{BD}, avalanche breakdown occurs. Setting $E_m = E_{BD}$ and $v_D = -V_{BD}$, we obtain the diode avalanche breakdown voltage

$$V_{BD} = \frac{\epsilon_r \epsilon_0 \left(1 + \dfrac{N_D}{N_A}\right) E_{BD}^2}{2qN_D} - V_{bi}. \tag{15.51}$$

Reducing the doping concentration on the lightly doped side allows the diode to support higher voltages. Usually, doping levels below $10^{15}\,\text{cm}^{-3}$ are necessary to achieve high breakdown voltages for silicon. Figure 15.8 shows the breakdown voltage V_{BD} as a function of doping concentration N_D at $N_A = 10^{17}\,\text{cm}^{-3}$ for silicon and silicon carbide.

For silicon, $E_{BD} = 2 \times 10^5$ V/cm (theoretically, $E_{BD} = 3 \times 10^5$ for silicon). The breakdown electric field E_{BD} of a semiconductor increases with increasing band gap energy E_G. The breakdown voltage V_{BD} can be increased by using semiconductors with a higher breakdown electrical field strength E_{BD}, such as silicon carbide, which has $E_{BD} = 22 \times 10^5$ V/cm. Assuming the same doping concentration N_D,

$$\frac{V_{BD(SiC)}}{V_{BD(Si)}} = \frac{\epsilon_{r(SiC)} E_{BD(SiC)}^2}{\epsilon_{r(Si)} E_{BD(Si)}^2} = \frac{9.7 \times (22 \times 10^5)^2}{11.7 \times (2 \times 10^5)^2} = 100.316. \tag{15.52}$$

Figure 15.9 shows the electric field distribution for two levels of doping concentration N_D.

15.8.4 Punch-through Breakdown Voltage

When the depletion region reaches one of the edges of the semiconductor, the diode current begins to increase very rapidly, causing *punch-through voltage breakdown*. If the breakdown occurs on the n-side first (as in p^+n diodes), we substitute $x_n = l_n$ and $v_D = -V_{BD(PT)}$ into

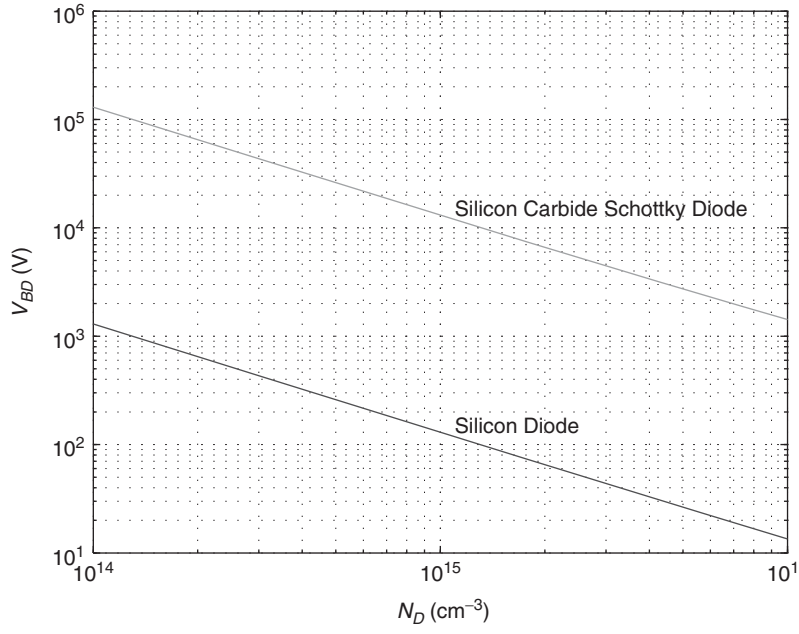


Figure 15.8 Breakdown voltage V_{BD} as a function of doping concentration N_D at $N_A = 10^{17}\,\text{cm}^{-3}$ for silicon and silicon carbide.

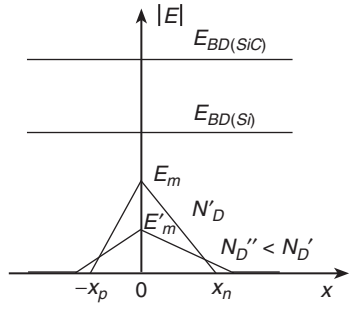


Figure 15.9 Electric field distribution at two levels of doping concentration N_D.

(15.26) to obtain the minimum length of the n-side,

$$l_n = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{bi} + V_{BD(PT)})}{qN_D\left(1 + \dfrac{N_D}{N_A}\right)}}. \tag{15.53}$$

Hence, the punch-through breakdown voltage is

$$V_{BD(PT)} = \frac{ql_n^2 N_D}{2\epsilon_r\epsilon_0}\left(1 + \frac{N_D}{N_A}\right) - V_{bi}. \tag{15.54}$$

Most diodes are designed to avoid punch-through voltage breakdown and the maximum reverse voltage is limited by the avalanche breakdown. A nonpunch-through drift region

corresponds to the case where the drift region thickness is equal to or larger than the parallel-plane avalanche breakdown width. In high voltage diodes, the n^- region is so lightly doped that it is a nearly intrinsic region. This type of device is called a *pin* diode. The electric field intensity is nearly constant in the i-region, reducing the length l_n by a factor of 2 at the same breakdown voltage.

Using (15.40) and (15.53) and setting $V_{BD} = V_{BD(PT)}$ and $x_n = l_n$, we obtain

$$l_n = \frac{\epsilon_r \epsilon_0 E_{BD}}{qN_D}. \tag{15.55}$$

From (15.54), the breakdown voltage can be expressed as

$$V_{BD} = \frac{\epsilon_r \epsilon_0 \left(1 + \dfrac{N_D}{N_A}\right) E_{BD}^2}{2qN_D} - V_{bi} \approx \frac{\epsilon_r \epsilon_0 E_{BD}^2}{2qN_D} = \frac{l_n E_{BD}}{2}. \tag{15.56}$$

Hence, the minimum length of the n-region at the maximum doping concentration is

$$l_n = \frac{2V_{BD}}{E_{BD}}. \tag{15.57}$$

The ratio of the drift length of the silicon diode $l_{n(Si)}$ to the drift length of the silicon carbide diode $l_{n(SiC)}$ at the same breakdown voltage V_{BD} is given by

$$\frac{l_{n(Si)}}{l_{n(SiC)}} = \frac{E_{BD(SiC)}}{E_{BD(Si)}} = \frac{2.2 \times 10^6}{2 \times 10^5} = 11. \tag{15.58}$$

15.8.5 Edge Terminations

So far only parallel-plate (infinitely flat) pn junctions have been considered and therefore edge effects have been neglected. Actual junctions are manufactured using masks and diffusions of impurities, resulting in pn junctions with curvature. Therefore, the electric field in the depletion region is nonuniform and has the highest values in areas with the shortest radius of curvature, reducing the breakdown voltage. By Coulomb's law, the charge density is the largest at the junction edges. The edge effects limit the breakdown voltage of practical diffused pn junctions to values below those set by ideal infinitely flat junctions. The electric field concentration occurs at the junction curvature, resulting in a severe reduction in the breakdown voltage. If the junction is poorly terminated, the breakdown voltage can be as low as 20 % of the breakdown voltage of the ideal diode. Since the charge balance between the two sides of the junction must be satisfied, the junction curvature leads to electric field crowding, as illustrated in Figure 15.10(a). A higher electric field intensity at the junction edges causes larger impact ionization in these areas. Consequently, the junction breakdown occurs at the edges rather than in the parallel-plane portion.

An effective edge termination technique makes the electric field distribution uniform at the edge of the diode in order to approach the breakdown voltage of an ideal diode. Many techniques, such as guard rings, floating field rings, trench rings, and junction termination extension, have been used to achieve this objective. To achieve near-ideal breakdown voltage, an implanted boron edge termination can be used around the device. Figure 15.10(b) shows a guard ring, resulting in more even distribution of electric field [2]. Multiple guard ring and field plate terminations are also used to reduce high concentrations of the electric field. Figure 15.11 shows the depletion region in a diode with multiple guard rings. The width and the spacing between individual floating rings are reduced with increasing distance from the main junction. Therefore, the depletion region thickness below them becomes

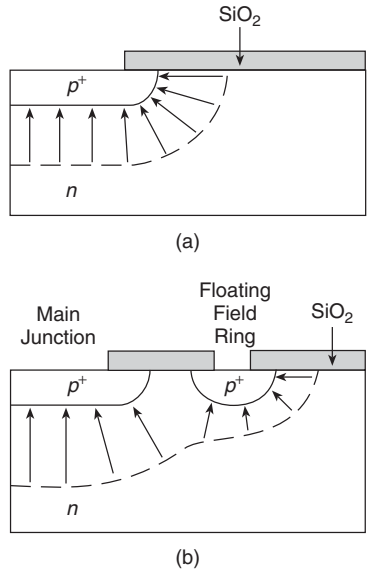


Figure 15.10 Electric field distribution in the pn junction without and with guard ring. (a) Electric field concentration at the corner. (b) More evenly distributed electric field in the diode with guard ring.

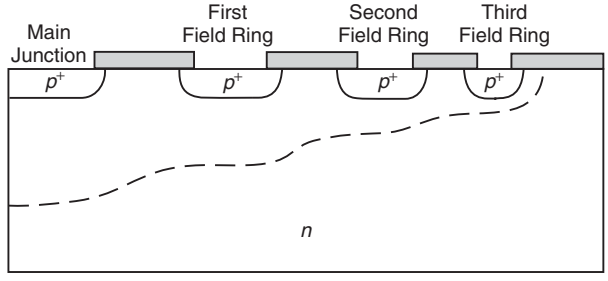


Figure 15.11 Depletion region profile in the pn junction diode with multiple guard ring termination.

progressively smaller. This allows the diode to achieve up to 80 % of the breakdown voltage of an ideal parallel plane junction. Beveled edge junction terminations can be used in large diodes to reduce surface electric field. Defects in the semiconductor structure reduce the junction breakdown voltage.

15.9 Capacitances of Junction Diodes

Power diodes are often used as electronic switches. Therefore, important parameters are their off-to-on and on-to-off transitions. There are charges stored in the depletion region and in the neutral regions. As a result, there are two capacitances in the pn junction diode model: the junction capacitance C_J and the diffusion capacitance C_D. The junction capacitance C_J is dominant in the reverse-bias region and the diffusion capacitance C_D is dominant in the forward-bias region.

15.9.1 Junction Capacitance

In the reverse-bias region, the depletion region does not contain free carriers and behaves like an insulator between the layers of opposite charge. This situation is similar to a parallel-plate capacitor. As the reverse voltage increases by Δv_D, the separation of the small-signal junction capacitance plates increases by $\Delta(x_n + x_p)$, the depletion width on the n-side increases by Δx_n and on the p-side by Δx_p, and the charge stored on either side of the depletion layer increases by ΔQ, as shown in Figure 15.12. It turns out that the incremental junction capacitance $C_J = \Delta Q/(-\Delta v_D)$ decreases steadily as v_D decreases to more negative values.

There is a *voltage-dependent charge* associated with the depletion region. The immobile depletion charge is stored on both sides of the junction. The immobile positive depletion charge due to donor ions that have been stripped of their mobile electrons is stored on the n-side of the depletion region in the volume $x_n A_J$. This charge is given by

$$Q_{Jn} = qN_D x_n A_J = A_J \sqrt{\frac{2q\epsilon_r\epsilon_0 N_D (V_{bi} - v_D)}{1 + \dfrac{N_D}{N_A}}}. \tag{15.59}$$

Figure 15.13 shows plots of Q_{Jn}, C_J, and W_{CJ} as functions of v_D.

The charge Q_{Jn} changes with the diode voltage v_D, resulting in the junction capacitance. The charge Q_{Jn} increases as the diode voltage v_D decreases. The small-signal (incremental) junction capacitance C_J is the modulus of the slope of the Q_{Jn}–v_D curve $C_J = \Delta Q_{Jn}/(-\Delta v_D)$ at the operating point $v_D = V_D$. For step junctions,

$$C_J = -\left.\frac{dQ_{Jn}}{dv_D}\right|_{v_D = V_D} = A_J \sqrt{\frac{\epsilon_r\epsilon_0 q}{2V_{bi}\left(\dfrac{1}{N_D} + \dfrac{1}{N_A}\right)\left(1 - \dfrac{v_D}{V_{bi}}\right)}} = \frac{C_{J0}}{\sqrt{1 - \dfrac{V_D}{V_{bi}}}}$$

$$= \frac{\epsilon A_J}{W}, \quad \text{for } v_D \le V_{bi}, \tag{15.60}$$

where C_{J0} is the small-signal junction capacitance at $v_D = 0$,

$$C_{J0} = A_J \sqrt{\frac{q\epsilon_r\epsilon_0}{2V_{bi}\left(\dfrac{1}{N_A} + \dfrac{1}{N_D}\right)}} \tag{15.61}$$

and V_{bi} is the *built-in potential* ranging from 0.55 to 1 V for silicon junction diodes, $V_{bi} = 0.5$ V for silicon Schottky diodes, and $V_{bi} = 1.1$ V for silicon carbide Schottky diodes.

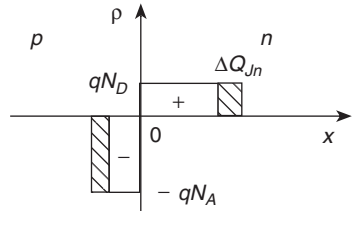


Figure 15.12 Changes in the charge stored in the depletion region and the depletion region width due to the diode voltage change v_D (usually for the reverse bias). The changes in the stored charge ΔQ_{Jn} and the depletion region width on the n-side Δx_n result in the junction capacitance C_J.

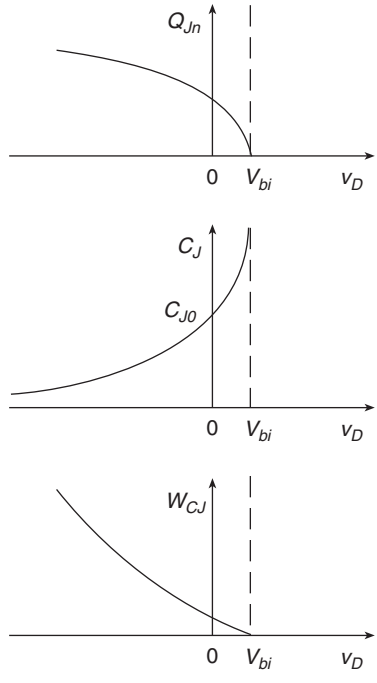


Figure 15.13 Charge Q_{Jn}, junction capacitance C_J, and energy stored in the junction capacitance W_{CJ} as functions of diode voltage v_D. (a) Charge stored in the depletion region on the n-side. (b) Junction capacitance C_J. (c) Energy stored in the junction capacitance W_{CJ}.

The expression $C_J = \epsilon A_J / W$ is identical to that of the capacitance of two closely spaced parallel plates separated by a distance W by a dielectric of permittivity $\epsilon = \epsilon_r \epsilon_0$. The diode voltage V_D modulates the separation W between the capacitor plates. For p^+n junctions,

$$C_{J0} = A_J \sqrt{\frac{q \epsilon_r \epsilon_0 N_D}{2 V_{bi}}}. \tag{15.62}$$

For impurity concentration profiles more gradual than the step junction, the small-signal junction capacitance is expressed by

$$C_J = \frac{C_{J0}}{\left(1 - \dfrac{V_D}{V_{bi}}\right)^m}, \quad \text{for } v_D \leq V_{bi}, \tag{15.63}$$

where m is the *grading coefficient*. For linearly graded junctions, $m = \frac{1}{3}$. For step junctions, $m = \frac{1}{2}$. For all doping concentration profiles, C_{J0} is directly proportional to the junction area A_J. High-current diodes have a large junction area A_J, resulting in a large junction capacitance C_J.

The large-signal junction capacitance is given by

$$C_{J(LS)} = \frac{Q_{Jn}}{v_D} = A_J \sqrt{\frac{2 q \epsilon_r \epsilon_0 N_D}{1 + \dfrac{N_D}{N_A}} \left(\frac{V_{bi} - v_D}{v_D^2}\right)}. \tag{15.64}$$

The energy stored in the junction capacitance C_J at voltage v_D is

$$W_{CJ} = -\int_0^{v_D} C_J v_D d(v_D) = \frac{2}{3}\sqrt{\frac{q\epsilon_r\epsilon_0 N_D}{2\left(1+\frac{N_D}{N_A}\right)}}(V_{bi}-v_D)^{3/2}. \tag{15.65}$$

The current through the junction capacitance C_J can be determined from the equation

$$i_{C_J} = \frac{dQ_{Jn}}{dt} = C_J\frac{dv_D}{dt} = \frac{C_{J0}}{\sqrt{1-\frac{v_D}{V_{bi}}}}\frac{dv_D}{dt}. \tag{15.66}$$

For example, if the diode voltage is sinusoidal, when the diode is OFF,

$$v_D = V_m \sin\ \omega t, \qquad \text{for} \qquad v_D < V_F, \tag{15.67}$$

the current through the junction capacitance C_J is given by

$$i_{C_J} = \frac{\omega C_{J0}}{\sqrt{1-\frac{V_m \sin\ \omega t}{V_{bi}}}} V_m \cos\ \omega t \qquad \text{for} \qquad v_D < V_F. \tag{15.68}$$

Figure 15.14 shows the current waveform through the junction capacitance C_J for the Cree CSD10060 SiC Schottky diode in a circuit consisting of a sinusoidal voltage source, a resistor R, and a diode connected in series. The amplitude of the voltage source was $V_m = 9$ V, the operating frequency was $f = 200$ kHz, and the series resistance was $R = 500\,\Omega$. The Schottky diode parameters were $C_{J0} = 381$ pF, $V_{bi} = 9.99$ V, and $T = 300$ K. When the diode turns off at $\omega t = 180^\circ$, the junction current i_{CJ} has a step change from zero to -4.3 mA. Then it increase, crosses zero, and reaches 4.3 mA at the end of the cycle at $\omega t = 360^\circ$. The junction current flows through resistances connected in series with the Schottky diode, causing power losses and reducing the efficiency of the overall system. As the operating frequency increases, the peak-to-peak value of the junction diode current also increases in proportion to frequency, causing larger power losses. SPICE simulation gives nearly identical waveform of the junction current waveform.

15.9.2 Diffusion Capacitance

When the pn junction is forward biased, the depletion region narrows and the junction capacitance C_J increases. However, a large number of minority carriers injected causes much greater excess charge. The excess minority-carrier charges are stored in the neutral regions. In each region, the excess holes and free electrons represent equal and opposite charges. For example, holes injected across the depletion layer into the n-region are stored in the quasi-neutral n-region immediately adjacent to the depletion region edge for $x > x_n$. For p^+n junctions, the electron current is negligible and the excess minority hole carrier charge due to diffusion is given by

$$Q_{Dp} \approx \tau_p i_D = \tau_p I_S(e^{\frac{v_D}{nV_T}} - 1), \tag{15.69}$$

where τ_p is the *hole carrier lifetime* in the n-type region. The hole carrier lifetime τ_p ranges from 1 fs to 1 μs. The excess charge Q_{Dp} increases by ΔQ_{Dp} as the diode voltage v_D increases by Δv_D, yielding the incremental diffusion capacitance $C_D = \Delta Q_{Dp}/\Delta v_D$, as

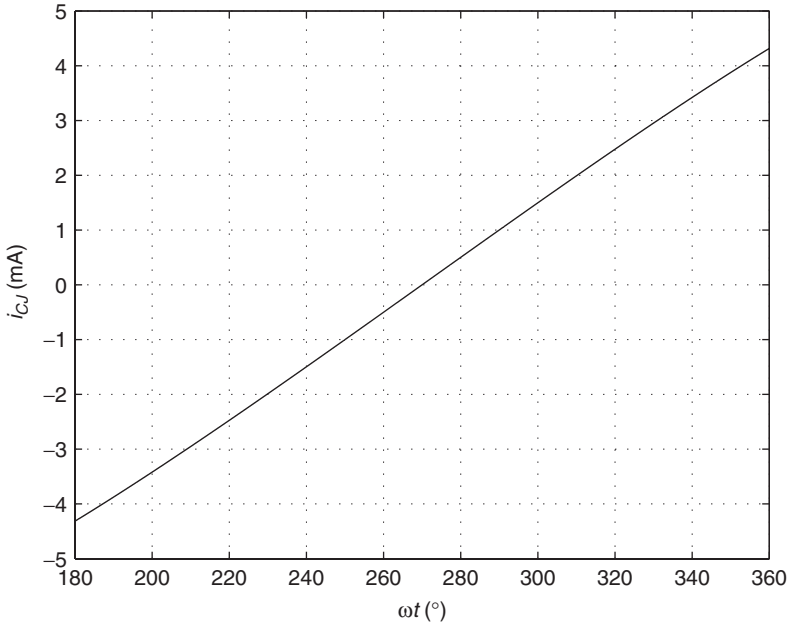


Figure 15.14 Waveform of the current through the junction capacitance C_J for the Cree CSD10060 SiC Schottky diode at $C_{J0} = 381\,\text{pF}$, $V_{bi} = 9.99\,\text{V}$, $R = 500\,\Omega$, $V_m = 9\,\text{V}$, $f = 200\,\text{kHz}$, and $T = 300\,\text{K}$.

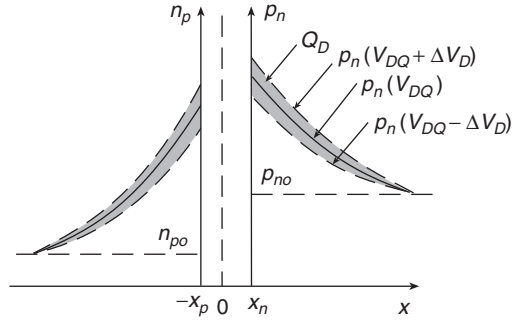


Figure 15.15 Change in minority carrier charge stored in the bulk regions due to a diode voltage change around the dc quiescent diode voltage V_{DQ}. The change in the excess carrier minority charge results in the diffusion capacitance C_D.

shown in Figure 15.15. The slope of the Q_{Dp}-v_D curve at the operating point $v_D = V_D$ is the small-signal diffusion capacitance

$$C_D = \left.\frac{dQ_{Dp}}{dv_D}\right|_{v_D=V_D} = \tau_p \left.\frac{di_D}{dv_D}\right|_{v_D=V_D} = \left.\frac{\tau_p}{nV_T} I_S e^{\frac{v_D}{nV_T}}\right|_{v_D=V_D} = \frac{\tau_p}{nV_T} I_S e^{\frac{V_D}{nV_T}}$$

$$= \frac{\tau_p}{nV_T}\left(I_S e^{\frac{V_D}{nV_T}} - I_S + I_S\right) = \tau_p \frac{(I_D + I_S)}{nV_T} = \frac{\tau_p}{r_d} \tag{15.70}$$

where $r_d = dv_D/di_D$ is the small-signal resistance of the diode at the operating point $v_D = V_D$. Note that $\tau_p = r_d C_D$. The diffusion capacitance C_D is negligible for reverse-biased

junctions because $i_D \approx -I_S$ and $di_D/dt \approx 0$. The large-signal diffusion capacitance is

$$C_{D(LS)} = \frac{Q_D}{v_D} = \frac{\tau_p i_D}{v_D}. \tag{15.71}$$

There are low-frequency and high-frequency diodes. The high-frequency switching diodes used in power electronics include soft recovery, fast recovery, ultrafast recovery, and hyperfast recovery pn junction silicon diodes, in which the reverse recovery switching time and power loss are reduced. For fast recovery diodes, $t_{rr} \leq 500$ ns. For ultrafast recovery diodes, $t_{rr} \leq 100$ ns. For hyperfast recovery diodes, $t_{rr} \leq 1$ ns. For instance, an IFR 8ETH06 hyperfast recovery diode has $t_{rr} = 1$ ns. For small-signal diodes, $0.75 \text{ ns} \leq t_{rr} \leq 5$ ns. The forward voltage drop of fast diodes is typically greater than that of slower diodes. The switching loss of diodes is due to the reverse recovery loss when a diode turns off.

15.10 Reverse Recovery of pn Junction Diodes

15.10.1 Qualitative Description

When a forward-biased voltage is applied, a large number of electrons progress through the depletion region from the n-type material into the p-type material and a large number of holes progress from the p-type material into the n-type material. The electrons in the p-type material and holes in the n-type material establish a large number of minority carriers in each material in the quasi-neutral regions immediately adjacent to the depletion region edges. This excess charge must be removed from both sides of the quasi-neutral regions, when the diode is switched from forward to reverse bias, as shown in Figure 15.16. Figure 15.17 shows the hole distribution in the n-region as a function of time during the turn-off transition.

When the applied voltage is reversed, the ideal diode should change instantaneously from the conducting state to the nonconducting state and start blocking the voltage. In a real diode, the excess of minority carriers stored in the diode must be removed before the diode is able to block the reverse voltage. The stored excess minority charge can be removed (1) by the flow of a reverse diode current and (2) by the recombination of the minority carriers. When the reverse current flows, the excess carriers are drawn beck across

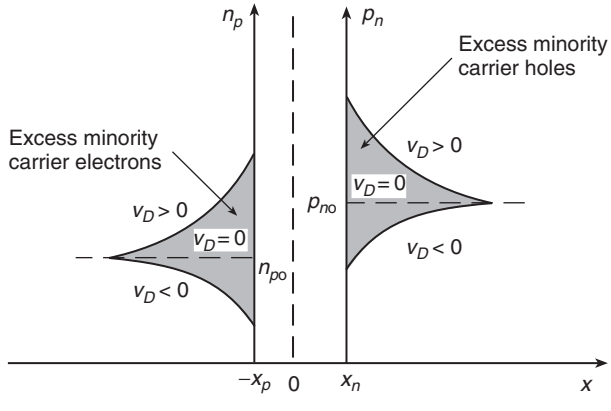


Figure 15.16 Change in minority carrier charge stored in the bulk regions during the turn-off transition. This charge must be removed when the diode is turned off from forward to reverse bias.

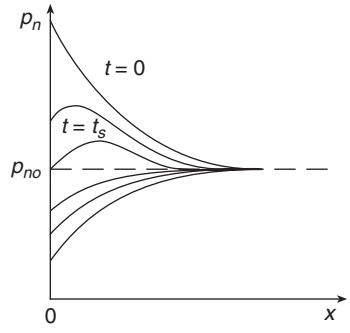


Figure 15.17 Hole distribution in the n-region as a function of time during the turn-off transition.

the junction. If $|I_R| \gg I_F$, most of the excess charge is removed by the reverse current flow. In contrast, if $|I_R| \ll I_F$, most of the excess charge is removed by recombination. The process of removing the excess charge is called *reverse recovery*.

15.10.2 Reverse Recovery in Resistive Circuits

The simplest circuit for studying the transitions in diodes consists of a square-wave voltage source v, a resistor R, and a diode, as depicted in Figure 15.18. Figure 15.19 shows the waveforms for pn junction diodes. The dynamic $i_D - v_D$ diode characteristic during the turn-off transition is shown in Figure 15.20.

The forward diode current is given by

$$I_F = \frac{V_H - V_{ON}}{R}. \tag{15.72}$$

The waveforms during the turn-on transition are shown in Figure 15.21. If a constant current I_F flows long enough, the minority carrier densities reach steady state and the excess stored charge is

$$Q_F = \tau I_F, \tag{15.73}$$

where τ is the carrier lifetime.

When the source voltage v is abruptly changed from a positive voltage V_H to a negative voltage V_R, the diode voltage cannot suddenly change because of the charge stored in the diffusion capacitance C_D. The diode current jumps to a negative value given by

$$I_R = \frac{V_R - V_{ON}}{R}. \tag{15.74}$$

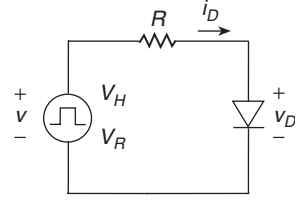


Figure 15.18 Circuit for studying the on-to-off and off-to-on transitions in diodes.

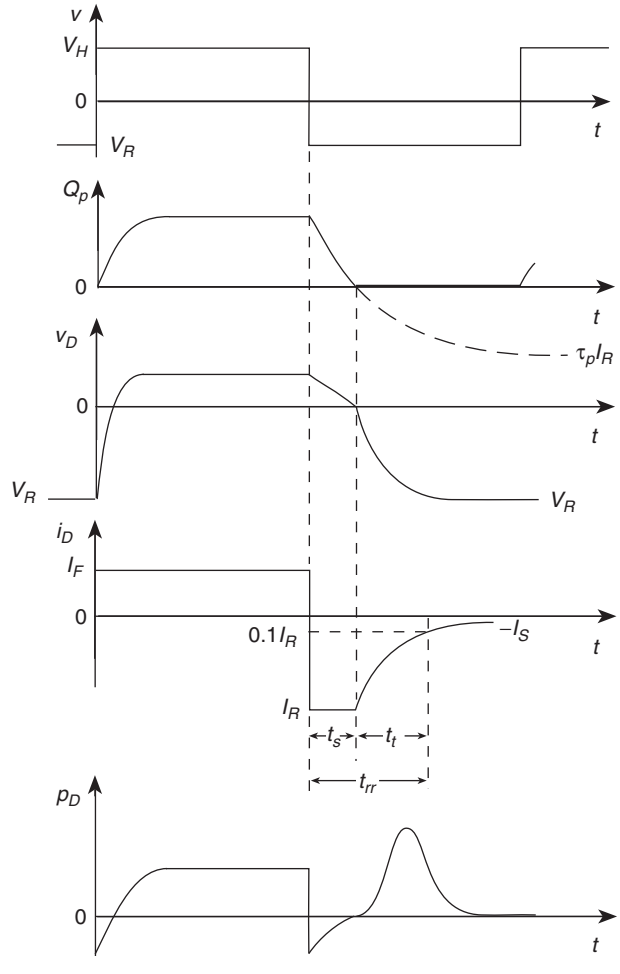


Figure 15.19 Waveforms for on-to-off and off-to-on transitions in junction diodes.

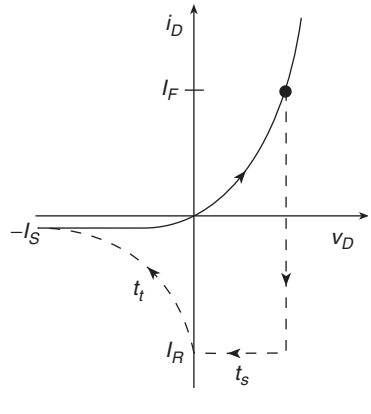


Figure 15.20 Dynamic $i_D - v_D$ diode characteristic during the turn-off transition in resistive circuit with square-wave driving voltage.

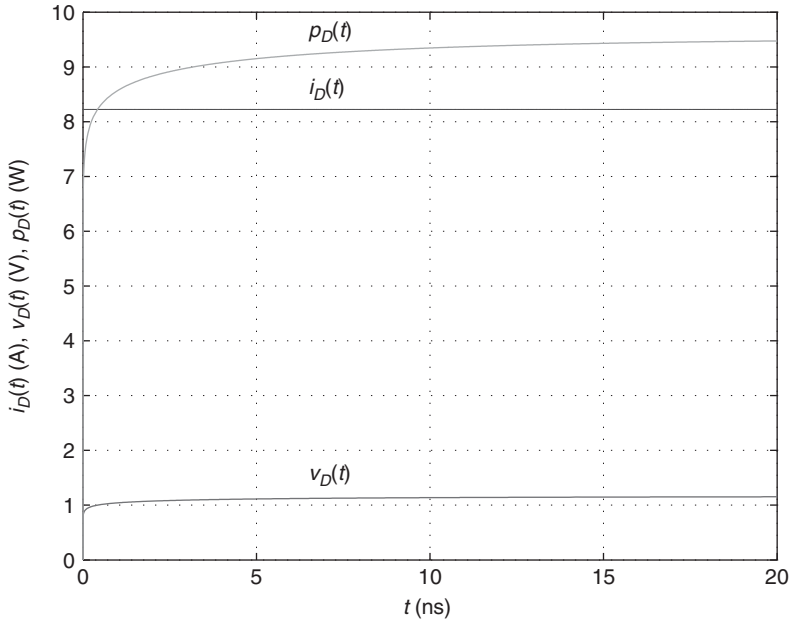


Figure 15.21 Waveforms for pn junction diode during the turn-on transition.

During the *storage time* t_s, the stored charge $Q_p(t)$ will gradually decrease to zero. The diode remains ON during the storage time t_s. At the end of the storage time t_s, the excess charge Q_p is removed and the diode voltage drops to zero.

During the *transient time* t_t, the diode current decreases exponentially from I_R to $-I_S$ and the diode voltage decreases exponentially from zero to V_R, charging the junction capacitance C_J. The storage time t_s is the time interval between the instant the diode current passes through zero and the instant the diode current reaches the peak reverse value I_R. The transition time interval t_t is defined as the time interval between the instant the diode current is equal to the peak reverse current I_R and the instant the diode current reaches 10 % (or 25 %) of I_R.

The *reverse recovery time* t_{rr} is defined as the time between the instant the diode current crosses zero and the instant the reverse recovery current decays to 10 % of its reverse recovery peak value I_R. Most commercially available switching diodes have t_{rr} in the range from 1 ns to 1 μs. The reverse recovery time t_{rr} consists of two time intervals: the *storage time* t_s and the *transition time* t_t,

$$t_{rr} = t_s + t_t. \tag{15.75}$$

At time $t = 0$, the diode begins to turn off. Since the excess charge in the diode cannot change instantaneously, the excess carrier concentrations at the edges of the depletion region are positive, and therefore the diode voltage is also positive, the junction is forward biased, and the diode current decreases from positive to negative. The negative diode current reduces the excess carrier concentrations. At time t_s, the excess carrier concentrations at the edges of the depletion region reach zero, the stored charge $Q(t_s)$ is zero, and the diode voltage $v_D(t_s)$ is zero. The product of the diode current and voltage $p_D(t) = i_D v_D$ during the storage time t_s is very low and negative because the diode voltage v_D is low (between 0.7 V and 0 V) and the diode current i_D is negative. The storage time t_s increases with increasing

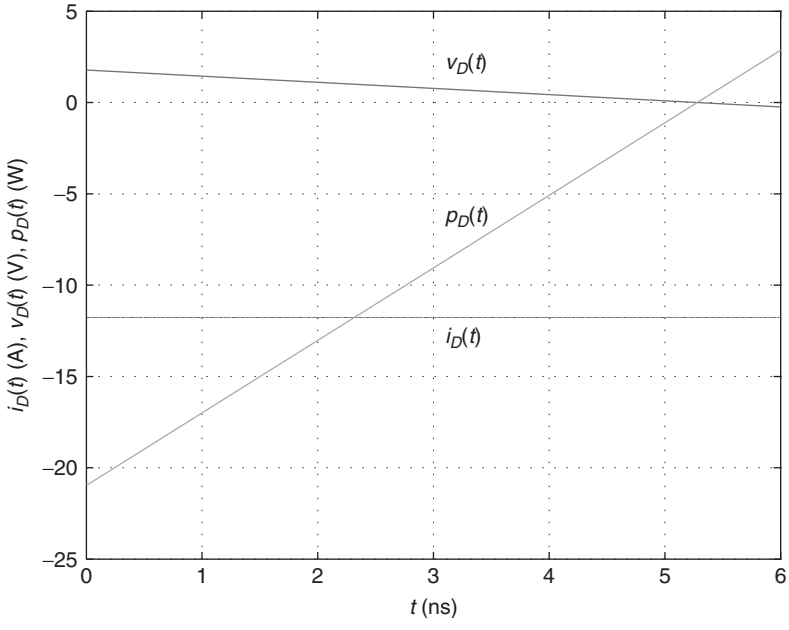


Figure 15.22 Waveforms for pn junction diode during the storage time t_s.

temperature T. The storage time t_s can be reduced by adding recombination centers to the bulk regions. For silicon, a gold atom doping of $10^{14}\,\text{cm}^{-3}$ can reduce the recombination time constant τ_p, for example, from 100 ns to 1 ns. Figure 15.22 depicts the waveforms during the storage time t_s. Figure 15.23 shows the waveform of the excess minority charge Q_p during the storage time t_s.

Once the excess carriers are no longer present at the end of storage time interval t_s, the diode begins to enter the reverse-bias region. During time t_t, the diode voltage v_D decreases from zero to V_R, the diode is OFF, and the current flows through the diode junction nonlinear capacitance, until the capacitance is fully charged. This current flows through the equivalent resistance of the charging path, causing the turn-off switching loss. For a linear capacitance, both the capacitance voltage and current are exponential functions during the time interval t_t. However, the junction nonlinear capacitance is large, when the diode voltage is close to zero and the diode voltage changes more slowly than that of the linear capacitance. On the other hand, the junction capacitance is small, when the diode voltage is close to the steady-state value V_R and the diode voltage changes faster than for the linear capacitance. Waveforms during the transient time t_t are shown in Figure 15.24. The maximum value of the instantaneous dissipated power is equal to $I_R V_R/4$.

15.10.3 Charge-continuity Equation

The process of storing charge in pn junction diodes is not the same as that of capacitors. The charge in the diode can be created by hole–electron pair generation and can disappear due to recombination. The reverse recovery process of p^+n junction diodes during the storage

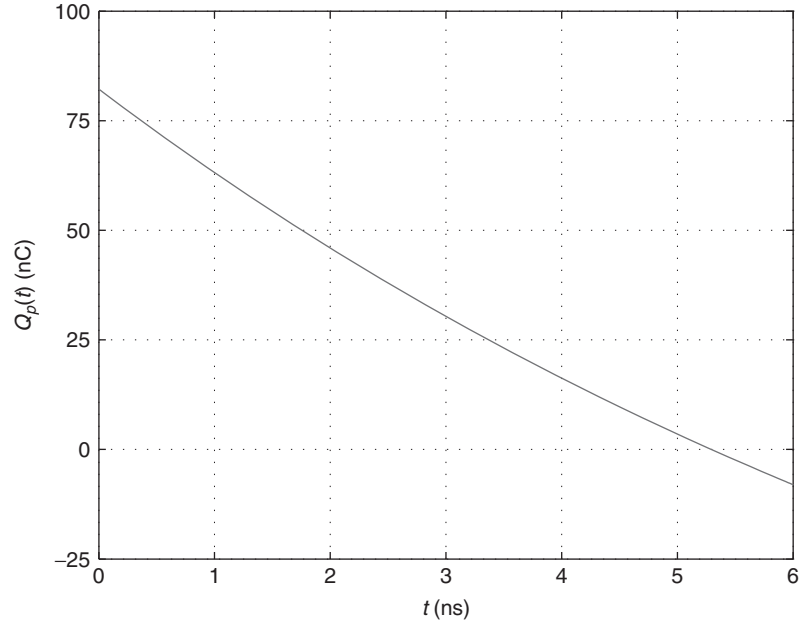


Figure 15.23 Waveform of the excess minority charge Q_p for pn junction diode during the storage time t_s.

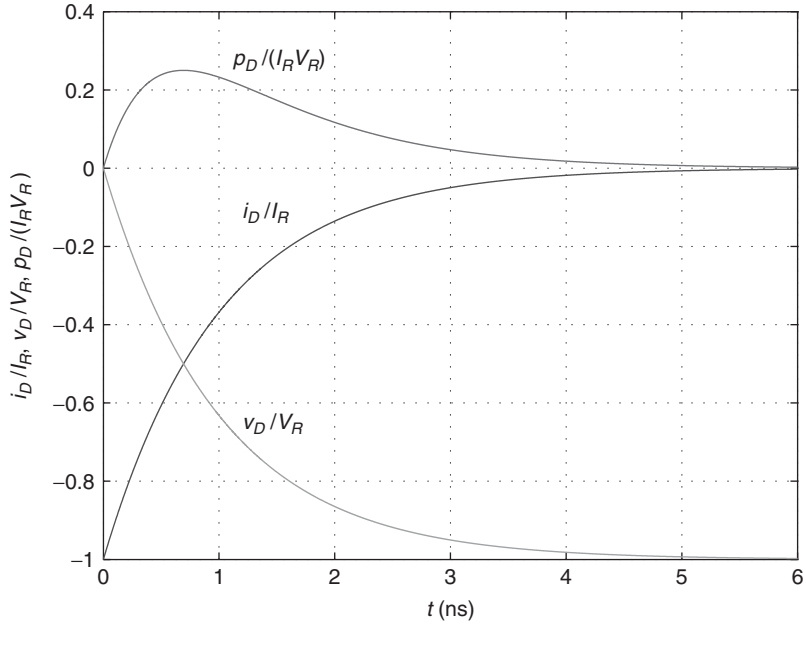


Figure 15.24 Waveforms for pn junction diode during the transient time t_t.

time interval t_s is described by the *charge-continuity equation*, also called the *charge-control equation*

$$i_D(t) = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt} \tag{15.76}$$

where $Q_p(t)$ is the excess minority hole charge stored in the n-bulk region adjacent to the depletion region edge and τ_p is the average hole lifetime in the n-region, also called the mean recombination time of minority holes. The term $Q_p(t)/\tau_p$ describes the recombination and generation of hole–electron pairs, and the term $dQ_p(t)/dt = i_D - Q_p(t)/\tau_p$ describes in the change in the stored minority excess hole charge due to the net carrier flow out from the quasi-neutral region [8]. If

$$\frac{dQ_p(t)}{dt} \ll \frac{Q_p}{\tau_p} \tag{15.77}$$

the charge-continuity equation simplifies to

$$Q_p(t) \approx \tau_p i_D(t). \tag{15.78}$$

In this case, the charge is proportional to the diode current. The diode current supplies the holes to the quasi-neutral n-bulk region at the same rate as they are being lost by recombination in the n-bulk region, whereas the current associated with the rate of change of the excess hole charge is negligible. The entire amount of charge Q_p recombines and must be replenished every τ_p nanoseconds. The total diode current is approximately equal to the hole current injected across the junction. The diode is in a quasi-static steady state. This situation usually occurs when the diode current is constant and the excess charge is in steady state (long after the turn-on transition) or the ac diode current is slowly varying, for example, a half sinusoidal diode current at low frequencies $f < 1/(20\pi\tau_p)$. The condition for low-frequency operation can be expressed by $\omega\tau_p \ll 0.1$. The storage time t_s for slowly varying diode current waveforms with low di_D/dt at all times is nearly zero. That is why zero-current switching of diodes is desirable. If

$$\frac{dQ_p(t)}{dt} \gg \frac{Q_p}{\tau_p}, \tag{15.79}$$

the charge-continuity equation becomes

$$i_D(t) \approx \frac{dQ_p(t)}{dt}. \tag{15.80}$$

In this case, the diode current is equal to the rate of change of the charge, whereas the recombination current is negligible. Solutions of (15.76) are given in [8] for selected waveforms of i_D.

When the diode is driven by a square-wave voltage, the charge equation for the storage time interval becomes

$$I_R = \frac{Q_p(t)}{\tau_p} + \frac{dQ_p(t)}{dt}. \tag{15.81}$$

This equation in the s-domain is given by

$$\frac{I_R}{s} = \frac{Q_p(s)}{\tau_p} + sQ_p(s) - Q_p(0). \tag{15.82}$$

Assuming that the excess charge waveform has reached the steady-state value before the beginning of the turn-off transition, the charge initial value is $Q_p(0) = \tau_p I_F$. Rearrangement of (15.82) produces

$$Q_p(s) = \frac{\tau_p I_F}{s + \dfrac{1}{\tau_p}} + \frac{I_R}{s\left(s + \dfrac{1}{\tau_p}\right)}. \tag{15.83}$$

Hence,

$$Q_p(t) = \tau_p I_F e^{-\frac{t}{\tau_p}} + \tau_p I_R(1 - e^{-\frac{t}{\tau_p}}) = \tau_p I_R + \tau_p(I_F - I_R)e^{-\frac{t}{\tau_p}}. \tag{15.84}$$

Imposing the condition $Q_p(t_s) = 0$, one obtains the storage time

$$t_s = \tau_p \ln\left(1 - \frac{I_F}{I_R}\right) = \tau_p \ln\left(1 + \frac{I_F}{|I_R|}\right). \tag{15.85}$$

The storage time t_s decreases when $I_F/|I_R|$ decreases.

15.10.4 Reverse Recovery in Inductive Circuits

In many applications, the rate of the diode current change di_F/dt is limited during the turn-off transition by an external circuit, such as an inductor connected in series with the diode. For example, this situation is present in PWM dc–dc converters. Figure 15.25 shows the diode current and voltage waveforms of a pn junction diode during the reverse recovery for a finite rate of change of the diode current di_F/dt. The dynamic $i_D - v_D$ diode characteristic during the turn-off transition in inductive circuits is depicted in Figure 15.26. When forward current is ramped down at a high rate of di_F/dt to zero, current flow does not come to an ideal stop. Instead the current briefly reverses its flow and continues with the same slope until a peak value I_R is reached. It will diminish thereafter to nearly zero, that is, to the saturation level $-I_S$. During the storage time t_s the high reverse blocking voltage does not start appearing until the reverse current peak I_R occurs. As the slope $|di_F/dt|$ decreases, the magnitude of the peak reverse current $|I_R|$ also decreases, as shown in Figure 15.27.

The *softness factor* or *snappiness factor* is defined as the ratio of the transient time t_t to the storage time t_s,

$$S = \frac{t_t}{t_s}. \tag{15.86}$$

A diode with $S \geq 1$ is called a *soft recovery diode* and a diode with $S < 1$ is called a *fast recovery diode*, *snappy recovery diode*, or *abrupt diode*. The time t_s is

$$t_s = t_{rr} - t_t = t_{rr} - St_s, \tag{15.87}$$

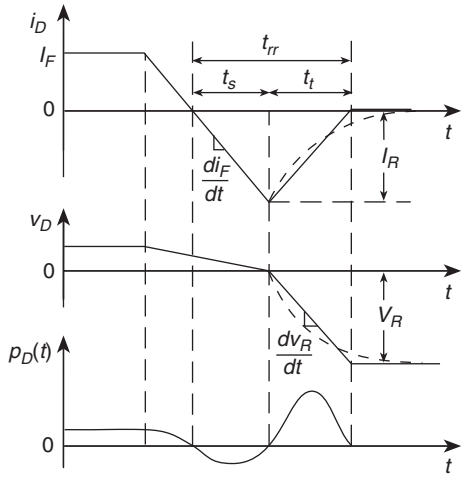


Figure 15.25 Idealized current and voltage waveforms of a pn junction diode illustrating the reverse recovery in inductive circuits.

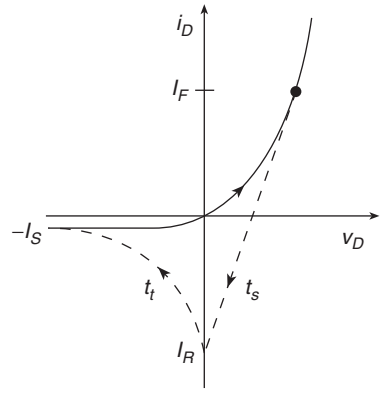


Figure 15.26 Dynamic $i_D - v_D$ diode characteristic during the turn-off transition in inductive circuits.

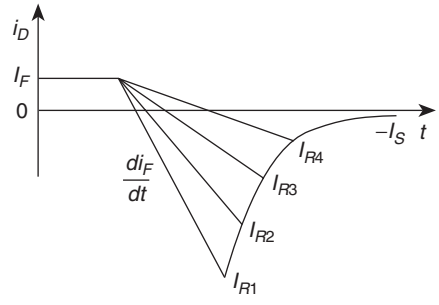


Figure 15.27 Dependence of the peak reverse recovery diode current I_R on the slope $|di_F/dt|$ during the turn-off transition in inductive circuits.

resulting in

$$t_s = \frac{t_{rr}}{S+1} \tag{15.88}$$

and

$$t_t = t_{rr} - t_s = \frac{St_{rr}}{S+1}. \tag{15.89}$$

The peak reverse current is given by

$$I_R = \left(\frac{di_F}{dt}\right) t_s = \left(\frac{di_F}{dt}\right) \frac{t_{rr}}{S+1}. \tag{15.90}$$

The reverse recovery charge stored in the diode, when the diode current is negative, is found to be

$$Q_{rr} = \frac{I_R t_{rr}}{2} = \left(\frac{di_F}{dt}\right) \frac{t_{rr}^2}{2(S+1)}, \tag{15.91}$$

which gives

$$t_{rr} = \sqrt{\frac{2(S+1)Q_{rr}}{\frac{di_F}{dt}}}. \tag{15.92}$$

Substituting (15.92) into (15.90) yields the peak reverse current

$$I_R = \sqrt{\frac{2Q_{rr}\left(\frac{di_F}{dt}\right)}{S+1}}. \tag{15.93}$$

As $|di_F/dt|$ decreases, $|I_R|$ and $|Q_{rr}|$ also decrease [8]. For example, 600 V silicon pn junction diodes have the reverse recovery charge $Q_{rr} = 100$ to 500 nC and the reverse recovery time $t_{rr} \approx 100$ ns. For 600 V ultrafast recovery pn junction diodes, $Q_{rr} \approx 100$ nC. The reverse recovery charge Q_{rr} increases significantly with temperature T, forward current I_F, and di_F/dt.

The charge stored in the diode during time interval t_t is

$$Q_b = \frac{I_R t_t}{2} = \frac{1}{2}\left(\frac{di_F}{dt}\right)\frac{St_{rr}^2}{(S+1)^2}. \tag{15.94}$$

The diode current and voltage waveforms during time interval t_t can be approximated by

$$i_D \approx I_R - \frac{I_R}{t_t}t = I_R\left(1 - \frac{t}{t_t}\right) \tag{15.95}$$

and

$$v_D \approx \frac{V_R}{t_t}t, \tag{15.96}$$

where $I_R < 0$ and $V_R < 0$. The instantaneous power loss during time interval t_t is given by

$$p_D(t) = i_D v_D = \frac{V_R I_R}{t_t}\left(t - \frac{t^2}{t_t}\right), \tag{15.97}$$

resulting in the average power dissipated during time interval t_t,

$$P_{RR} = \frac{1}{T}\int_0^{t_t} p_D\, dt = \frac{f_s V_R I_R t_t}{6} = \frac{f_s V_R S}{6}\left(\frac{di_F}{dt}\right)\left(\frac{t_{rr}}{S+1}\right)^2. \tag{15.98}$$

As $|di_F/dt|$ decreases, the power P_{RR} also decreases. Reverse recovery causes switching loss in the diode, increases current stress in the diodes and in other devices connected to the same node (except inductors), and increases harmonics and the level of conducted and radiated electromagnetic interference.

All these adverse effects can be reduced by slowing down the turn-off rate $|di_F/dt|$. The switching power loss in Si pn junction diodes increases dramatically with temperature due to the increase in peak reverse current.

15.11 Schottky Diodes

Diodes made with a rectifying metal-semiconductor junction are called Schottky diodes or Schottky barrier diodes; they are majority carrier devices, and the diffusion of minority charge carriers is negligible. The physical structure of a Schottky diode is depicted in Figure 15.28. The semiconductor is usually an n-type material because of the higher mobility of electrons than of holes. The semiconductor is lightly doped to form a rectifying contact. The doping level of the n^- type semiconductor is very low; typically, $N_D = 10^{14}$ to $10^{16}\,cm^{-3}$ for silicon. The doping level on the cathode side is very high to form a nonrectifying ohmic contact between metal and n^+ type semiconductor. The metal is aluminum, platinum, chrome, molybdenum, tungsten, nickel, or titanium. A thin metal film

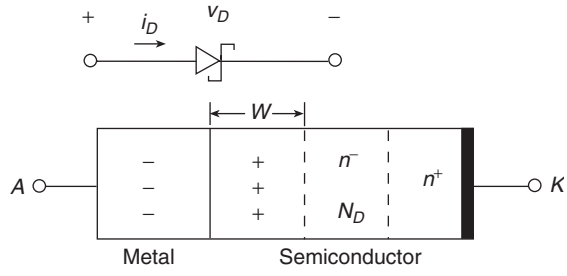


Figure 15.28 Physical structure of Schottky diode.

is usually deposited on an n-type semiconductor. Electrons from the n-type semiconductor flow into the metal, as they would flow into the acceptor semiconductor in the p^+n junction diode, where the p^+ region is heavily doped and behaves like a conductor. The forward current is due to injection of the majority charge carriers (i.e., electrons) from the n-type semiconductor into the metal. The flow of electrons into the metal leaves a region in the semiconductor adjacent to the metal–semiconductor interface that is depleted of carriers as in the pn junction, forming a depletion region. The depletion region is only formed on the semiconductor side. Schottky diodes are unique because the conduction is entirely by majority charge carriers. The current in Schottky diodes has only the drift component. Majority charge carriers move or *drift* in response to the electric field. Therefore, there is no need to accumulate or remove excess carriers. This eliminates the forward and reverse recovery phenomena. However, reverse-biased Schottky diodes have much higher leakage current than the corresponding pn junction diodes.

A typical commercial Schottky diode consists of a rectifying metal–semiconductor contact deposited on an optimally designed n^- epitaxial layer (a drift region), an edge termination, a highly doped substrate, and a backside ohmic contact. The cross-section of a silicon carbide Schottky diode is depicted in Figure 15.29 [11]. The diode was designed for a maximum forward current of 6 A and a breakdown voltage of 1200 V. The thickness of the lightly doped n^- epilayer is 10 μm and the doping concentration is $N_D = 2.7 \times 10^{15}\,\text{cm}^{-3}$. The n^+ substrate and the metal form an ohmic nonrectifying contact. The thickness of the substrate is typically 500 μm. The diode diameter is 3 mm. The top-side nickel thickness is

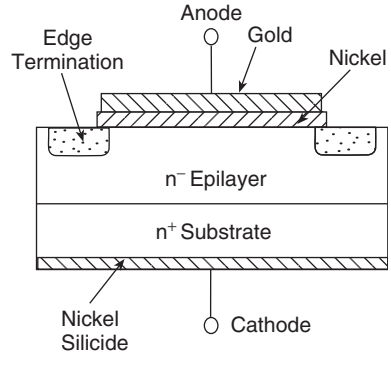


Figure 15.29 Cross-section of silicon carbide Schottky diode.

0.1 μm. A 1 μm thick gold plating layer is deposited on top of the nickel contact by electron beam evaporation to minimize the spreading resistance. Boron is implanted in a 100 μm ring around the device as a resistive edge termination to achieve a nearly ideal breakdown voltage.

The series resistance R_S of Schottky diodes consists of a lightly doped n^- region and a heavily doped n^+ substrate. For low-voltage devices, these two resistances are comparable because the heavily doped substate is much (usually two orders of magnitude) longer than the lightly doped n^- region. For high-voltage devices, the resistance of the n^- region is much higher than that of the substrate because the n^- region is long and has a low doping concentration N_D. For example, $R_S = 46.641\,\text{m}\Omega$ for a silicon carbide CSD10060 Schottky diode.

Conductivity modulation is not present in Schottky diodes to reduce the resistance during conduction of forward current. Therefore, silicon Schottky diodes with high voltage ratings are not made. In contrast, silicon carbide Schottky diodes may have high voltage ratings, above 1 kV.

The breakdown voltage of Schottky diodes is due to the avalanche effect caused by a high peak electric field intensity E_m at the metal–semiconductor interface. The avalanche current may damage the metal–semiconductor contact. Therefore, all Schottky diodes have guard or field rings surrounding the metal–semiconductor contact. The rings are made of p^+ diffusions that form p^+n junctions. Schottky diodes are designed in such a way that the avalanche breakdown voltage of the p^+n junction of the ring guard is higher than that of the Schottky metal–semiconductor junction.

15.11.1 Static I–V Characteristic of Schottky Diodes

The equation for the dc $I-V$ characteristic of Schottky diodes is similar to that of the pn junction diodes:

$$I_D = A_J D T^2 e^{-\frac{\phi_B}{V_T}} \left(e^{\frac{V_D}{nV_T}} - 1 \right) = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right). \tag{15.99}$$

The saturation current is determined by a different equation than that of the pn junction diodes,

$$I_S = A_J D T^2 e^{-\frac{\phi_B}{V_T}}, \tag{15.100}$$

where D is the effective Richardson constant and ϕ_B is the potential barrier height for electron injection from the metal to the semiconductor. It depends on the work function of the metal contact. For silicon, $D = 120\,\text{A/cm}^2\text{K}^2$) and for an aluminum to n-type silicon (Al-Si) junction, $\phi_B = 0.7\,\text{V}$. The reverse saturation current I_S is of the order of $10^{-7}\,\text{A}$. It is usually four to six orders of magnitude larger than that of the pn bipolar junction diodes with the same junction area A_J. Therefore, the forward voltage drop is 0.25 to 0.35 V lower than that of pn junction diodes with the same current density $J_D = I_D/A_J$. The typical maximum current density of silicon Schottky diodes is $J_{Dmax} = 100\,\text{A/cm}^2$.

The threshold voltage is $V_F = 0.3$ to 0.4 V for silicon Schottky diodes and is $V_F = 1.5$ to 2 V for silicon carbide Schottky diodes. The threshold voltage V_F decreases as the junction temperature T increases. For SiC Schottky diodes, the thermal coefficient of V_F is

$$\delta_{T(SiC)} = \frac{\Delta V_F}{\Delta T} = -0.64\,\text{mV}/^\circ\text{C}. \tag{15.101}$$

The reverse-biased Si Schottky diode has a reverse leakage current that is larger than that of a Si pn junction diode with the same junction area A_J. This current increases

with temperature. The temperature coefficient for the saturation current of Si Schottky diodes is

$$\gamma_s = \frac{\frac{\Delta I_S}{I_S}}{\Delta T} = \frac{2q\phi_B}{kT^3} \approx 10\,\%/\text{K}, \qquad \text{for } T = 300\,\text{K}. \tag{15.102}$$

Schottky diodes exhibit nearly zero reverse recovery because there is no need to remove excess carriers as the current flows only by drift. The peak reverse recovery current I_R of silicon diodes is much higher than that of the SiC diodes. The current I_R increases with increasing temperature for Si diodes, but it remains nearly constant for SiC diodes. The reverse breakdown voltage of Si Schottky diodes is low, typically below 50–200 V. In contrast, the breakdown voltage of SiC Schottky diodes is high, typically in the range of 300–1200 V. Schottky diodes find applications in high-power, fast-switching power circuits. The threshold voltage of SiC Schottky diodes V_F decreases with temperature. The forward resistance R_F of these diodes increases with temperature due to the reduction in the mobility at elevated temperatures. Therefore, many diodes can be connected in parallel without any unequal current sharing issues. Silicon Schottky diodes are attractive in low-voltage applications because of the low forward voltage V_F, whereas SiC diodes are attractive in high-voltage, high-frequency, high-temperature applications because of their high breakdown voltage and high speed. The typical turn-off time $t_{off} = t_t$ of SiC Schottky diodes is less than 50 ns, even at high junction operating temperature T_J. Typically, $t_{rr(Si)}/t_{rr(SiC)} = 1000$.

15.11.2 Junction Capacitance of Schottky Diodes

The depletion region width of Schottky diodes is

$$W = x_n = \sqrt{\frac{2\epsilon(V_{bi} - v_D)}{qN_D}}. \tag{15.103}$$

Hence, the junction capacitance is

$$C_J = \epsilon\frac{A_J}{W} = A_J\sqrt{\frac{\epsilon qN_D}{2V_{bi}\left(1 - \frac{v_D}{V_{bi}}\right)}} = \frac{C_{J0}}{\sqrt{1 - \frac{v_D}{V_{bi}}}}, \tag{15.104}$$

where

$$C_{J0} = A_J\sqrt{\frac{\epsilon qN_D}{2V_{bi}}}. \tag{15.105}$$

Ideally, Schottky diodes do not exhibit reverse recovery. Therefore, the turn-off transient behavior of these diodes is determined by the junction capacitance C_J. The diffusion capacitance C_D is zero and therefore the storage time t_s is zero. In reality, the lifetime of the minority carriers is very short. For example, $\tau = 14.474 \approx 15$ ps for a silicon carbide CSD10060 Schottky diode. The diode model in the off-state is the junction capacitance C_J. For example, $C_{j0} = 381.44$ pF, $V_{bi} = 9.99$ V, and $m = 0.63338$ for a silicon carbide CSD10060 Schottky diode.

A simple circuit for investigating off-to-on and on-to-off transitions in Schottky diodes is shown in Figure 15.18. Figure 15.30 depicts idealized waveforms illustrating turn-off and turn-on transitions due to junction capacitance. To gain some insight into dynamics of Schottky diodes, assume that the junction capacitance C_J is linear.

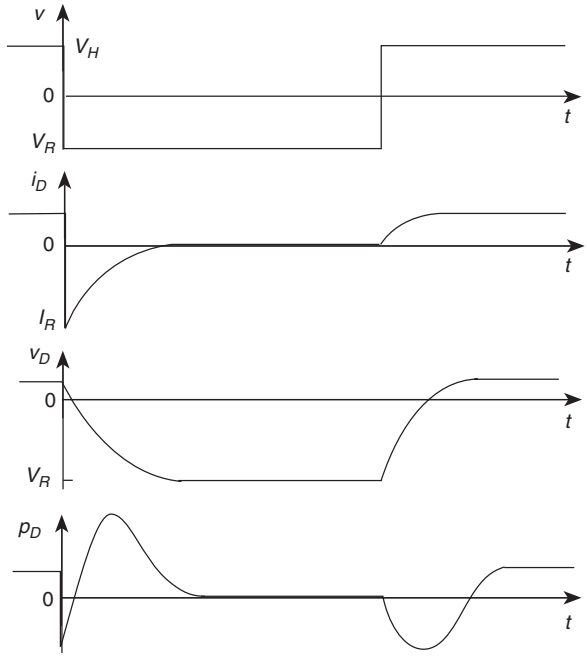


Figure 15.30 Waveforms of Schottky diodes illustrating the transitions.

15.11.3 Switching Characteristics of Schottky Diodes

Let us consider the turn-off transition, when the junction capacitance is charged and the diode voltage decreases from V_F to V_R. At $t = 0$, the input voltage v is switched from V_H to V_R. For $t > 0$, the diode current, voltage, and instantaneous power waveforms are given by

$$i_D = I_R e^{-\frac{t}{\tau}}, \tag{15.106}$$

$$v_D = V_F + (V_R - V_F)\left(1 - e^{-\frac{t}{\tau}}\right) \approx V_R\left(1 - e^{-\frac{t}{\tau}}\right), \tag{15.107}$$

and

$$p_D(t) = i_D v_D = I_R V_R e^{-\frac{t}{\tau}}\left(1 - e^{-\frac{t}{\tau}}\right) = I_R V_R\left(e^{-\frac{t}{\tau}} - e^{-\frac{2t}{\tau}}\right), \tag{15.108}$$

where $\tau = C_J R$ is the time constant, R is the resistance in the junction capacitance charging path, including the diode series resistance R_S, and

$$I_R = \frac{V_R - V_F}{R}. \tag{15.109}$$

The series resistance R_S consists of the spreading resistance of Schottky metal, the drift region resistance, the substrate resistance, the backside resistance, the bond wire resistance, and the package resistance. The average power transferred from the input voltage source v to the diode during the turn-off transition is given by

$$P_D = \frac{1}{T}\int_0^\infty p_D\, dt = \frac{I_R V_R}{T}\int_0^\infty \left(e^{-\frac{t}{\tau}} - e^{-\frac{2t}{\tau}}\right) dt = \frac{I_R V_R \tau}{2T} = \frac{V_R(V_R - V_F)RC_J}{2TR}$$

$$\approx \frac{f_s C_J V_R^2}{2}, \tag{15.110}$$

for $|V_R| \gg V_F$, where $f_s = 1/T$ is the switching frequency. The energy corresponding to this power is stored in the junction capacitance C_J. The power delivered from the input voltage source v to the R–C_J circuit during the turn-off transition is

$$P_I = \frac{1}{T}\int_0^\infty v i_D \, dt = \frac{V_R}{T}\int_0^\infty i_D \, dt = \frac{V_R}{T} Q_{CJ} = \frac{V_R}{T} C_J V_R = f_s C_J V_R^2. \tag{15.111}$$

The switching power loss in the charging path resistor R during the turn-off transition is

$$P_R = P_I - P_D = \frac{1}{2} f_s C_J V_R^2. \tag{15.112}$$

Figure 15.31 shows the waveforms of the diode current i_D, the diode voltage v_D, and the diode power p_D for the Schottky diode during the turn-off transition at $V_H = 10\,\text{V}$, $V_R = -10\,\text{V}$, $V_F = 1.78\,\text{V}$, $R = 1\,\Omega$, $C_J = 10\,\text{ns}$, and $\tau = 10\,\text{ns}$.

Next, let us consider the turn-on transition, when the junction capacitor is discharged and the diode voltage increases from V_R to V_F. The diode current, voltage, and instantaneous power waveforms are given by

$$i_D = I_F \left(1 - e^{-\frac{t}{\tau}}\right), \tag{15.113}$$

$$v_D = V_F + (V_R - V_F)e^{-\frac{t}{\tau}} \approx V_R e^{-\frac{t}{\tau}}, \tag{15.114}$$

and

$$p_D(t) = i_D v_D = I_F V_R e^{-\frac{t}{\tau}} \left(1 - e^{-\frac{t}{\tau}}\right) = I_F V_R \left(e^{-\frac{t}{\tau}} - e^{-\frac{2t}{\tau}}\right), \tag{15.115}$$

where

$$I_F = \frac{V_H - V_F}{R}. \tag{15.116}$$

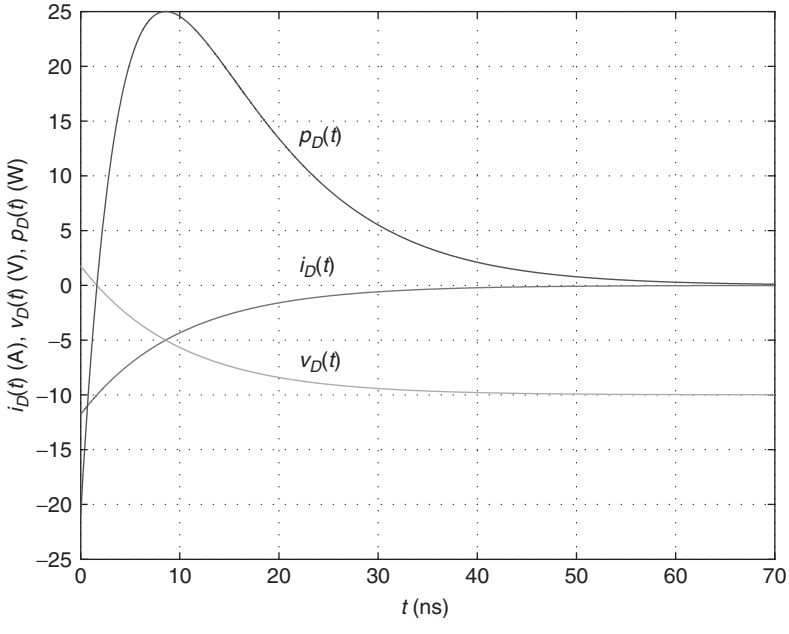


Figure 15.31 Waveforms for Schottky diodes during turn-off transition.

The average power lost during the turn-on transition is given by

$$P_D = \frac{1}{T}\int_0^\infty p_D\,dt = \frac{I_F V_R}{T}\int_0^\infty \left(e^{-\frac{t}{\tau}} - e^{-\frac{2t}{\tau}}\right) dt = \frac{I_F V_R \tau}{2T} = \frac{V_R(V_H - V_F)RC_J}{2TR}$$

$$= \frac{1}{2} f_s C_J V_R (V_H - V_F). \tag{15.117}$$

The energy stored in the junction capacitance C_J during the time interval when the diode is in the off-state is lost during the turn-on transition. Therefore, the turn-on switching power loss is given by

$$P_{turn\text{-}on} = \frac{1}{2} f_s C_J V_R^2. \tag{15.118}$$

Figure 15.32 shows the waveforms of i_D, v_D, and p_D for the Schottky diode during the turn-on transition for $V_H = 10\,\text{V}$, $V_R = -10\,\text{V}$, $V_F = 1.78\,\text{V}$, $R = 1\,\Omega$, and $\tau_p = 10\,\text{ns}$.

In summary, the total switching power loss during both the turn-off and turn-on transitions is given by

$$P_{sw} \approx f_s C_J V_R^2. \tag{15.119}$$

For SiC Schottky diodes, the transient current and the switching power loss are independent of temperature. In reality, the junction capacitance C_J is nonlinear and the transition processes are more complex. The junction capacitance is large at low diode voltages and low at high reverse voltages. Therefore, the diode voltage changes more slowly when the diode voltage is close to zero and more rapidly when the diode voltage is close to V_R as compared to the case with a linear junction capacitance.

High-voltage Schottky diodes store minority carrier charge in lightly doped regions and suffer slightly from reverse recovery. In contrast, low-voltage Schottky diodes store very little minority charge and exhibit no significant reverse recovery current. A typical value of the transient time τ for Schottky diodes is 10 ps.

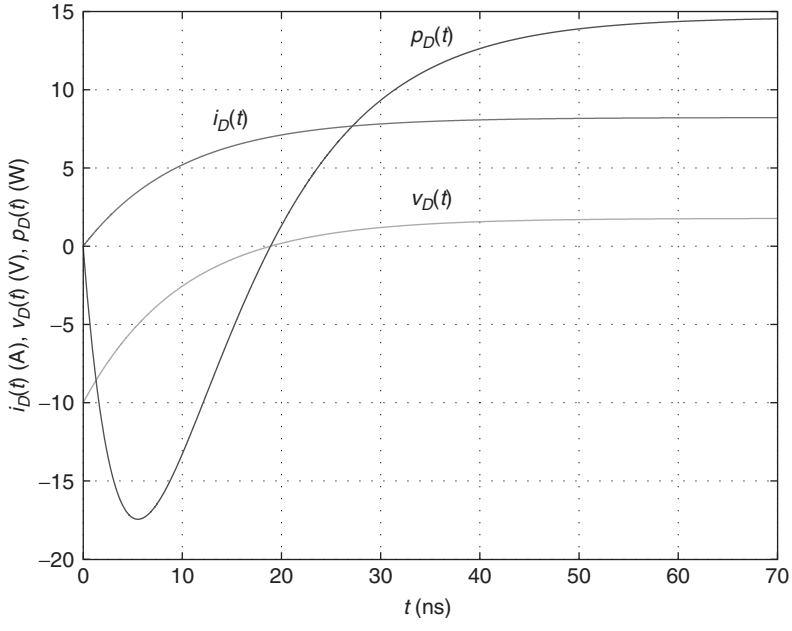


Figure 15.32 Waveforms for Schottky diodes during turn-on transition.

15.12 SPICE Model of Diodes

Figure 15.33 shows a SPICE large-signal model for diodes. The diode SPICE model parameters are given in Table 15.2. The diode dc characteristic in SPICE is given by

$$I_D = I_N + I_B, \tag{15.120}$$

in which the diode current for the forward- and reverse-bias regions is

$$I_N = I_S \left(e^{\frac{V_D}{NV_T}} - 1 \right) \tag{15.121}$$

and the diode current in the breakdown region is

$$I_B = IBVe^{\frac{-BV-V_D}{V_T}}, \tag{15.122}$$

where the *thermal potential* is

$$V_T = \frac{kT}{q} \tag{15.123}$$

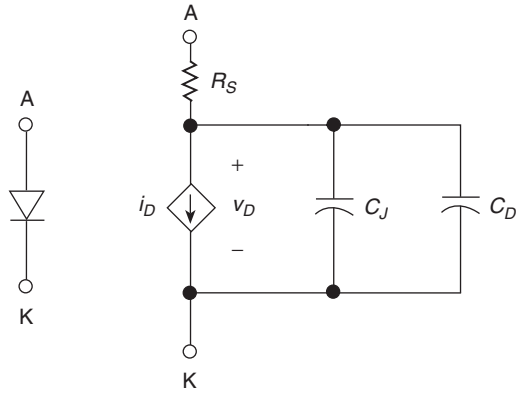


Figure 15.33 SPICE large-signal model for diodes.

Table 15.2 SPICE diode large-signal model parameters

Symbol	SPICE Symbol	Model Parameter	Default value	Typical value
I_S	IS	Saturation current	10^{-14} A	10 nA
n	N	Emission coefficient	1	1.1 to 1.8
r_S	RS	Series resistance	0	0.1 Ω
V_{BR}	BV	Reverse breakdown voltage	∞	100 V
I_{BR}	IBV	Reverse breakdown current	10^{-10} A	100 μA
C_{J0}	CJ0	Zero-bias C_J	0	1 nF
V_{bi}	VJ	Junction potential	1 V	0.8 V
m	M	Grading coefficient	0.5	0.33 to 0.5
E_g	EG	Band gap energy	1.11 eV	1.11 eV
F_C	FC	Forward-biased C_J coeff.	0.5	0.5
τ	TT	Transit time	0	150 ns
x	XTI	IS temperature exponent	3	3
K_F	KF	Flicker noise coefficient	0	0
A_F	AF	Flicker noise exponent	1	1

and the dependence of the saturation current on temperature T is described by

$$I_S = IS \left(\frac{T}{T_{nom}}\right)^{\frac{XTI}{N}} \exp\left(\frac{EG}{NV_T}\ \frac{T - T_{nom}}{T_{nom}}\right). \tag{15.124}$$

In the above equations, I_S is the *saturation current* at $T = T_{nom}$, $k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, $q = 1.602 \times 10^{-26}$ C is the magnitude of the electron charge, $T = 273\,\text{K} +$ temperature in °C is the temperature in kelvin, and $N = 1$ to 2 is the *emission coefficient*. For $T = 25°\text{C}$, $V_T = kT/q = T/11{,}609 = 25.7\,\text{mV}$. Typically, $I_S = 10^{-14}$ A for Si small-signal junction diodes and $I_S = 10^{-11}$ to 10^{-7} A for Si power junction diodes. For Si Schottky diodes, the typical value of I_S is 10^{-7} A. For silicon carbide Schottky diodes, I_S is in the range 10^{-15} to 10^{-21} A.

The diode junction capacitance is given by

$$C_J = \frac{CJ0}{\left(1 - \frac{v_D}{VJ}\right)^M} \tag{15.125}$$

where $VJ = 0.55$ to 1 V is the built-in potential and $M = 1/3$ to 1/2 is the *grading coefficient*. The diffusion capacitance is

$$C_D = TT\frac{i_D}{NV_T}. \tag{15.126}$$

Note, finally, that the diode topology syntax takes the form

Dxxxx A K model-name

for example

D1N9999 1 0 10A-diode

The SPICE diode model syntax takes the form

.model diode-model-name D (SPICE diode parameters)

for example

.model 10A-diode D(Is = 100 nA n = 1.666 Rs = 0.02 Ohm BV = 100 V IBV
= 100 nA CJ0 = 1 nF TT = 12 ns)

15.13 Summary

- The resistivity of semiconductors is in the range $10^{-3}\,\Omega\text{cm} \le \rho \le 10^{6}\,\Omega\text{cm}$. At $T = 300$ K, the resistivity of the intrinsic silicon is $\rho_{Si} = 2.26 \times 10^5\ \Omega\text{cm}$ and the conductivity of the intrinsic silicon is $\sigma_{Si} = qn\mu_n + qn\mu_p = 4.4 \times 10^{-6}\ (\Omega\text{cm})^{-1}$. For comparison, the conductivity of copper is $\sigma_{Cu} = 5.8 \times 10^7\ (\Omega\text{cm})^{-1}$. Thus, the conductivity of silicon is 11 orders of magnitude lower than that of copper.
- A missing electron in a semiconductor is equivalent to a hole.
- In intrinsic semiconductors, the electron and hole concentrations are equal, that is, $n = p = n_i = p_i$.
- In extrinsic semiconductors, the concentrations of electrons and holes are not equal ($n \neq p$).

- At sufficiently high temperatures, all semiconductors (including doped semiconductors) become intrinsic.
- The depletion layer extends deeper into the more lightly doped semiconductor in pn junctions.
- Avalanche breakdown is caused by impact ionization and begins when the initiating electron has enough energy to knock an electron from the valence band to the conduction band.
- Silicon carbide has a large band gap energy, high breakdown electrical field intensity, and high thermal conductivity.
- The breakdown electric field intensity E_{BD} increases with increasing band gap energy E_G. The avalanche breakdown voltage V_{BD} increases with the band gap energy E_G.
- A higher breakdown diode voltage requires a longer lightly doped region and a lower doping concentration.
- Doping levels below $10^{15}\,\text{cm}^{-3}$ are necessary to achieve high breakdown voltages.
- Silicon carbide diodes are capable of delivering large currents and withstanding high voltages, without the need for sophisticated cooling systems.
- The breakdown voltage of silicon carbide junction diodes is about 11 times higher than that of the silicon junction diodes at the same doping concentration.
- Silicon carbide has a higher band gap energy E_G, breakdown (critical) electric field E_{DB}, thermal conductivity, and drift saturation velocity v_{sat} than silicon. In addition, silicon carbide devices have the inherent ability to operate at higher junction temperature (up to 600°C) because of their low intrinsic carrier concentration.
- An effective edge termination technique makes the electric field distribution uniform at the edge of the device in order to approach the ideal breakdown voltage capability.
- The breakdown voltage of diodes can be increased by using guard rings and field plate terminations to reduce concentrations of the electric field at depletion region corners and chip edges.
- The breakdown voltage is reduced by defects in the semiconductor structure, especially at the surface and around the corners.
- The threshold voltage V_F is 0.3 V for silicon Schottky diodes, 0.7 V for silicon pn junction diodes, 1 V for silicon carbide Schottky diodes, and 2.8 V for silicon carbide pn junction diodes.
- Silicon carbide Schottky diodes can be used in high-voltage, high-temperature, high-frequency applications.
- The junction capacitance C_J is identical to a parallel-plate capacitor with its electrodes separated by the depletion region width $W(V_D)$ at a particular dc diode voltage V_D.
- The junction and diffusion capacitances prevent the diode from turning on and off instantaneously.
- When a forward bias is applied suddenly to a pn junction, a charge is supplied to the depletion region and the neutral regions.

- Junction diodes suffer from reverse recovery. There are two mechanisms for removing the excess minority charge stored in the quasi-neutral regions adjacent to the edges of the depletion region: reverse current flow and recombination.
- The minority carrer lifetime τ_p or τ_n can be reduced by adding recombination centers; adding gold atoms to silicon increases the recombination rate. This reduces the storage time t_s.
- Reverse recovery causes switching loss in the diode, high reverse current spikes in the diode and other components (except inductors) connected to the same node, and generates a broad spectrum of harmonics, reducing electromagnetic compatibility performance. Switching loss P_{RR}, peak reverse current I_R, and EMI level can be reduced by slowing down the turn-off rate $|di_F/dt|$.
- The forward current in Schottky diodes is due to the injection of majority charge carriers from silicon into metal. Therefore Schottky diodes are majority devices.
- Schottky diodes show less dependence on temperature than pn junction diodes.
- The switching loss in silicon diodes increases dramatically with temperature, whereas it remains essentially unchanged for silicon carbide diodes.
- Low-voltage Schottky diodes virtually do not exhibit reverse recovery, whereas high-voltage Schottky diodes store some minority charge in the lightly doped region, causing a small effect of reverse recovery (much smaller than in pn junction diodes). Silicon carbide Schottky diodes have much smaller reverse recovery than silicon Schottky diodes.

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15.15 Review Questions

15.1 List different types of power diodes.

15.2 How does the threshold voltage and saturation current depend on temperature for silicon pn junction diodes?

15.3 What is the typical maximum current density of silicon pn junction diodes and silicon carbide Schottky diodes?

15.4 How can we achieve a high breakdown voltage for pn junction diodes?

15.5 How does the doping concentration affect the breakdown diode voltage?

15.6 Why are the edge terminations used in power diodes?

15.7 What kind of capacitances are present in pn junction diodes?

15.8 List the effects of the reverse recovery on pn junction diodes.

15.9 What is a rectifying and a nonrectifying metal–semiconductor contact?

15.10 List the properties of the Schottky diodes.

15.11 What kind of capacitance is present in Schottky diodes?

15.16 Problems

15.1 A silicon sample is doped with 1.5×10^{16} boron atoms/cm^3. Find the electron and hole concentrations and the semiconductor resistivity and conductivity at $T = 300\,\text{K}$. What is the ratio of the silicon to boron atoms? What is the ratio p/n? What is the ratio of the resistivities of the intrinsic to doped silicon at $T = 300\,\text{K}$?

15.2 A silicon step junction diode has $N_D = 10^{16}\,\text{cm}^{-3}$, $N_A = 10^{18}\,\text{cm}^{-3}$, $T = 300\,\text{K}$, and $V_D = 0$. Find x_p, x_n, W, and x_n/x_p.

15.3 A silicon step junction diode has $N_D = 10^{14}\,\text{cm}^{-3}$, $N_A = 10^{16}\,\text{cm}^{-3}$, $T = 300\,\text{K}$, and $V_D = 0$. Find x_p, x_n, W, and x_n/x_p.

15.4 A silicon step junction diode has $N_D = 10^{14}\,\text{cm}^{-3}$, $N_A = 10^{16}\,\text{cm}^{-3}$, $T = 300\,\text{K}$, and $v_D = -600\,\text{V}$. Find x_p, x_n, W, x_n/x_p, and E_m.

15.5 At time $t = 0$, the current of a p^+n diode is increased from 0 to I_F with the rise time equal to zero. Derive an expression for the charge waveform $Q_p(t)$ and the diode voltage waveform $v_D(t)$. Draw these waveforms using MATLAB. Neglect the junction capacitance.

15.6 At time $t = 0$, the current of a p^+n diode is reduced from I_F to I_R with the fall time equal to zero. Derive an expression for the charge waveform $Q_p(t)$. Draw

it using MATLAB for $I_F = 1\,\text{A}$, $I_R = 5\,\text{A}$, and $\tau_p = 100\,\text{ns}$. Derive expression for the storage time t_s. Calculate t_s in terms of τ_s for: (a) $I_R = -0.1\,I_F$. (b) $I_R = -I_F$. (c) $I_R = -10\,I_F$.

15.7 A dc current source with current I_F supplies a p^+n junction diode in the forward direction for a long time and at $t = 0$ is suddenly removed. Derive an expression for the excess minority hole charge and draw $Q_p(t)/(\tau_p I_F)$ as a function of t/τ_p using MATLAB. Find the time in terms of τ_p at which the initial charge decreases to 10 % of its initial value.

15.8 A silicon carbide pn junction diode has $di_F/dt < 0, f_s = 1\,\text{MHz}$, $V_R = -600\,\text{V}$, $I_R = -5\,\text{A}$, and $t_t = 10\,\text{ns}$. Find the power dissipated during time t_t.

15.9 Design a SiC Schottky diode to meet the following specifications: $V_{BD} = 600\,\text{V}$, $I_{Dmax} = 5\,\text{A}$, $J_{max} = 100\,\text{A/cm}^2$, and $V_{bi} = 10\,\text{V}$. Find A_J, N_D, l_n, C_{J0}, and R_{DR}.

16

Silicon and Silicon Carbide Power MOSFETs

16.1 Introduction

The concept of the MOSFET dates back to the 1930s. The first MOSFET was built in the 1960s. Power MOSFETs were introduced in 1976. MOSFETs have led the revolution in the semiconductor industry. In this chapter, the physical structure and the principle of operation of the enhancement-type power MOSFETs are described, their current–voltage characteristics are derived, and their short-channel effects are explored. The breakdown voltages are studied for silicon and silicon carbide power MOSFETs. Expressions for the on-resistance and capacitances are derived. A SPICE model of the MOSFET is presented. Power MOSFETs have been studied in many publications [1]–[14].

16.2 Physical Structure of Power MOSFETs

The physical structure of the enhancement-type n-channel power MOSFET (NMOS) is shown in Figure 16.1. It is called a vertical double-diffusion (DMOS, DMOSFET, or VDMOSFET) transistor because (1) the drain and source contacts are on the opposite sides of the die, causing vertical current conduction, and (2) two diffusions are used to fabricate p-wells and n^+ sources.

Two diffusions are employed: one to form the p-type body regions and the other to form the n^+-type source regions. This is termed the DMOS process. The MOSFET has four semiconductor layers: $n^+pn^-n^+$. The transistor is fabricated on an n^+ substrate, which is a single-crystal silicon wafer that provides physical support to the device. The thickness of the substrate is usually from 400 to 900 μm. Typically, the substrate is an antimony-doped semiconductor with a thickness of 500 μm, a resistivity of 0.01 Ωcm, and a resistance per unit area of 5×10^{-4} Ω/cm^2. Then an n^- drift region is grown as an epitaxial layer. Epitaxy

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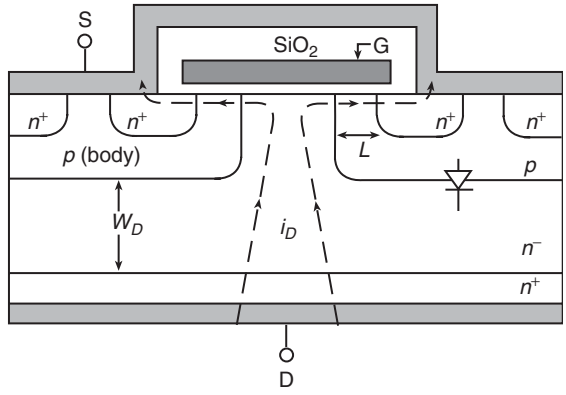


Figure 16.1 Physical structure of n-channel power MOSFET (NMOS).

produces a crystalline layer, which is an extension of the underlying semiconductor lattice. Additional silicon grows following the lattice pattern of the pre-existing crystal. Next, the p-type wells are diffused. The p-type wells are called the *body* regions. Finally, n^+ sources are diffused. The drain current density J reaches 100 A/cm^2. The body is internally shorted to the source by the source metal contact. The arsenic-doped substrate has a resistivity of 0.01 Ωcm. A heavily doped n^+ polycrystalline silicon (called polysilicon) or metal is used as a gate electrode. The typical doping concentration of the polysilicon is $N_D = 10^{20}\,\text{cm}^{-3}$. A thin layer of the gate oxide SiO_2 is grown on the p-wells and the n^- drift region, called the neck region. SiO_2 is a good electrical insulator with resistivity as high as 10^{18} Ωcm, dielectric constant $\epsilon_{r(ox)} = 3.9$, and breakdown voltage $E_{BD(SiO_2)} = 10^7$ V/cm. The thickness t_{ox} of the SiO_2 ranges from 0.01 to 1 μm with a typical value of 0.1 μm. It is in the range of 400 to 1000 atom diameters. The oxide SiO_2 is covered with a metal or a heavily doped n^+ polysilicon, which behaves electrically like a metal electrode. The polysilicon or metal gate, the SiO_2 insulator, and the channel form a capacitor. For $v_{GS} > 0$, a positive charge is accumulated on the gate electrode and a negative charge is formed by the electrons in the induced channel. Therefore, an electric field is created from the positive to negative charges. This field controls the density of electrons and holes in the channel, the channel conductivity, the channel resistance, and the charge movement in the channel, thus controlling the drain current i_D. The region between the p-wells and near the SiO_2 is the *accumulation region*. The n^+ substrate and the n^+ source form nonrectifying ohmic contacts with metal. The substrate is connected to the metal case.

The doping concentration of the drift region N_D is usually 10^{14} to $10^{15}\,\text{cm}^{-3}$. The thickness of the drift region W_D ranges from 10 to 60 μm. The doping of the p-wells is typically $10^{16}\,\text{cm}^{-3}$ and is kept below $5 \times 10^{16}\,\text{cm}^{-3}$. The doping of the n^+ sources is usually $10^{19}\,\text{cm}^{-3}$. There are thousands of parallel cells in the power MOSFET, as depicted in Figure 16.2. The channel length is typically $L = 0.5$ to 2 μm. The channel width W_1 of each cell is from 20 to 100 μm. The channel width of all n cells is $W = nW_1$. The MOSFET aspect ratio is $W/L = nW_1/L$.

There are various patterns of cells: squares on a square grid, squares on a hexagonal grid, squares on an offset square grid, hexagons on a hexagonal grid, hexagons on a square grid, and triangles on a square grid. HEXFET is the trade mark of the International Rectifier MOSFETs, which consist of hexagonal cells. Figure 16.3 shows square cells on a square grid and hexagonal cells on a hexagonal grid. The cells have a square or hexagonal pattern to maximize the channel width W_1 of each cell (equal to the perimeter of the p-well) and

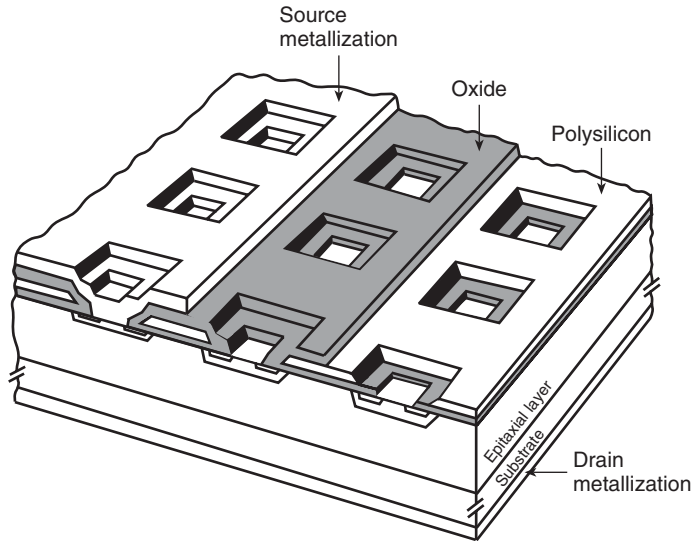


Figure 16.2 Three-dimensional structure of power MOSFETs.

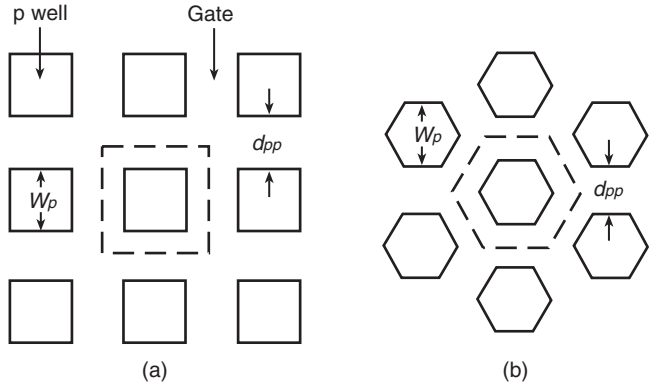


Figure 16.3 Commonly used patterns of power MOSFET cells. (a) Squares on a square grid. (b) Hexagons on a hexagonal grid.

the aspect ratio W/L per unit die area. Figure 16.4 shows a cross-section of the n-channel MOSFET with a square pattern. For square pattern cells, $W_1 = 4W_p$, $W = nW_1 = 4nW_p$, and $W/L = 4nW_p/L$, where W_p is the width of the p-well. The area of a single square cell is $A_1 = (W_p + d_{pp})^2$, where d_{pp} is the distance between the p-wells. The area of all square cells is

$$A_c = nA_1 = n(W_p + d_{pp})^2. \tag{16.1}$$

Hence, the channel width per unit area for square cells is given by

$$D = \frac{W}{A_c} = \frac{4nW_p}{n(W_p + d_{pp})^2} = \frac{4W_p}{(W_p + d_{pp})^2}. \tag{16.2}$$

The channel width per unit area $D = W/A_c$ is 0.07 to 0.17 m/mm^2. The lower value of D corresponds to high-voltage MOSFETs and the higher value of D is achieved for

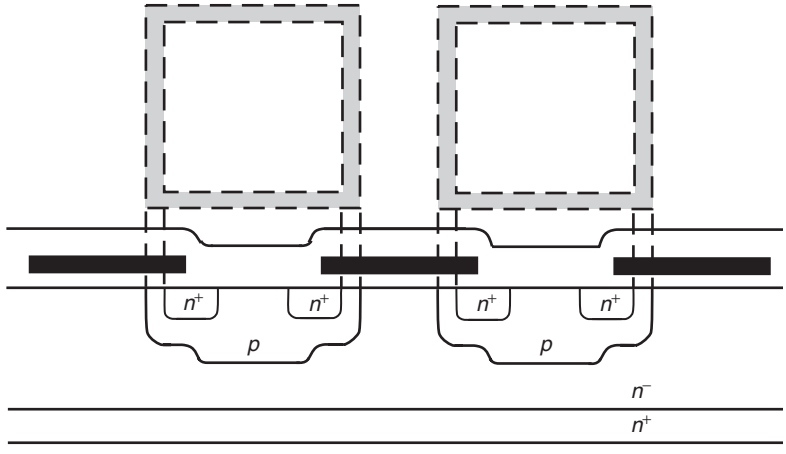


Figure 16.4 Square pattern of n-channel power MOSFET.

low-voltage MOSFETs. The cell density is defined as

$$CD = \frac{n}{A_c}. \tag{16.3}$$

Typically, there are 2500 to 5400 cells/mm^2. The high-current source and the gate bounding pads are not laid over the active semiconductor to increase the reliability. The field guard rings and field plate terminations are used around the corners and edges of the chip to prevent crowding of the electric field and peripheral voltage breakdown. Both the area of the pads A_p and the area of the field guard rings A_r increase the area of the chip by about 25 %. The total chip area is

$$A_{ch} = A_c + A_p + A_r. \tag{16.4}$$

The chip area utilization is

$$U = \frac{W}{A_{ch}} = \frac{W}{A_c + A_p + A_r}. \tag{16.5}$$

In the p-channel enhancement-type MOSFET (PMOS), the dopant types, the voltage polarities, and the drain current direction are reversed, as illustrated in Figure 16.5. This

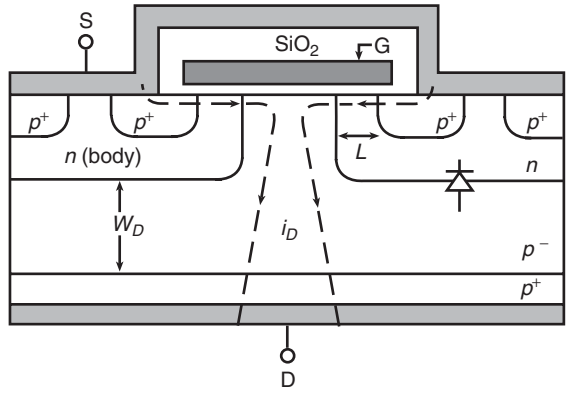


Figure 16.5 Physical structure of p-channel power MOSFET.

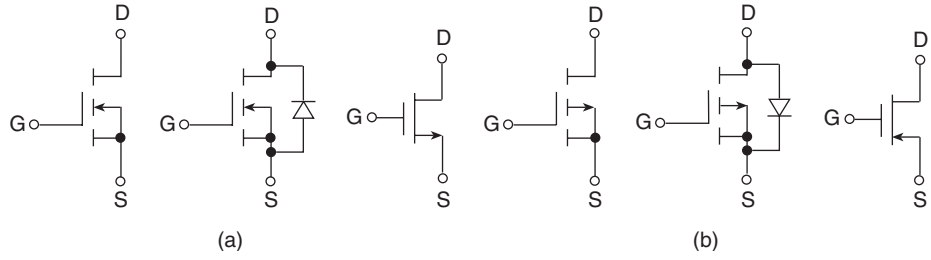


Figure 16.6 Complete and simplified circuit symbols for enhancement power MOSFETs. (a) For n-channel power MOSFET. (b) For p-channel power MOSFET.

transistor has four layers: $p^+np^-p^+$. The current flows from source to drain, and $V_t < 0$, $v_{GS} < 0$, and $v_{DS} < 0$. Applying a negative potential to the gate attracts holes in the n-wells under the gate, and the electrons are repelled away from the oxide-semiconductor interface. An overbalance of holes in the formerly n-type semiconductor causes an inversion. The n-type semiconductor becomes a p-type semiconductor, connecting drain to source. Holes are charge carriers. Figure 16.6 shows circuit symbols for the enhancement-type MOSFETs.

16.3 Principle of Operation of Power MOSFETs

16.3.1 Cutoff Region

For $v_{GS} \leq 0$ (or, to be more exact, for $v_{GS} < V_t$), the drain and source are isolated from each other because the pn junction is reverse biased and there are no charge carriers (electrons) in the p-type material. The drain current i_D is zero. The MOSFET channel is in the off-state. It is very important to have a high-quality, low-leakage-current pn body diode junction to ensure a low off-state leakage current in the MOSFET.

16.3.2 Formation of Channel

For $v_{GS} > 0$, the gate positive potential and the electric field at the $Si-SiO_2$ interface attracts free electrons from the n^+ source and the p-type body and repels free holes into the p-type body. The value of v_{GS} at which the concentration of free electrons is equal to the concentration of holes is termed the *threshold voltage* V_t. When $v_{GS} > V_t$, the concentration of free electrons becomes higher than that of holes, and the area behaves like an n-type semiconductor and is called an *inversion layer*. This is because the p-type semiconductor is 'inverted' into the n-type semiconductor. An n-type channel or conductive path is created, which connects the drain to the source. The lateral n-channel is induced in the p-wells beneath the gate dioxide between the n-type drain and the n^+-type source. The resulting channel is short and its thickness is of the order of 10 nm. The threshold voltage V_t is the minimum gate-to-source voltage required to induce the channel. The phenomenon used to modulate the conductivity of a semiconductor and control the current flow by applying an electric field is called the *field effect*. If the drain-to-source voltage v_{DS} is applied, the drain current i_D flows between drain and source through the induced n-channel, carried

by the mobile free electrons, which are majority carriers. For $v_{GS} > V_t$ and $v_{DS} > 0$, $i_D > 0$. Current is conducted by electrons from the source, moving horizontally through the channel, and then vertically down through the neck, the drift region, and the substrate to the drain. For $v_{GS} > V_t$ and $v_{DS} < 0$, $i_D < 0$. In this case, electrons flow from drain to source.

16.3.3 Linear Region

For $v_{DS} < v_{GS} - V_t$ and $v_{GS} > V_t$, the electron drift current, equal to the drain current i_D, increases *linearly* with the increase in the drain-to-source voltage v_{DS} at a given voltage v_{GS}. As the gate-to-source voltage v_{GS} is increased, more electrons are attracted to the channel, reducing the channel resistivity and the channel resistance r_{DS}. Therefore, the MOSFET looks electrically like the gate-to-source voltage-controlled n-type channel resistor $r_{DS}(v_{GS})$. Other components of the drain-to-source resistance are neglected at this stage of the analysis. This mode of operation is called the *linear region*, *triode region*, or *ohmic region* because $i_D = v_{DS}/r_{DS}$. When the gate-to-source voltage v_{GS} increases, the slope of the nearly the linear $i_D - v_{DS}$ characteristic increases, which means that the channel on-resistance r_{DS} decreases. The voltage-controlled resistor can be called the 'transfer resistor', which led to the name transistor. The drain current flow i_D takes place by the movement of only one type of carriers, which are electrons in n-channel MOSFETs. The electrons are majority charge carriers in NMOS transistors. Therefore, MOSFETs belong to the family of unipolar semiconductor devices. Due to the absence of minority carrier transport, MOSFETs can be switched on and off at high frequencies. The channel resistance is in the range $5\,\text{m}\Omega \leq r_{DS} \leq \infty$. Therefore, MOSFETs are very attractive electronic on–off switches for power electronics applications.

16.3.4 Saturation Region

The gate-to-drain voltage is $v_{GD} = v_{GS} - v_{DS}$. For $v_{DS} < v_{GS} - V_t > 0$ and $v_{GS} > V_t$, $i_D > 0$ and the voltage v_{DS} drops along the channel due to the channel distributed resistance r_{DS}. This voltage increases from 0 at the source end to v_{DS} at the drain end. As the drain current i_D increases, the ohmic voltage drop along the channel also increases. The overall voltage along the channel decreases from $v_{GD} = v_{GS}$ at the source end to $v_{GD} = v_{GS} - v_{DS}$ at the drain end. As a result, the largest channel depth is at the source end and the smallest at the drain end. At $v_{DS(sat)} = v_{GS} - V_t$, that is, at $v_{GD} = V_t = v_{GS} - v_{DS(sat)}$, the channel depth at the drain end is reduced almost to zero, and the channel is said to be *pinched off*. As the drain-to-source voltage v_{DS} increases beyond $v_{DS(sat)}$, the point at which the channel is pinched off moves more and more into the channel, closer to the source end. The electric field E along the channel in the pinch-off region is very high, and the electrons in this part of the channel travel at the saturation drift velocity v_{sat}. Therefore, the drain current does not increase with increasing voltage v_{DS}. When $v_{DS} \geq v_{GS} - V_t$ and $v_{GS} > V_t$, the drain current saturates and remains nearly constant, independent of v_{DS}. The additional drain-to-source voltage $\Delta v_{DS} = v_{DS} - v_{DS(sat)}$ is dropped across the depletion region in the range from the pinch-off point to the drain end. This mode of operation is called the *saturation region* or *pinch-off region*. When v_{GS} increases, i_D also increases. The transistor in the pinch-off region behaves like a voltage-dependent current source.

16.3.5 Antiparallel Diode

For $v_{GS} \leq V_t$, the transistor channel is in the cutoff region. The p-type body well and the lightly doped n^- type *drift region* form a pn junction, which prevents the current flow and supports a high voltage drop. The pn junction is reverse biased, the MOSFET channel disappears, and the MOSFET channel is OFF. The diode is called the *body diode* or *antiparallel body diode*. As the drain-to-source voltage v_{DS} increases, the pn junction depletion region extends into the drift region because the doping of the drift region is much lower than that of the body region. The MOSFET breakdown voltage, denoted by V_{BD} or BV_{DSS}, is determined by the drift region. The junction breakdown voltage V_{BD} increases as the drift region thickness W_D increases and the drift region doping concentration N_D decreases.

If $v_{GS} < V_t$ and $i_D < 0$, the channel is OFF and the body diode conducts the current i_D. If $v_{GS} > V_t$, $v_{DS} < 0$, and the voltage drop across the MOSFET on-resistance r_{DS} is greater than 0.7 V (i.e., $|r_{DS} i_D| > 0.7\,\text{V}$), the body diode is ON, and both the channel and the body diode conduct negative current i_D. At high negative currents, the body diode conducts much more current than the channel. When the transistor is turned off at a large negative current i_D, the body diode suffers from reverse recovery.

16.3.6 Integrated MOSFETs

In integrated small-signal MOSFETs, the source and the drain are on the same side of the chip surface, causing horizontal current conduction. The depletion region of the reverse-biased drain-to-body pn junction diode spreads into the short channel, resulting in a low punch-through breakdown voltage between source and drain. If a MOSFET is designed to withstand high voltages, the channel length L must be increased, which reduces the aspect ratio W/L and the maximum drain current. The breakdown voltage is proportional to the channel length L, whereas the drain current is inversely proportional to the channel length L. The power MOSFET structure allows for a short channel and a high breakdown voltage, resolving the conflict between high current and high voltage in IC MOSFETs.

16.4 Derivation of Power MOSFET Characteristics

16.4.1 Ohmic Region

Consider the situation shown in Figure 16.7(a), where $v_{GS} > V_t$ and $v_{DS} = 0$. In this case, $v_{GD} = v_{GS} - v_{DS} = v_{GS} > V_t$ and therefore a channel is induced. The electron charge stored in the channel is given by

$$Q_n = -C\,\Delta V_{GS} = -C\,(v_{GS} - V_t) = -\frac{C}{WL}\,WL(v_{GS} - V_t) = -C_{ox}\,WL(v_{GS} - V_t), \quad (16.6)$$

where the gate-oxide-channel capacitance is

$$C = \epsilon_{r(ox)}\epsilon_0 \frac{WL}{t_{ox}} = \epsilon_{r(ox)}\epsilon_0 \frac{A_G}{t_{ox}}, \quad (16.7)$$

the gate-oxide-channel capacitance (or oxide capacitance) per unit area is

$$C_{ox} = \frac{C}{WL} = \frac{C}{A_G} = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}, \quad (16.8)$$

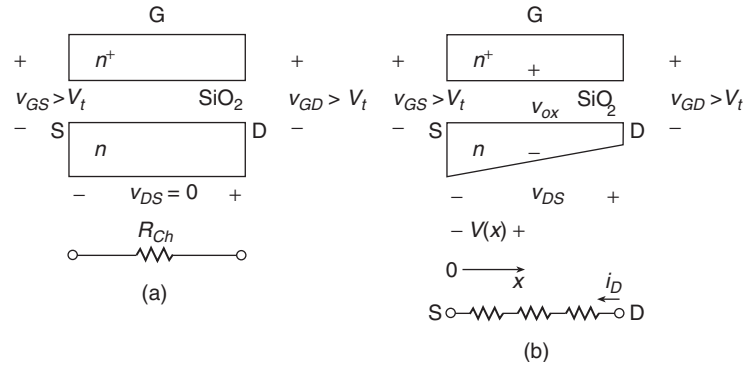


Figure 16.7 Voltages in the MOSFET structure in the linear region. (a) For $v_{DS} = 0$. (b) For $0 < v_{DS} < v_{DS(sat)}$.

L is the channel length, W is the channel width, $A_G = WL$ is the gate area, and t_{ox} is the silicon oxide thickness. As the silicon oxide thickness t_{ox} decreases, C_{ox} increases, and the field effect becomes stronger. If the electrons travel the length of the channel L with average electron drift velocity v, the time it takes to travel that distance is given by

$$T = \frac{L}{v}. \tag{16.9}$$

Hence, the drain current (i.e., the movement of charge) is

$$i_D = \frac{Q_n}{T} = \frac{Q_n}{L/v} = \frac{Q_n v}{L} = Q_L v, \tag{16.10}$$

where the electron charge per unit length is uniform along the channel and is expressed by

$$Q_L = \frac{Q_n}{L} = -C_{ox} W (v_{GS} - V_t). \tag{16.11}$$

The electron charge per unit length Q_L is directly proportional to $v_{GS} - V_t$. Assuming that the space-charge density in the channel is uniform, we have

$$\rho_v = nq = \frac{-Q_n}{Vol} = \frac{-Q_n}{WLH} = \frac{-Q_L}{A} = \frac{C_{ox} W}{A}(v_{GS} - V_t), \tag{16.12}$$

where $A = WH$ is the inverted-channel cross-sectional area perpendicular to the direction of the drain current flow, $Vol = LWH = AH$ is the channel volume, and H is the channel height. As $v_{GS} - V_t$ increases, the channel conductivity σ also linearly increases. The electron density in the channel is

$$n = \frac{\rho_v}{q} = \frac{C_{ox} W}{qA}(v_{GS} - V_t). \tag{16.13}$$

Hence, the channel conductivity is

$$\sigma = nq\mu_n = \rho_v \mu_n = \frac{\mu_n C_{ox} W}{A}(v_{GS} - V_t). \tag{16.14}$$

This equation describes the channel conductivity modulation by the gate-to-source voltage v_{GS}. The space-charge density ρ_v, the electron density n in the channel, and the channel conductivity σ are directly proportional to the voltage $v_{GS} - V_t$ that induces the channel. They are also directly proportional to the electron mobility μ_n in the channel and the channel width W, and inversely proportional to the channel cross-sectional area A.

If the drain-to-source voltage $v_{DS} > 0$ and is very low, (e.g., 0.1 V), $v_{GD} > V_t$, the voltage drop along the channel will be very low and its effect on the channel height along the channel can be neglected. The channel conductivity σ remains approximately uniform. The electric field intensity along the channel from drain to source is

$$E = -\frac{v_{DS}}{L}. \tag{16.15}$$

The drain current density J is equal to the drift current density caused by the movement of charge carriers forced by the electric field E,

$$J = -\sigma E. \tag{16.16}$$

Hence, the drain current is given by

$$i_D = JA = -\sigma EA = -\sigma EHW = \sigma HW\frac{v_{DS}}{L} = \mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)v_{DS}. \tag{16.17}$$

The large-signal channel resistance at a very low drain voltage is

$$R_{Ch} = \frac{v_{DS}}{i_D} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)}. \tag{16.18}$$

Now, consider the situation depicted in Figure 16.7(b), where $v_{GS} > V_t$, $0 < v_{DS} < v_{DS(sat)}$, and $i_D > 0$. The channel is induced, but it is not pinched off. There is a lateral voltage drop along the channel due to the voltage v_{DS}, which changes from point to point. Let us denote the voltage drop along the channel from the source end to a point x by $V(x)$. By Kirchhoff's voltage law, the voltage between the gate electrode and any local point x in the channel is

$$v_{ox}(x) = v_{GS} - V(x) > V_t. \tag{16.19}$$

At the source end, $V(0) = 0$, resulting in

$$v_{ox}(0) = v_{GS}. \tag{16.20}$$

At the drain end, $V(L) = v_{DS}$, leading to

$$v_{ox}(L) = v_{GD} = v_{GS} - v_{DS}. \tag{16.21}$$

As v_{DS} increases at a fixed voltage v_{GS}, the voltage v_{GD} decreases. The charge stored in the channel is

$$Q_n(x) = -C[v_{GS} - V_t - V(x)] = -\frac{CWL}{WL}[v_{ox}(x) - V_t] = -C_{ox}WL[v_{GS} - V_t - V(x)]. \tag{16.22}$$

The electron charge per unit length at point x is

$$Q_L(x) = \frac{Q_n(x)}{L} = -C_{ox}W[v_{GS} - V_t - V(x)]. \tag{16.23}$$

The electron density in the channel is

$$n(x) = \frac{\rho_v(x)}{q} = \frac{C_{ox}}{qA(x)}[v_{GS} - V_t - V(x)]. \tag{16.24}$$

The conductivity of the channel depends on x and is given by

$$\sigma(x) = n(x)q\mu_n = \rho_v(x)\mu_n = \frac{\mu_n C_{ox}W}{A(x)}[v_{GS} - V_t - V(x)]. \tag{16.25}$$

The channel conductivity $\sigma(x)$ decreases as x increases from the source to the drain. The electric field along the channel is given by

$$E(x) = -\frac{dV(x)}{dx}. \tag{16.26}$$

The average drift electron velocity caused by the electric field E is

$$v(x) = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx}. \tag{16.27}$$

The drain current is

$$i_D = \frac{Q_n(x)}{t} = \frac{Q_n(x)}{L}\frac{L}{t} = Q_L(x)v, \tag{16.28}$$

where $v = L/t$ is the average drift electron velocity. Hence,

$$i_D = -C_{ox}W[v_{GS} - V_t - V(x)](-\mu_n E) = \mu_n C_{ox}W[v_{GS} - V_t - V(x)]\left[\frac{dV(x)}{dx}\right]. \tag{16.29}$$

Since the drain current i_D along the channel remains constant, $V(x)$ and $dV(x)/dx$ vary in such a way that the product of $v_{GS} - V_t - V(x)$ and $dV(x)/dx$ is independent of x. Regrouping (16.29), we get

$$i_D dx = \mu_n C_{ox}W[v_{GS} - V_t - V(x)]\,dV(x). \tag{16.30}$$

Integrating both sides of (16.30),

$$i_D \int_0^L dx = \mu_n C_{ox}W \int_0^{v_{DS}} [v_{GS} - V_t - V(x)]\,dV(x), \tag{16.31}$$

one obtains the drain current for the linear region

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{v_{DS}^2}{2}\right] = \left[\frac{C_{ox}WL}{L}\left(v_{GS} - V_t - \frac{v_{DS}}{2}\right)\right]\left(\frac{\mu_n v_{DS}}{L}\right)$$

$$= \frac{Q_{AV}}{L}|v_{AV}|. \tag{16.32}$$

The first term represents the magnitude of the average charge per unit length in the channel $|Q_n|/L$ because the average voltage along the channel is $V_{AV} = v_{DS}/2$. The second term represents the magnitude of the average electron drift velocity in the channel $|v_{AV}| = \mu_n E_{AV}$, where the average electric field along the channel is $E_{AV} = v_{DS}/L$.

In summary, a larger C_{ox} and a higher voltage v_{GS} result in a larger electron density n in the channel. A higher gate-to-source voltage v_{GS} yields a higher channel conductivity σ and a lower channel resistance. The voltage drop along the channel inversion layer v_{Ch} becomes low for high values of v_{GS}. A higher drain-to-source voltage v_{DS} forces a larger drain current i_D. The drain current i_D increases quadratically with increasing v_{DS} for a given v_{GS} and reaches the saturation level $i_{D(sat)}$ at $v_{DS(sat)} = v_{GS} - V_t$.

The large-signal channel resistance is

$$R_{Ch} = \frac{v_{DS}}{i_D} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(v_{GS} - V_t - \frac{v_{DS}}{2}\right)}, \quad \text{for } v_{DS} < v_{GS} - V_t. \tag{16.33}$$

This equation simplifies to

$$R_{Ch} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)}, \quad \text{for } v_{DS} \ll 2(v_{GS} - V_t). \tag{16.34}$$

16.4.2 Pinch-off Region

At the boundary between the linear region and the saturation region, $v_{GS} > V_t$, $v_{DS} = v_{DS(sat)} = v_{GS} - V_t$, $v_{GD} = V_t$, and the channel is pinched off just at the drain, as shown in Figure 16.8(a). Substituting this condition into (16.32), we obtain the drain current in the saturation region

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 = \left(\frac{C_{ox}WL}{L}\frac{v_{GS} - V_t}{2}\right)\left(\mu_n \frac{v_{GS} - V_t}{L}\right)$$
$$= \frac{Q_{AV}}{L}|v_{AV}|. \tag{16.35}$$

The first term represents the magnitude of the average electron charge in the inversion layer, where the average voltage along the inverted channel region is $(v_{GS} - V_t)/2$, which is independent of v_{DS}. The second term represents the magnitude of the average drift electron velocity in the channel $|v_{AV}| = \mu_n E_{AV} = \mu_n(v_{GS} - V_t)/L$.

At $v_{GS} > V_t$ and $v_{DS} > v_{GS} - V_t$, the channel is pinched off between the drain and the source at a point x_{po}, where $V(x_{po}) = v_{GS} - V_t$, that is, at $v_{ox} = v_{GS} - V(x_{po}) = V_t$. Figure 16.8(b) shows this situation. The voltage drop across the inverted channel between the source and the end of the channel x_{po} is $v_{ch} = v_{GS} - V_t$. The voltage across the pinched-off region located between the point x_{po} and the drain is $v_{pinch} = v_{DS} - v_{DSsat}$. The electrons flow from the source to the pinched-off point x_{po} through the inverted channel, and then are injected into the depletion region between the pinched-off point x_{po} and the drain. A high electric field in the depletion region sweeps the electrons into the drain. The voltage across the channel is constant equal to $v(x_{po}) = v_{GS} - V_t$. Therefore, the drain current i_D is approximately constant and nearly independent of the voltage v_{DS}.

16.4.3 Channel-length Modulation

As the drain-to-source voltage v_{DS} increases at fixed voltage v_{GS} in the saturation region, the pinched-off point x_{po} moves from the drain towards the source and the length of the

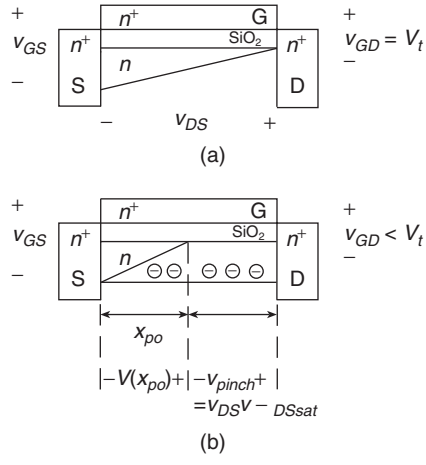


Figure 16.8 Voltages in the MOSFET structure in the saturation region. (a) The channel is pinched off at the drain. (b) The channel is pinched off between the drain and the source.

inverted channel is reduced, resulting in increased drain current. The effective channel length is

$$L_e = L - \Delta L = L\left(1 - \frac{\Delta L}{L}\right). \tag{16.36}$$

The phenomenon of channel length variation with voltage v_{DS} is called *channel-length modulation*. The drain current in the saturation region is given by

$$\begin{aligned} i_D &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_e}\right)(v_{GS} - V_t)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L - \Delta L}\right)(v_{GS} - V_t)^2 \\ &= \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L(1 - \frac{\Delta L}{L})}\right](v_{GS} - V_t)^2 \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2\left(1 + \frac{\Delta L}{L}\right) \\ &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2(1 + \lambda v_{DS}) = I_{Dsat}(1 + \lambda v_{DS}), \end{aligned} \tag{16.37}$$

where

$$\frac{\Delta L}{L} = \lambda v_{DS} = \frac{v_{DS}}{V_A}. \tag{16.38}$$

As the channel length L decreases, the ratio $\Delta L/L$ increases. Therefore, the slope of the $i_D - v_{DS}$ characteristic increases more in short-channel MOSFETs.

16.5 Power MOSFET Characteristics

The MOSFET characteristics for the cutoff (or voltage blocking), linear (ohmic or triode), and saturation (or pinch-off) regions are given by

$$i_D = \begin{cases} 0, & \text{for } v_{GS} \le V_t, \\ K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2], & \text{for } v_{GS} \ge V_t \text{ and } v_{DS} \le v_{GS} - V_t, \\ K(v_{GS} - V_t)^2(1 + \lambda v_{DS}), & \text{for } v_{GS} \ge V_t \text{ and } v_{DS} > v_{GS} - V_t. \end{cases} \tag{16.39}$$

The device parameter K is given by

$$K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) = \frac{1}{2}k_p\left(\frac{W}{L}\right), \tag{16.40}$$

where W/L is the aspect ratio, and μ_n is the electron mobility in the channel, also called the surface mobility or the effective mobility (typically, $\mu_n = 600\,\text{cm}^2/\text{Vs}$ for Si). C_{ox} is the oxide capacitance C per unit area of the gate-oxide-channel capacitor with the oxide SiO_2 acting as a dielectric; it is given by

$$C_{ox} = \frac{C}{A_{ox}} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}, \tag{16.41}$$

where $\epsilon_{ox} = \epsilon_r\epsilon_0$ is the oxide permittivity, $\epsilon_{r(SiO_2)} = 3.9$, $\epsilon_0 = 8.8542 \times 10^{-14}\,\text{F/cm} = 8.8542 \times 10^{-12}\,\text{F/cm}$, A_{ox} is the silicon dioxide area, and t_{ox} is the silicon dioxide thickness. The process constant k_p, also called the transconductance parameter, in (16.40) is given by

$$k_p = \mu_n C_{ox} = \mu_n\frac{\epsilon_{ox}}{t_{ox}} = \mu_n\frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}. \tag{16.42}$$

The term λ which appears in (16.39) is the channel-length modulation coefficient, $\lambda = 1/V_A$, where V_A is the Early voltage; λ lies in the range $0.001\,\text{V}^1 \le \lambda \le 0.1\,\text{V}^{-1}$.

V_t in (16.39) is the threshold voltage, defined as the gate-to-sure voltage at which the MOSFET begins to conduct,

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}], \tag{16.43}$$

and it is increased by the *body effect* when $V_{SB} > 0$. ϕ_F is the surface potential, with $2\phi_F$ in the range $0.3\,\text{V} \le 2\phi_F \le 1\,\text{V}$, and γ is the body-effect parameter, with $0 \le \gamma \le 3\,\text{V}^{1/2}$. Typically, $\gamma = 0.5\,\text{V}^{1/2}$ and $2\phi_F = 0.6\,\text{V}$. The body-effect parameter is given by

$$\gamma = \frac{\sqrt{2q\epsilon_{r(Si)}\epsilon_0 N_A}}{C_{ox}} = \frac{t_{ox}\sqrt{2q\epsilon_{r(Si)}\epsilon_0 N_A}}{\epsilon_{r(ox)}\epsilon_0}. \tag{16.44}$$

V_{t0} in (16.43) is the threshold voltage at the source-to-body voltage $V_{SB} = 0$, and is given by

$$V_{t0} = \frac{2\sqrt{\epsilon_{r(Si)}\epsilon_0 q N_A \phi_F}}{C_{ox}} + 2\phi_F = \frac{2t_{ox}\sqrt{\epsilon_r(Si)\epsilon_0 q N_A}}{\epsilon_r(ox)\epsilon_0} + 2\phi_F. \tag{16.45}$$

Typical values of V_{t0} are from 1 to 4 V for power MOSFETs. It can be decreased by deliberately decreasing the p-well body concentration and by decreasing t_{ox}. However, the body doping concentration N_A is constrained by the need to avoid or reduce the channel-modulation effect caused by v_{DS}. Reducing t_{ox} makes the MOSFET more vulnerable to gate-oxide voltage breakdown. The MOSFET threshold voltage V_{t0} is measured at $V_{GD} = 0$ and $I_D = 0.25\,\text{mA}$.

The electron mobility μ_n in the channel is less than that in the bulk of silicon. In addition to lattice and ionized impurity scattering, the mobility in the channel is limited by the surface collisions. The majority carriers in the MOSFET move in the surface inversion layer, where the gate-induced electric field E accelerates the carriers towards the surface, causing the collisions with the semiconductor surface. In this layer, the charge carrier collisions with the oxide–semiconductor interface defects reduce the mobility. The effect of charge trapping at the interface is one reason for mobility reduction.

The output MOSFET characteristics get steeper as the drain current increases with increasing gate-to-source voltage v_{GS}. If the $i_D - v_{DS}$ characteristics are extended to the left, they meet and intersect the v_{DS}-axis at voltage $-V_A = -1/\lambda$. As t_{ox} decreases, C_{ox} and k_p increase.

The drain-to-source voltage at the boundary between the linear and saturation regions is

$$v_{DS(sat)} = v_{GS} - V_t. \tag{16.46}$$

The drain saturation current is

$$i_{Dsat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) v_{DS(sat)}^2. \tag{16.47}$$

In discrete power MOSFETs, the body is internally connected to the source to keep the body diode reverse biased for most modes of operation. To increase the current capability of the power MOSFET, its width W should be made very large and the length should be made as small as possible. Figure 16.9 shows the n-channel MOSFET $v_{GS} - i_D$ and $v_{DS} - i_D$ characteristics.

The maximum rms drain current is limited by the MOSFET power loss. Assuming that the conduction loss P_{rDS} in the MOSFET on-resistance r_{DS} is dominant, the maximum rms value of the drain current is

$$I_{Drms(max)} = \sqrt{\frac{P_{rDS}}{r_{DS}}} \;\alpha\; \sqrt{\frac{P_{rDS}}{V_{DSS}^{2.4}}}. \tag{16.48}$$

Since the MOSFET on-resistance r_{DS} increases with increasing breakdown voltage V_{DSS}, the maximum rms drain current $I_{Drms(max)}$ decreases with increasing breakdown voltage V_{DSS}.

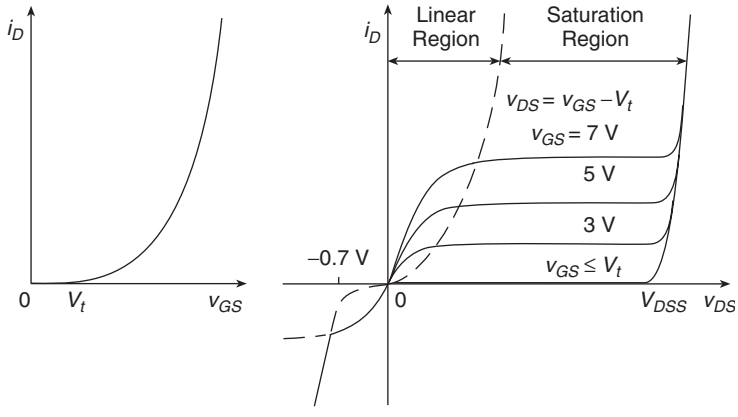


Figure 16.9 Input and output characteristics of n-channel MOSFET.

The maximum gate-to-source voltage is $\pm V_{GS(max)} = \pm 20\,\text{V}$. The threshold voltage V_t is in the range of 2 to 4 V. A typical maximum operating junction temperature $T_{J(max)}$ for silicon power MOSFETs is 150°C. The maximum case temperature $T_{C(max)}$ is typically 100°C. For silicon carbide power MOSFETs, the maximum operating junction temperature is much higher, usually about 300°C. The junction-to-case thermal resistance θ_{JC} is typically 1°C/W for silicon devices and 0.3°C/W for silicon carbide devices. The threshold voltage V_{t0} exhibits a negative thermal coefficient

$$\delta_{Vt0} = \frac{\Delta V_{t0}}{\Delta T} = -6\,\text{mV/°C}. \tag{16.49}$$

However, k_p decreases with increasing temperature T. The slope of the $v_{GS}-i_D$ characteristic decreases when the temperature increases. The drain current i_D exhibits a negative thermal coefficient for its higher values. Therefore, MOSFETs do not suffer from thermal runaway at high currents.

The parameters of the IRF540 power MOSFET are: $V_{DSS} = 100\,\text{V}$, $I_{Dmax} = 28\,\text{A}$, $r_{DS(ON)} = 0.077\,\Omega$, $W/L = 1.4 \times 10^6$, $V_t = 3.5\,\text{V}$, $W = 1\,\text{m}$, $\mu_n = 0.06\,\text{m}^2/\text{Vs} = 600\,\text{cm}^2/\text{Vs}$, $C_{ox} = 3.45 \times 10^{-4}\,\text{F/m}^2 = 3.45 \times 10^{-8}\,\text{F/cm}^2 = 34.5\,\text{nF/cm}^2$, and $\theta = 0.02\,\text{V}^{-1}$. Hence, $k_p = \mu_n C_{ox} = 0.06 \times 3.45 \times 10^{-4} = 20.7\,\mu\text{A/V}^2$, $K = \frac{1}{2}k_p(W/L) = \frac{1}{2} \times 20.7 \times 10^{-6} \times 1.4 \times 10^6 = 14.49\,\text{A/V}^2$, $L = 10^6/(1.4 \times 10^6) = 0.7\,\mu\text{m}$, and $t_{ox} = \epsilon_{r(SiO_2)}\epsilon_0/C_{ox} = 3.9 \times 8.8542 \times 10^{-14}/(34.5 \times 10^{-9}) = 0.1\,\mu\text{m}$.

16.6 Mobility of Charge Carriers

The charge carriers in a solid are in constant motion at $T > 0\,\text{K}$. Holes and free electrons move through a crystal structure in a random manner at high speed (of the order of 10^7 cm/s), undergoing frequent collisions with the vibrating atoms, other electrons, and defects. An applied electric field E exerts forces on the charge carriers, causing them to acquire small average drift velocity. Holes move in the direction of the applied field and electrons move in the opposite direction to the electric field. This results in electron and hole drift currents. The freedom (or ease) of movement of carriers in a crystal in referred to as mobility. It has significant influence on the electron and hole transport and the drift region resistance. The mobility of electrons μ_n is greater than the mobility of holes μ_p. The bulk carrier mobility

is inversely proportional to the amount of scattering within the semiconductor. There are two major scattering mechanisms: (1) lattice scattering, involving collisions with vibrating lattice atoms; and (2) ionized acceptors and donors scattering. The thermal vibrations cause the displacement of lattice atoms; from their lattice positions.

The velocity of a carrier increases linearly with time between collisions. The velocity just before the collision at time t_c is

$$v_f = at_c = \frac{qE}{m_e}t_c = \frac{qt_c}{m_e}E = \mu E, \tag{16.50}$$

where $a = qE/m_e$ is the acceleration and m_e is the electron effective mass. The average drift velocity is $v_c = v_f/2$. Thus, the mobility is given by

$$\mu = \frac{qt_c}{2m_e}, \tag{16.51}$$

where t_c is the mean free time interval between the collisions, called the relaxation time. As the number of collisions increases, the mean free time t_c decreases, reducing the mobility μ. The mobilities are functions of doping N_D or N_A, temperature T, and electric field intensity E, that is, $\mu_n = f(N, T, E)$ and $\mu_p = f(N, T, E)$.

16.6.1 Effect of Doping Concentration on Mobility

At low doping concentration N_D or N_A, the mobilities are almost independent of the doping concentrations because the ionized impurity scattering is much lower than the lattice scattering and can be neglected. For silicon, the critical concentration $N_c = 10^{15}\,\text{cm}^{-3}$. At high doping concentrations, the mobilities μ_n and μ_p monotonically decrease with increasing doping concentration N_D or N_A, respectively. This is because the ionized impurity scattering is no longer negligible. The carrier mobility in terms of total doping concentration $N = N_A + N_D$ at room temperature is given by the Caughey–Thomas equation [10]

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\dfrac{N}{N_c}\right)^{\alpha}} = \mu_{min} + \frac{\mu_0}{1 + \left(\dfrac{N}{N_c}\right)^{\alpha}}, \tag{16.52}$$

where $\mu_0 = \mu_{max} - \mu_{min}$.

For silicon, the low-field doping-dependent bulk mobilities of electrons and holes at room temperature $T = 300\,\text{K}$ are given by [7]

$$\mu_{n(300)} = 92 + \frac{1268}{1 + \left(\dfrac{N_D + N_A}{1.3 \times 10^{17}}\right)^{0.91}} \approx 92 + \frac{1268}{1 + \left(\dfrac{N_D}{1.3 \times 10^{17}}\right)^{0.91}} \tag{16.53}$$

and

$$\mu_{p(300)} = 54.3 + \frac{406.9}{1 + \left(\dfrac{N_A + N_D}{6.3 \times 10^{16}}\right)^{0.88}} \approx 54.3 + \frac{406.9}{1 + \left(\dfrac{N_A}{6.3 \times 10^{16}}\right)^{0.88}}. \tag{16.54}$$

Figure 16.10 shows the mobilities μ_n and μ_p as functions of doping concentration $N = N_D$ or N_A at $T = 300\,\text{K}$ for silicon.

The resistivities of the n- and p-type semiconductors are

$$\rho_n = \frac{1}{\sigma_n} = \frac{1}{qN_D\mu_n} \tag{16.55}$$

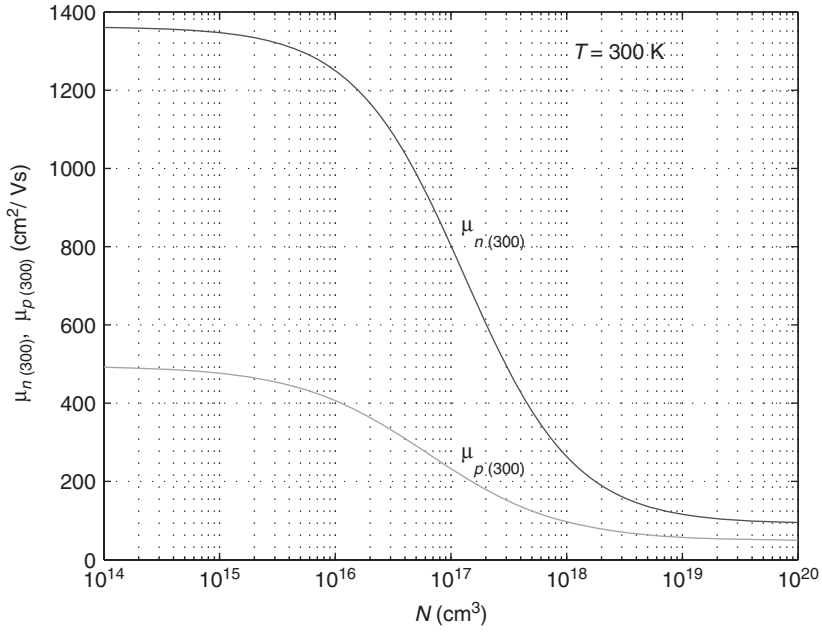


Figure 16.10 Low-field electron mobility μ_n and hole mobility μ_p as functions of doping concentration N at $T = 300\,\text{K}$ for silicon.

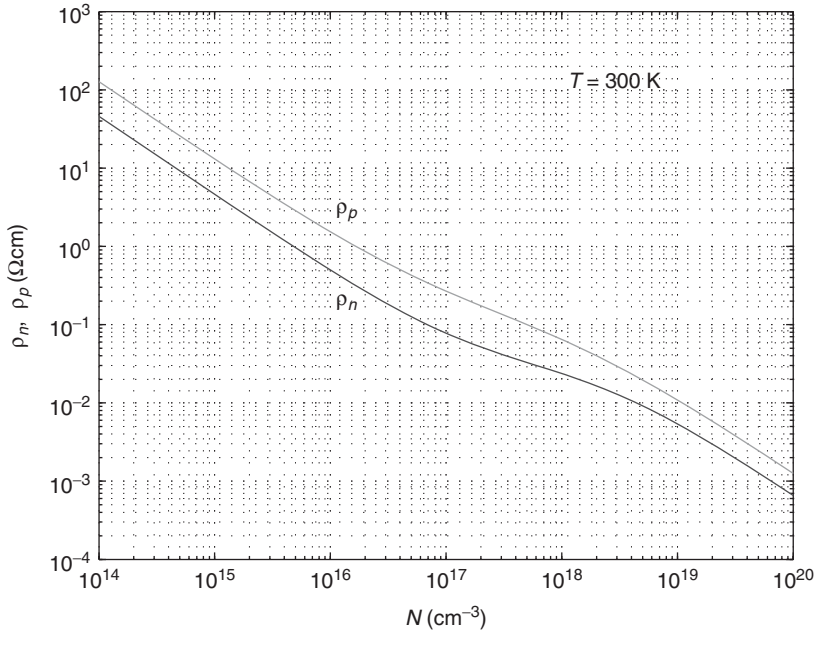


Figure 16.11 Low-field resistivities ρ_n and ρ_p as functions of doping concentration N at $T = 300\,\text{K}$ for silicon.

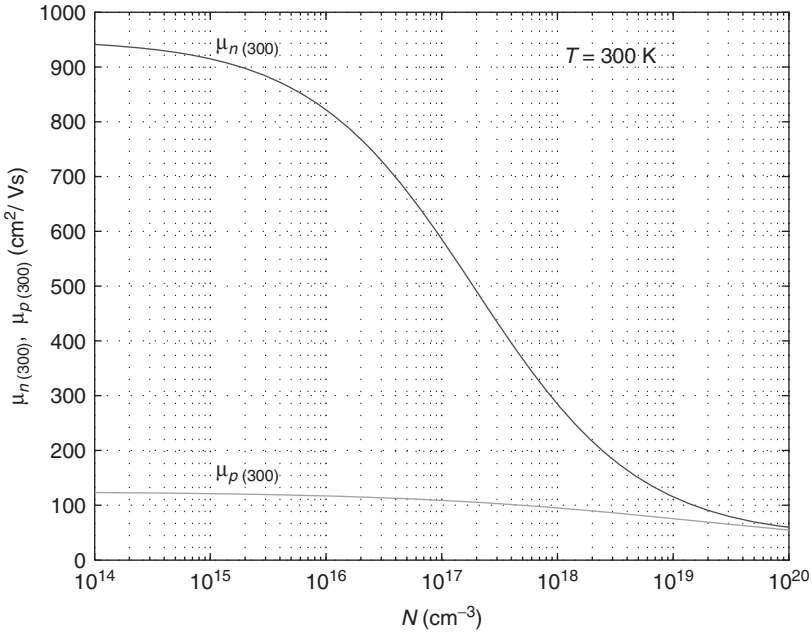


Figure 16.12 Low-field electron mobility μ_n and hole mobility μ_p as functions of doping concentration N at $T = 300\,\text{K}$ for silicon carbide.

and

$$\rho_p = \frac{1}{\sigma_p} = \frac{1}{qN_A\mu_p}. \tag{16.56}$$

Figure 16.11 shows the resistivities ρ_n and ρ_p as functions of doping concentration at $T = 300\,\text{K}$ computed from (16.53)–(16.56) for silicon.

For silicon carbide, the low-field mobilities of electrons and holes at $T = 300\,\text{K}$ are given by

$$\mu_{n(300)} = 40 + \frac{947}{1 + \left(\frac{N_D + N_A}{1.94\times 10^{17}}\right)^{0.61}} \approx 40 + \frac{947}{1 + \left(\frac{N_D}{1.94\times 10^{17}}\right)^{0.61}} \tag{16.57}$$

and

$$\mu_{p(300)} = 15.9 + \frac{124}{1 + \left(\frac{N_A + N_D}{1.76 \times 10^{19}}\right)^{0.34}} \approx 15.9 + \frac{124}{1 + \left(\frac{N_A}{1.76 \times 10^{19}}\right)^{0.34}}. \tag{16.58}$$

Figures 16.12 and 16.13 show the mobilities μ_n and μ_p and resistivities ρ_n and ρ_p as functions of doping concentration N at $T = 300\,\text{K}$ for silicon carbide.

16.6.2 Effect of Temperature on Mobility

The atoms in a crystal vibrate due to their thermal energies. When the temperature of a crystal is increased, the amplitude of the atom vibrations also increases. This results in

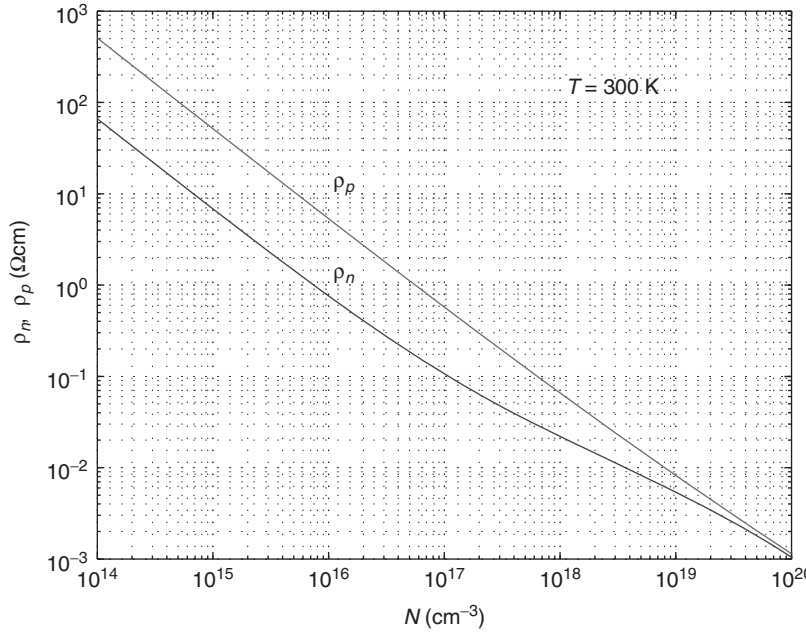


Figure 16.13 Low-field resistivities ρ_n and ρ_p as functions of doping concentration N at $T = 300\,\text{K}$ for silicon carbide.

more frequent collisions between the charge carriers and the atoms, reducing the mobility. The general dependence of the mobility on temperature is

$$\mu = \mu_{(300)} \left(\frac{300}{T} \right)^{\eta}. \tag{16.59}$$

For silicon and silicon carbide, the low-field electron and hole mobilities decrease with increasing temperature T and are given by

$$\mu_{n0} = \mu_{n(300)} \left(\frac{300}{T} \right)^{2.4} \tag{16.60}$$

and

$$\mu_{p0} = \mu_{p(300)} \left(\frac{300}{T} \right)^{2.2}. \tag{16.61}$$

For silicon, the low-field mobilities are $\mu_{n0} = 639\,\text{cm}^2/\text{Vs}$ and $\mu_{p0} = 230\,\text{cm}^2/\text{Vs}$ at $T = 150^\circ\text{C}$. Figures 16.14 and 16.15 show plots of the low-field electron mobility μ_{n0} and hole mobility μ_{p0} as functions of temperature T for silicon.

The resistivities of n- and p-type semiconductors as functions of temperature T are given by

$$\rho_n = \frac{1}{qN_D\mu_n} = \frac{1}{qN_D\mu_{n(300)}} \left(\frac{T}{300} \right)^{2.4} \tag{16.62}$$

and

$$\rho_p = \frac{1}{qN_A\mu_p} = \frac{1}{qN_A\mu_{p(300)}} \left(\frac{T}{300} \right)^{2.2}. \tag{16.63}$$

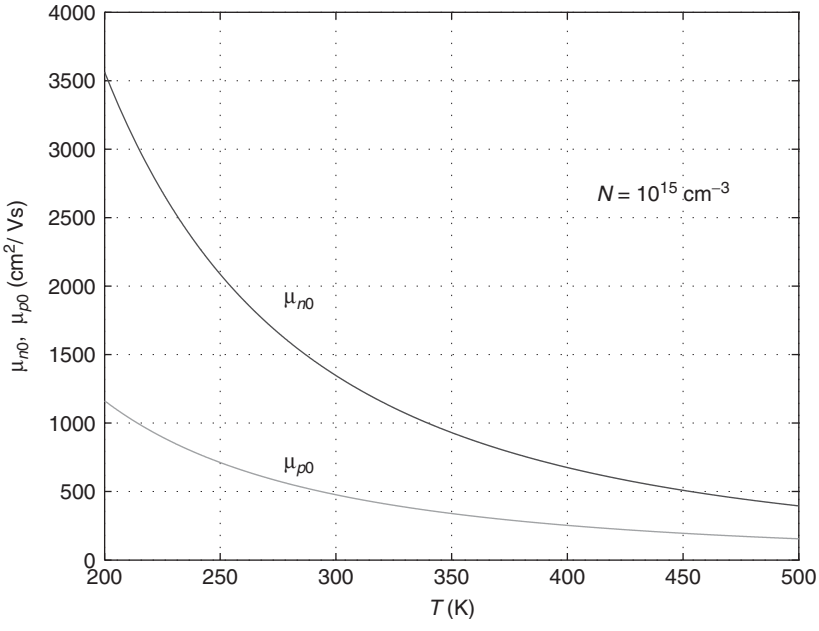


Figure 16.14 Low-field electron mobility μ_{n0} and hole mobility μ_{p0} as functions of temperature T at constant doping concentration $N = 10^{15}\,\text{cm}^{-3}$ for silicon.

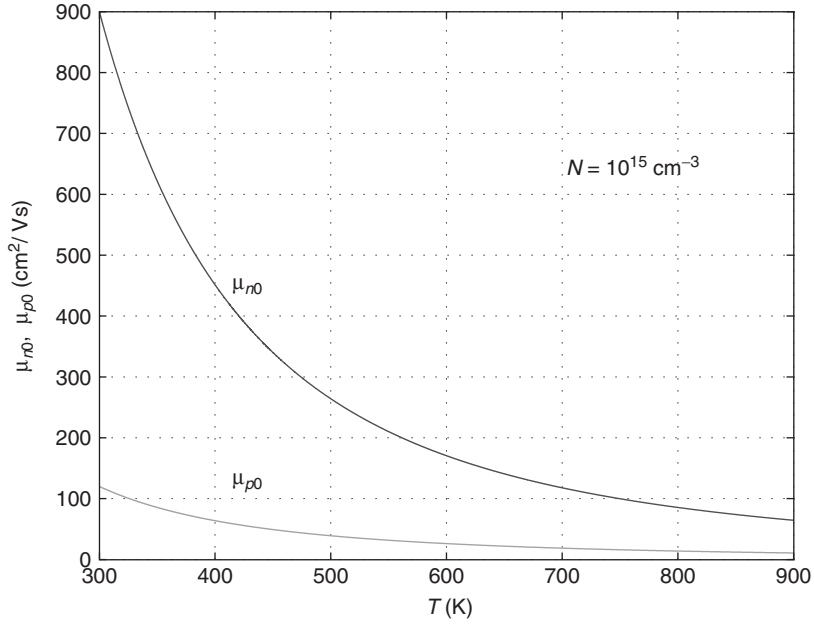


Figure 16.15 Low-field electron mobility μ_{n0} and hole mobility μ_{p0} as functions of temperature T at constant doping concentration $N = 10^{15}\,\text{cm}^{-3}$ for silicon carbide.

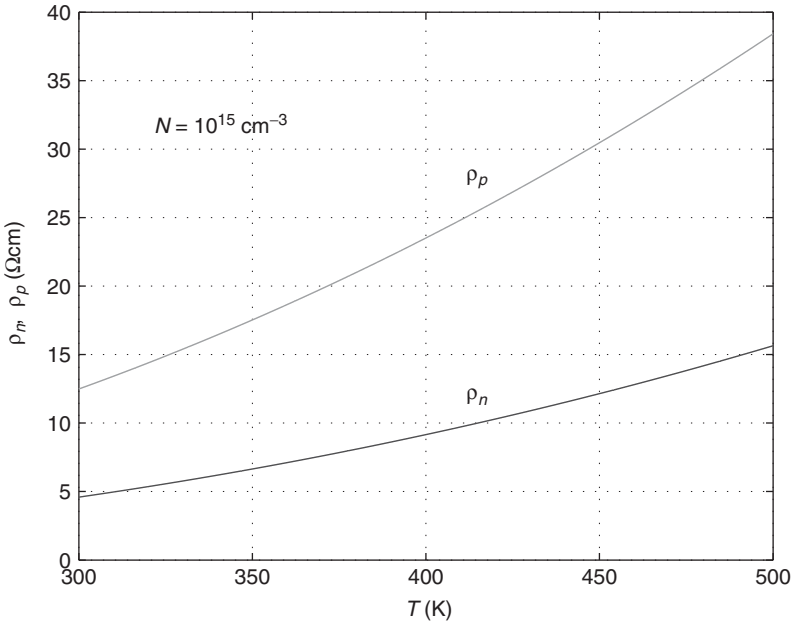


Figure 16.16 Resistivities ρ_n and ρ_p as functions of temperature T at constant doping concentration $N = 10^{15}\,\text{cm}^{-3}$ for silicon.

Figure 16.16 shows plots of resistivities ρ_n and ρ_p as functions of temperature T at $N = 10^{15}\,\text{cm}^3$ for silicon.

16.6.3 Effect of Electric Field on Mobility

If an electric field E is applied to a semiconductor, the holes move as a group in the direction of the electric field intensity E and the electrons move as a group in the opposite direction. In steady state, the carriers gain a net drift velocity from the electric field intensity E. In general, the group average electron drift velocity is given by

$$v = \mu_n E. \tag{16.64}$$

The mobility $\mu = v/E$ is the average drift speed of electrons or holes (as a group) v, when the applied electric field intensity E is 1 V/m. The average drift electron velocity in terms of the electric field intensity E is given by

$$v = \frac{\mu_{n0} E}{1 + \dfrac{\mu_{n0} E}{v_{sat}}}, \tag{16.65}$$

resulting in the electron mobility

$$\mu_n = \frac{v}{E} = \frac{\mu_{n0}}{1 + \dfrac{\mu_{n0} E}{v_{sat}}}. \tag{16.66}$$

Figures 16.17 and 16.18 show the average electron drift velocity v and the electron mobility μ_n as functions of electric field intensity E for silicon at $\mu_{n0} = 1360\,\text{cm}^2/\text{Vs}$ and $v_{sat} = 8 \times 10^6\,\text{cm/s}$. At low values of the electric field intensity E, the average carrier velocity v

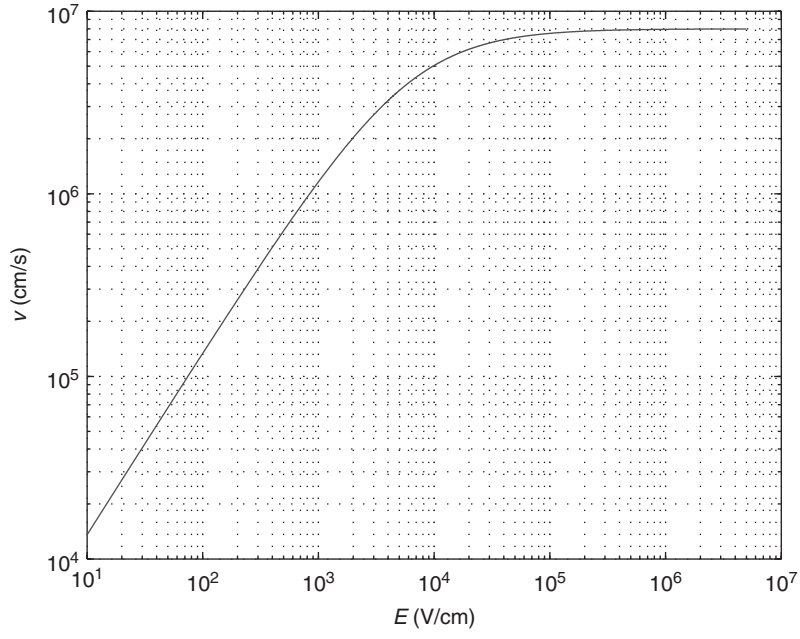


Figure 16.17 Average electron drift velocity v as a function of electric field E for $\mu_n = 1360\,\text{cm}^2/\text{Vs}$, $v_{sat} = 8 \times 10^6\,\text{cm/Vs}$, and $T = 300\,\text{K}$ for silicon.

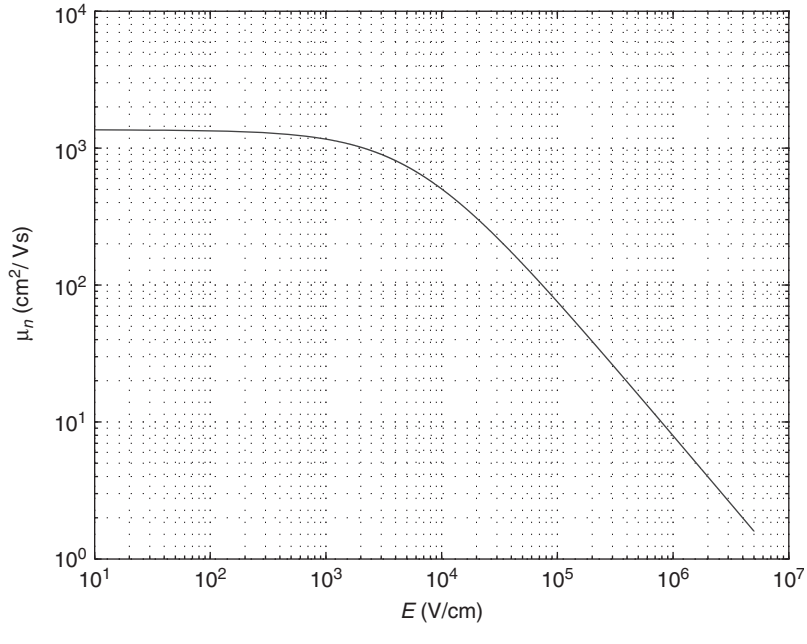


Figure 16.18 Mobility μ_n as a function of electric field intensity E for $\mu_n = 1360\,\text{cm}^2/\text{Vs}$, $v_{sat} = 8 \times 10^6\,\text{cm/Vs}$, and $T = 300\,\text{K}$ for silicon.

is nearly directly proportional to the electric field strength E because the carrier mobility is approximately constant. When the electric field intensity E approaches a sufficiently high level, the carriers collide with the lattice so frequently and the time between the collisions is so short that they do not accelerate much. At high levels of the electric field intensity E, the increase in the electron drift velocity v is very slow with increasing E because the scattering rate increases dramatically. At a very high electric field intensity E, the velocity reaches a saturation level v_{sat} and is independent of the electric field E. Therefore, the mobility is inversely proportional to the electric field intensity E. The saturation velocities of electrons and holes are characteristic parameters of each semiconductor material. For silicon, $v_{sat} = 8 \times 10^6$ cm/s. The average electron velocity is $v = v_{sat}/2$ for $E_{sat} = 6 \times 10^3$ V/cm $=$ 0.6 V/μm. For silicon carbide, $v_{sat} = 2.7 \times 10^7$ cm/s. A significant portion of the carrier transport occurs under strong electric fields. Therefore, high-field carrier transport dominates the device performance. The following approximations can be made for the average electron drift velocity v and the electron mobility μ_n.

The resistivities of n- and p-type semiconductors as functions of the electric field intensity E are given by

$$\rho_n = \frac{1}{qN_D\mu_{n0}}\left(1 + \frac{\mu_{n0}E}{v_{sat}}\right) \tag{16.67}$$

and

$$\rho_p = \frac{1}{qN_A\mu_{p0}}\left(1 + \frac{\mu_{p0}E}{v_{sat}}\right). \tag{16.68}$$

Figure 16.19 shows plots of resistivities ρ_n and ρ_p as functions of the electric field intensity E for silicon.

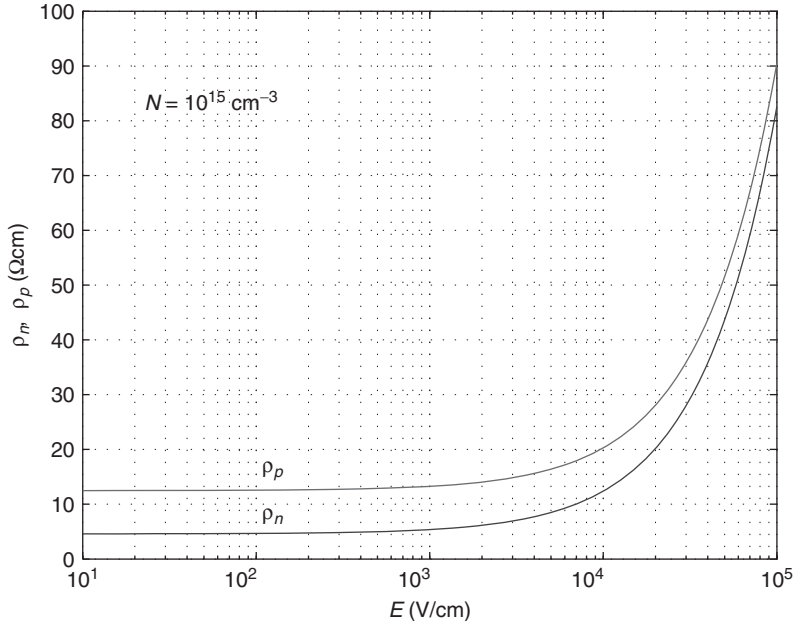


Figure 16.19 Resistivities of ρ_n and ρ_p as functions of electric field intensity E for $\mu_{n0} = 1360\,\text{cm}^2/\text{Vs}$, $\mu_{p0} = 480\,\text{cm}^2/\text{Vs}$, $v_{sat} = 8 \times 10^6$ cm/Vs, $N = 10^{15}\,\text{cm}^{-3}$, and $T = 300$ K for silicon.

Low-field range. The low-field electron mobility is approximately constant and is given by

$$\mu_n \approx \mu_{n0}, \quad \text{for } E \leq E_{LFmax} = 3 \times 10^3 \text{ V/cm}, \tag{16.69}$$

and the low-field average electron drift velocity is directly proportional to the electric field intensity E,

$$v = \mu_n E \approx \mu_{n0} E, \quad \text{for } E \leq E_{LFmax} = 3 \times 10^3 \text{ V/cm}. \tag{16.70}$$

Intermediate-field range. The intermediate-field electron mobility is field-dependent and decreases with increasing E,

$$\mu_n = \frac{\mu_{n0}}{1 + \dfrac{\mu_{n0} E}{v_{sat}}}, \quad \text{for } E_{LFmax} = 3 \times 10^3 \text{ V/cm} \leq E \leq E_{sat} = 6 \times 10^4 \text{ V/cm}. \tag{16.71}$$

The intermediate-field average drift electron velocity is

$$v = \frac{\mu_{n0} E}{1 + \dfrac{\mu_{n0} E}{v_{sat}}}, \quad \text{for } E_{LFmax} = 3 \times 10^3 \text{ V/cm} \leq E \leq E_{sat} = 6 \times 10^4 \text{ V/cm}. \tag{16.72}$$

High-Field Range. The high-field average drift electron velocity is equal to the saturation drift velocity

$$v \approx v_{sat}, \quad \text{for } E > E_{sat} = 6 \times 10^4 \text{ V/cm}. \tag{16.73}$$

Hence, the electron mobility is inversely proportional to the electric field intensity E,

$$\mu_n \approx \frac{v_{sat}}{E}, \quad \text{for } E > E_{sat} = 6 \times 10^4 \text{ V/cm}. \tag{16.74}$$

At the silicon breakdown electric field $E_{BD} = 2 \times 10^5$ V/cm and $T = 300$ K, the average electron drift mobility is

$$\mu_{n(BD)} = \frac{v_{sat}}{E_{BD}} = \frac{8 \times 10^6}{2 \times 10^5} = 40 \text{ cm}^2/\text{Vs}. \tag{16.75}$$

Hence,

$$\frac{\mu_{n0}}{\mu_{n(BD)}} = \frac{1360}{40} = 34. \tag{16.76}$$

Figure 16.20 shows the electron saturation drift velocity $v_{n(sat)}$ and hole saturation drift velocity $v_{p(sat)}$ as functions of temperature T at constant doping concentration $N = 10^{15}$ cm^{-3} for silicon.

The average drift saturation velocity decreases with increasing temperature. For silicon, the saturation velocities of electrons and holes are given by

$$v_{n(sat)} = \frac{1.434 \times 10^9}{T^{0.87}} \text{ cm/s} \tag{16.77}$$

and

$$v_{p(sat)} = \frac{1.624 \times 10^8}{T^{0.52}} \text{ cm/s}. \tag{16.78}$$

From these equations, $v_{n(sat)} = 7.44 \times 10^6$ cm/s and $v_{p(sat)} = 6.997 \times 10^6$ cm/s at $T = 150^\circ$C. The drift saturation velocity of holes is about 20 % lower than that of electrons at $T = 300$ K. However, this difference decreases with increasing temperature and both velocities are equal at $T = 500$ K.

Figures 16.21 and 16.22 show the average electron drift velocity v and the electron mobility as functions of electric field intensity E at $T = 300$ K for silicon carbide.

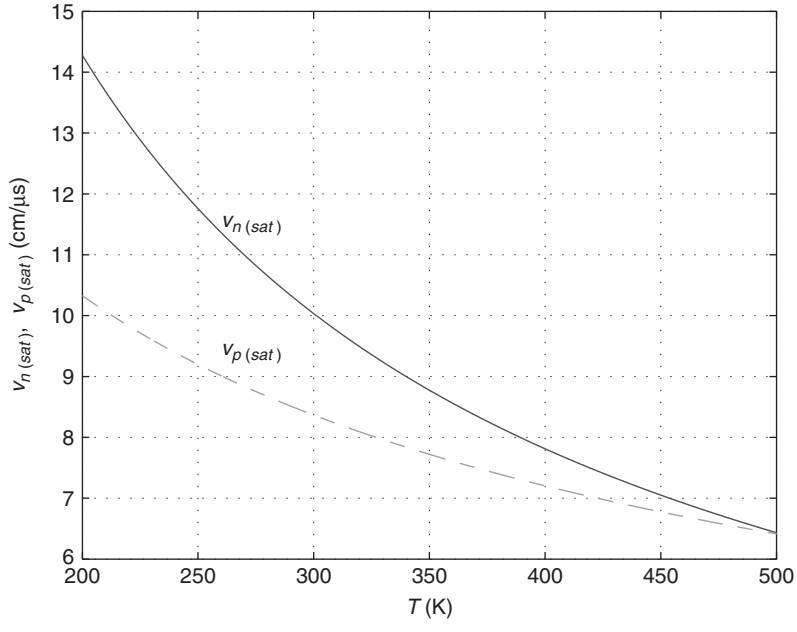


Figure 16.20 Electron saturation drift velocity $v_{n(sat)}$ and hole saturation drift velocity $v_{p(sat)}$ as functions of temperature T at constant doping concentration $N = 10^{15}\,\text{cm}^{-3}$ for silicon.

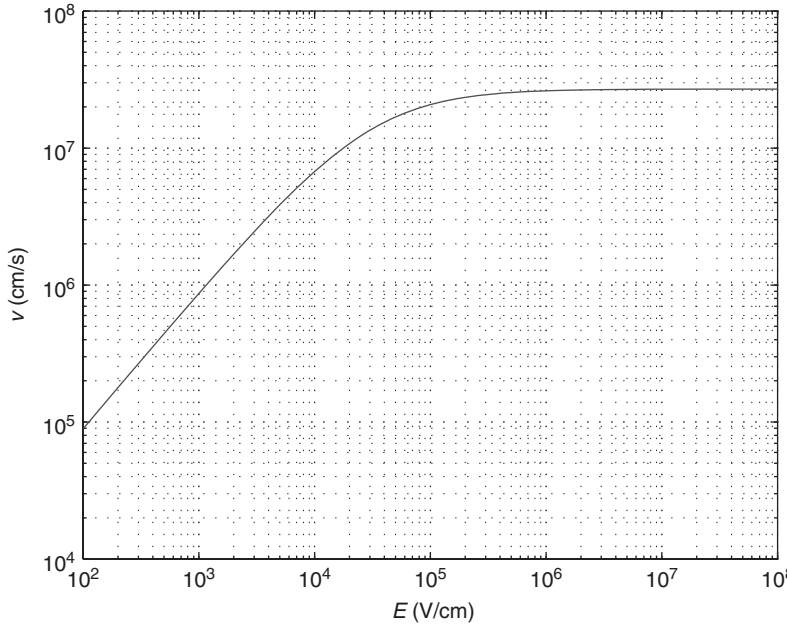


Figure 16.21 Average electron drift velocity v as a function of electric field intensity E for silicon carbide.

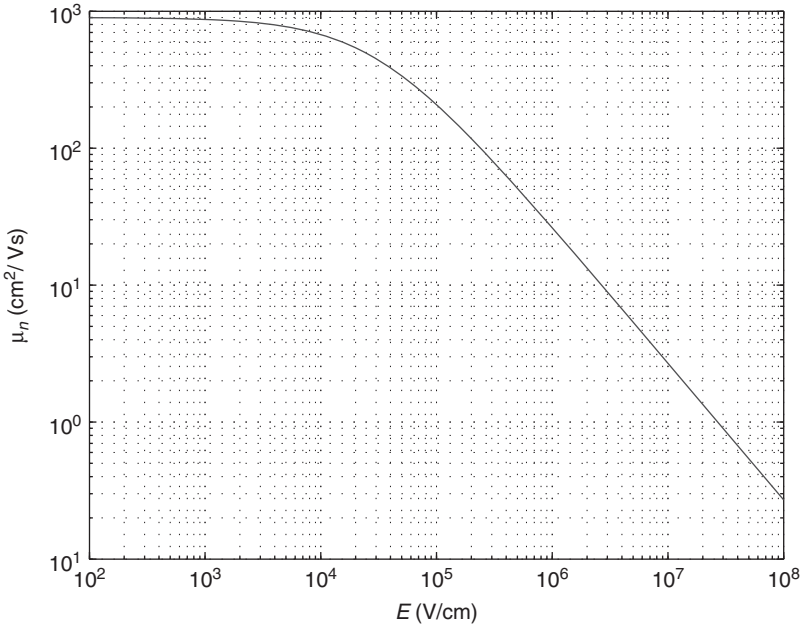


Figure 16.22 Mobility μ_n as a function of electric field intensity E for silicon carbide.

16.7 Short-channel Effects

The short-channel effects are as follows:

1. The decrease in the carrier mobility μ_n in the channel.
2. The carrier velocity saturates.
3. The decrease in the threshold voltage V_t.
4. The decrease in V_A and the increase in λ.
5. The decrease in v_{DSsat} and the increase in i_{Dsat}.

The electric field distribution in the MOSFET channel is very complex and depends on both the drain-to-source voltage v_{DS} and the gate-to-source voltage v_{GS}. The electron carrier mobility μ_n is a function of the vertical electric field in the inversion layer. As v_{GS} increases, the carrier mobility decreases. This causes the 'short-channel effect'. For low values of v_{GS}, the carrier mobility is nearly independent of the electric field E, and the drain current i_D is related to the voltage v_{GS} by the square-law characteristic. However, for higher values of v_{GS}, the high transverse electric field E perpendicular to the gate oxide causes the carrier drift velocity to saturate at v_{sat} due to degradation of carrier mobility with increasing v_{GS}, Therefore, the $i_D - v_{GS}$ characteristic becomes linear. In the saturation region, the drain-to-source voltage v_{DS} has usually dominant effect on the carrier mobility. At the edge of saturation, $v_{DS} = v_{GS} - V_t$. For the *saturation region*, the drain current at

any value of the average carrier drift velocity v is given by

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)v_{DS}^2 = \frac{1}{2}C_{ox}Wv_{DS}\mu_n\left(\frac{v_{DS}}{L}\right)$$
$$= \frac{1}{2}C_{ox}Wv_{DS}\mu_n E = \frac{1}{2}C_{ox}Wv_{DS}v$$
$$= \frac{1}{2}C_{ox}Wv_{DS}\frac{\mu_{n0}E}{1 + \dfrac{\mu_{n0}E}{v_{sat}}}, \quad \text{for } v_{DS} \geq v_{GS} - V_t, \tag{16.79}$$

where $E = v_{DS}/L$ and $v = \mu_n E$. At $v = v_{sat}$, the drain current in the *saturation region* is given by

$$i_D = \frac{1}{2}C_{ox}Wv_{sat}(v_{GS} - V_t), \quad \text{for } v_{DS} \geq v_{GS} - V_t. \tag{16.80}$$

For short-channel MOSFETs that operate in the velocity saturated region, the drain current i_D is proportional to $(v_{GS} - V_t)$ rather than to $(v_{GS} - V_t)^2$.

In the linear region, the gate-to-source voltage v_{GS} usually has a dominant effect on the carrier mobility because the drain-to-source voltage v_{DS} is low. For the *linear region*, the drain current at any average carrier drift velocity v is

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{v_{DS}^2}{2}\right] = \frac{\mu_{n0}C_{ox}}{1 + \dfrac{\mu_{n0}E}{v_{sat}}}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{v_{DS}^2}{2}\right]$$
$$= \frac{\mu_{n0}C_{ox}}{1 + \dfrac{\mu_{n0}}{v_{sat}}\dfrac{(v_{GS} - V_t)}{L}}\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{v_{DS}^2}{2}\right] = \mu_{n0}C_{ox}\left(\frac{W}{L}\right)$$
$$\times \frac{1}{1 + \theta(v_{GS} - V_t)}\left[(v_{GS} - V_t)v_{DS} - \frac{v_{DS}^2}{2}\right], \quad \text{for } v_{DS} < v_{GS} - V_t, \tag{16.81}$$

where $E = (v_{GS} - V_t)/L$ and $\theta = \mu_{n0}/(v_{sat}L)$ is the *mobility degradation coefficient* and its typical value ranges from 0.01 to 0.2 V^{-1}. The carrier mobility in the ohmic region can be described by

$$\mu_n = \frac{\mu_{n0}}{1 + \theta(v_{GS} - V_t)}. \tag{16.82}$$

The short-channel effect also reduces the MOSFET effective channel length L_{eff} and the threshold voltage V_t. As L_{eff} decreases, V_t approaches zero. In addition, λ is inversely proportional to the channel length. For this reason, the slope of the $i_D - v_{DS}$ characteristics is high in the saturation region.

Most devices operate with characteristics intermediate between the constant mobility and the constant velocity. If the constant velocity saturation dominates, the $i_D - v_{DS}$ characteristics are more evenly spaced compared to those for the long-channel, constant-mobility case.

16.8 Aspect Ratio of Power MOSFETs

The current capability of power MOSFETs increases as the aspect ratio W/L increases. The channel of power MOSFETs is short and very wide. The maximum drain saturation

current I_{Dsat} at the maximum gate-to-source voltage V_{GSmax} is given by

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GSmax} - V_t)^2. \tag{16.83}$$

For the MOSFET to operate properly as a switch, the maximum switch current I_{SMmax} must be sufficiently lower than I_{Dsat}. For example, if

$$I_{SMmax} = \frac{1}{2}aI_{Dsat} = \frac{1}{2}a\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GSmax} - V_t)^2, \tag{16.84}$$

the minimum aspect ratio of the MOSFET is given by

$$\left(\frac{W}{L}\right)_{min} = \frac{I_{SMmax}}{\frac{1}{2}a\mu_n C_{ox}(V_{GSmax} - V_t)^2} = \frac{I_{SMmax}}{\frac{1}{2}ak_p(V_{GSmax} - V_t)^2}. \tag{16.85}$$

where a is in the range 0.05–0.75 and V_{GSmax} is the maximum gate voltage. For instance, for $I_{SMmax} = 10\,\text{A}$, $V_{GSmax} = 8\,\text{V}$, $V_t = 3\,\text{V}$, $k_p = 20\,\mu\text{A/V}^2$, $L = 1\,\mu\text{m}$, and $a = 0.5$, we obtain $(W/L)_{min} = 8 \times 10^4$ and $W = 8 \times 10^4\,\mu\text{m} = 8\,\text{cm}$.

At high drain currents, the internal parasitic source resistance R_S or a current sensing resistor reduces the gate-to-source voltage $v_{GS} = v_G - R_S i_D$ and can cause considerable degradation of the MOSFET characteristics. For the saturation region with a long channel,

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(v_G - R_S i_D - V_t)^2. \tag{16.86}$$

Hence, the aspect ratio is

$$\left(\frac{W}{L}\right) = \frac{2i_D}{\mu_n C_{ox}(v_G - R_s i_D - V_t)^2}. \tag{16.87}$$

Therefore, a larger aspect ratio (W/L) may be required [11]:

$$\left(\frac{W}{L}\right)_{min} = \frac{I_{SMmax}}{a\mu_n C_{ox}\left(V_{Gmax} - \dfrac{R_S I_{SMmax}}{a} - V_t\right)^2} = \frac{I_{SMmax}}{ak_p\left(V_{Gmax} - \dfrac{R_S I_{SMmax}}{a} - V_t\right)^2}. \tag{16.88}$$

16.9 Breakdown Voltage of Power MOSFETs

The blocking voltage capability of power MOSFETs is determined by the *avalanche breakdown voltage* of the body diode, formed by the p-wells and the n^- drain region. Since this is a pn^- diode, the drift region is lightly doped, and the reverse-biased depletion region extends mostly into the lightly doped drain region and does not spread into the channel. Therefore, the voltage breakdown of power MOSFETs is determined by the avalanche voltage breakdown of the n^- side of the depletion region. In general, the *avalanche breakdown voltage* of a pn junction is given by

$$V_{BD} = \frac{\epsilon_r \epsilon_0 E_{BD}^2}{2q}\left(\frac{1}{N_D} + \frac{1}{N_A}\right), \tag{16.89}$$

where $\epsilon_0 = 8.8542 \times 10^{-14}\,\text{F/cm}$, ϵ_r is the semiconductor dielectric constant, $q = 1.60219 \times 10^{-19}\,\text{C}$ is the magnitude of the electron charge, E_{BD} is the breakdown electric field, and N_A and N_D are acceptor and donor densities, respectively. For Si, $\epsilon_{r(\text{Si})} = 11.7$, while For SiC, $\epsilon_{r(\text{SiC})} = 9.7$. For Si, the theoretical value of the breakdown electric field

E_{BD} for silicon is 300,000 V/cm and the measured value is 200,000 V/cm = 20 V/μm. For SiC, $E_{BD} = 2.2 \times 10^6$ V/cm. The band gap energy is $E_G = 1.12$ eV at $T = 300$ K for Si, and $E_G = 2.26$ eV for SiC. The breakdown voltage V_{BD} is proportional to $\sqrt{E_G}$.

For the pn$^-$ junction, the n-type drift region with donor density N_D is much more lightly doped than the p-side region with acceptor density N_A, that is, $N_D \ll N_A$. Hence, for Si n-channel power MOSFETs,

$$V_{BD(Si)} \approx \frac{\epsilon_r \epsilon_0 E_{BD}^2}{2qN_D} = \frac{11.7 \times 8.8542 \times 10^{-14} \times 200{,}000^2}{2 \times 1.602 \times 10^{-19} N_D} = \frac{1.293 \times 10^{17}}{N_D} \text{(V)}, \quad (16.90)$$

where N_D is in cm^{-3}. The breakdown voltage V_{BD} is inversely proportional to the doping density N_D. In high-voltage MOSFETs, the drain doping concentration N_D is low.

Rearrangement of the expression for the avalanche breakdown voltage for pn junction diodes given by (16.89) produces

$$\epsilon_r \epsilon_0 = \frac{2qV_{BD}N_A N_D}{(N_A + N_D)}. \quad (16.91)$$

Substituting this equation into (15.26) and setting $v_{DS} = -v_D = V_{BD}$ and $W_D = l_n$, we obtain the required minimum thickness of the depletion region of the pn junction body diode on the lightly doped n$^-$side extending into the drift region at the maximum doping concentration required to support the blocking voltage,

$$x_n = W_D = \frac{2V_{BD}}{E_{BD}}. \quad (16.92)$$

The required depletion layer thickness W_D is directly proportional to the breakdown voltage V_{BD}. In real designs, the concentration is usually lower than the maximum value. Also, the thickness W_D is usually lower that its minimum value.

For silicon MOSFETs,

$$W_{D(Si)} = \frac{2V_{BD}}{E_{BD(Si)}} = \frac{2V_{BD}}{200{,}000} = \frac{V_{BD}}{100{,}000} \text{(cm)} = \frac{V_{BD}}{10} \text{(μm)}. \quad (16.93)$$

The lowest drain thickness W_D is located between the n$^+$ substrate and the p-wells. In high-voltage MOSFETs, the drain region is thick. Some of the standard breakdown voltages ($V_{BD} = V_{DSS}$) of silicon power MOSFETs are 20, 50, 100, 200, 400, and 500 V.

For SiC n-channel power MOSFETs,

$$V_{BD(SiC)} \approx \frac{\epsilon_r \epsilon_0 E_{BD}^2}{2qN_D} = \frac{9.7 \times 8.8542 \times 10^{-14} \times 2{,}200{,}000^2}{2 \times 1.602 \times 10^{-19} N_D} = \frac{1.2974 \times 10^{19}}{N_D} \text{(V)} \quad (16.94)$$

where N_D is in cm^{-3}. The breakdown voltage V_{BD} is inversely proportional to the doping density N_D. The thickness of the drain region is

$$W_{D(SiC)} = \frac{2V_{BD}}{E_{BD(SiC)}} = \frac{2V_{BD}}{2{,}200{,}000} = \frac{V_{BD}}{1{,}100{,}000} \text{ (cm)} = \frac{V_{BD}}{110} \text{ (μm)}. \quad (16.95)$$

The ratios are

$$\frac{V_{BD(SiC)}}{V_{BD(Si)}} = \frac{1.2974 \times 10^{19}}{N_{D(SiC)}} \frac{N_{D(Si)}}{1.293 \times 10^{17}} = 100 \frac{N_{D(Si)}}{N_{D(SiC)}} \quad (16.96)$$

and

$$\frac{W_{D(Si)}}{W_{D(SiC)}} = \frac{E_{BD(SiC)}}{E_{BD(Si)}} = \frac{2{,}200{,}000}{200{,}000} = 11. \quad (16.97)$$

At the same doping concentration of the drift region N_D, the avalanche breakdown voltage of the SiC MOSFET is 100 times higher than that of the Si MOSFET. At the same breakdown voltage V_{BD}, the doping concentration of the drift region N_D of the SiC MOSFET can be 100 times higher and the drift region thickness W_D can be 11 times lower than those of the Si MOSFET.

The avalanche breakdown voltage V_{DSS} decreases as the junction temperature T_J decreases. The minimum breakdown voltage $V_{DSS(min)}$ occurs at the lowest junction temperature T_{Jmin}. At lower temperatures, the average distance between collisions, called the mean free path of charge carriers, is longer because the amplitude of the atom oscillations is lower. Therefore, the impact ionization rate is higher, yielding a lower avalanche breakdown voltage V_{BD}. The thermal coefficient of the breakdown voltage is $(\Delta V_{DSS}/V_{DSS})/\Delta T = 0.001/^{\circ}\text{C}$. The breakdown voltage $V_{BD} = V_{DSS}$ is measured at $V_{GS} = 0$ and $I_D = 0.25\,\text{mA}$. The breakdown voltage V_{DSS} depends on the defects in the semiconductor structure, especially the defects on the surface and in the curved areas, where the electric field is the strongest. Since it is impossible to predict accurately the distribution of defects, the calculations of the breakdown voltage are uncertain. Manufactures' data sheets for power MOSFETs usually give lower values of the breakdown voltage than the actual ones.

16.10 Gate Oxide Breakdown Voltage of Power MOSFETs

The electric field in the oxide increases with increasing gate-to-source voltage v_{GS}. If the electric field in the oxide becomes large enough, breakdown will occur, which causes catastrophic failure of the MOSFET. For SiO_2, the dielectric strength is $E_{BD(SiO_2)} = 6 \times 10^6\,\text{V/cm}$. The electric field in the oxide is $E_{ox} = v_{GS}/t_{ox}$. For example, if $t_{ox} = 50\,\text{nm}$, $\pm V_{GSmax} = \pm E_{BD(SiO_2)} t_{ox} = \pm 6 \times 10^6 \times 5 \times 10^{-6} = \pm 30\,\text{V}$. However, a safety margin is necessary because defects in the oxide lower the breakdown electric field $E_{BD(SiO_2)}$.

MOSFETs must be protected against electrostatic discharge. They have a very large dc input resistance $R_{in(dc)} > 4\,\text{G}\Omega$, and a small amount of static charge accumulated on the gate capacitance can cause the voltage breakdown of the oxide. Electrostatic discharge destruction of a MOSFET occurs when the gate-to-source voltage v_{GS} is high enough to puncture the gate dielectric. The arc burns a microscopic hole in the gate oxide, resulting in a gate-to-source short circuit or a high leakage current path. The high leakage current path eventually breaks down into a full short circuit. The rated maximum gate-to-source voltage V_{GSmax} is usually two to three times lower than the breakdown voltage of the oxide $V_{BD(SiO_2)}$. MOSFETs should be stored in closed conductive containers. Tables and floors should have grounded static-dissipative covering. Grounded soldering irons should be used to install MOSFETs. Conductive plastic bags are manufactured from carbon or metal-impregnated base.

16.11 Resistance of Drift Region

Neglecting the edge effects with or without terminations, the resistance of a planar drift region is given by [12]

$$R_{DR} = \frac{v_{DR}}{i_D} = \frac{4(V_{BD} + V_{bi})^2}{A\mu_n \epsilon_r \epsilon_0 E_{BD}^3} \approx \frac{4V_{BD}^2}{A\mu_n \epsilon_r \epsilon_0 E_{BD}^3}, \quad \text{for } V_{bi} \ll V_{BD}, \tag{16.98}$$

where v_{DR} is the voltage drop across the drift region, i_D is the drain current, A is the cross-sectional area of the drift region, μ_n is the bulk electron mobility, and V_{bi} is the built-in potential. The built-in potential V_{bi} ranges from 0.55 to 0.9 V for silicon junction diodes. For silicon, the low-field electron mobility $\mu_n = 1360\,\text{cm}^2/\text{Vs}$ at $N_D < 10^{15}\,\text{cm}^{-3}$ and at room temperature $T = 300\,\text{K}$, whereas the low-field hole mobility is $\mu_p = 480\,\text{cm}^2/\text{Vs}$ at $N_A < 10^{15}\,\text{cm}^{-3}$ at room temperature $T = 300\,\text{K}$. The electron mobility μ_n decreases when N_D, T, and E increase. For example, $\mu_n = 576\,\text{cm}^2/\text{Vs}$ at $V_{BD} = 600\,\text{V}$ and $T = 150^\circ\text{C}$.

The *specific resistance of the drift region* with the doping concentration and thickness required to support the desired breakdown voltage is given by

$$S = \frac{v_{DR}}{J} = \frac{v_{DR}}{i_D/A} = AR_{DR} = \frac{4V_{BD}^2}{\mu_n \epsilon_r \epsilon_0 E_{BD}^3}, \tag{16.99}$$

where $J = i_D/A$ is the drain current density. The specific drift on-resistance is inversely proportional to the cube of the breakdown electric field strength E_{BD} and can be reduced if the semiconductor has a higher breakdown electric field strength (e.g., SiC). For silicon devices, the specific resistance of the drift region is

$$S_{(Si)} = AR_{DR} = \frac{4V_{BD}^2}{1360 \times 11.7 \times 8.8542 \times 10^{-14} \times 200{,}000^3} = 3.55 \times 10^{-7} V_{BD}^2 \ (\Omega\text{cm}^2). \tag{16.100}$$

Figure 16.23 shows AR_{DR} as a function of V_{BD}.

The MOSFET drift specific resistance increases with increasing temperature T,

$$S = AR_{DR} = \frac{4V_{BD}^2 \left(\dfrac{T}{300}\right)^{2.4}}{\mu_{n0} \epsilon_r \epsilon_0 E_{BD}^3}. \tag{16.101}$$

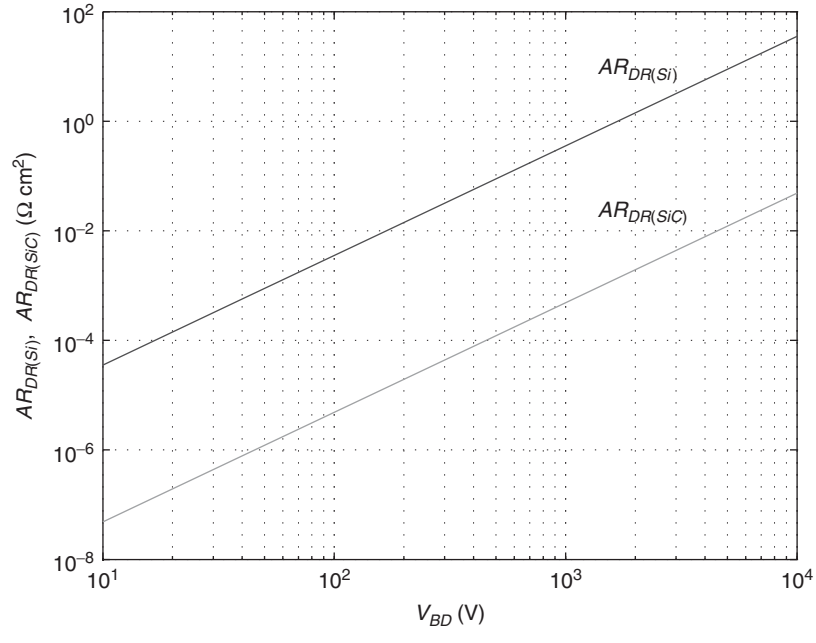


Figure 16.23 Specific drift resistance AR_{DR} as a function of breakdown voltage V_{BD} for silicon and silicon carbide.

For silicon,

$$S_{(Si)} = AR_{DR} = \frac{4V_{BD}^2 \left(\frac{T}{300}\right)^{2.4}}{1360\epsilon_r \epsilon_0 E_{BD}^3}. \tag{16.102}$$

As the temperature T is increased by 100°C, from 27°C to 127°C, the specific drain resistance S increases by a factor of 2:

$$\frac{S(T + 100^\circ)}{S(T)} = \left(\frac{400}{300}\right)^{2.4} = 2. \tag{16.103}$$

Example 16.1

The breakdown voltage V_{BD} of a Si power MOSFET is 500 V and $R_{DR} = 0.6\,\Omega$. Calculate N_D, W_D, S, and A.

Solution. The maximum donor density in the drift region is

$$N_D = \frac{1.293 \times 10^{17}}{V_{BD}} = \frac{1.293 \times 10^{17}}{500} = 2.586 \times 10^{14}\,\text{cm}^{-3}. \tag{16.104}$$

The minimum thickness of the drift region is

$$W_{D(Si)} = \frac{V_{BD}}{10}\ (\mu\text{m}) = \frac{500}{10} = 50\,\mu\text{m}. \tag{16.105}$$

The specific drift resistance is

$$S_{(Si)} = AR_{DR} = 3.55 \times 10^{-7} V_{BD}^2\ (\Omega\text{cm}^2) = 3.55 \times 10^{-7} \times (500)^2 = 88.75 \times 10^{-3}\,\Omega\text{cm}^2. \tag{16.106}$$

Hence, the cross-sectional area of the drift region of the power MOSFET is

$$A = \frac{S_{(Si)}}{R_{DR}} = \frac{88.75 \times 10^{-3}}{0.6} = 0.1479\,\text{cm}^2. \tag{16.107}$$

Silicon carbide has the following properties: $\epsilon_{r(SiC)} = 9.7$, $E_{BD} = 2.2 \times 10^6$ V/cm, the band gap energy $E_G = 3.26$ eV, $\mu_n = 800\,\text{cm}^2/\text{Vs}$ at $V_{BD} = 100$ V and $T = 27^\circ$C, $\mu_n = 148\,\text{cm}^2/\text{Vs}$ at $V_{BD} = 600$ V and $T = 150^\circ$C. For SiC MOSFETs, the specific resistance of the drift region is given by

$$S_{(SiC)} = AR_{DR} = \frac{4V_{BD}^2}{\mu_n \epsilon_r \epsilon_0 E_{BD}^3} = \frac{4V_{BD}^2}{148 \times 9.7 \times 8.8542 \times 10^{-14} \times (2.2 \times 10^6)^3}$$
$$= 2.95 \times 10^{-9} V_{BD}^2\ (\Omega\text{cm}^2). \tag{16.108}$$

At $V_{BD} = 600$ V and $T = 150^\circ$C, $\mu_{n(Si)} = 576\,\text{cm}^2/\text{Vs}$ and $\mu_{n(Si)} = 148\,\text{cm}^2/\text{Vs}$. The ratio of specific resistance for silicon to the specific resistance of silicon carbide is given by

$$\frac{S_{(Si)}}{S_{(SiC)}} = \frac{\mu_{n(SiC)} \epsilon_{r(SiC)} E_{BD(SiC)}^3}{\mu_{n(Si)} \epsilon_{r(Si)} E_{BD(Si)}^3} = \frac{148 \times 9.7 \times (22 \times 10^5)^3}{576 \times 11.7 \times (2 \times 10^5)^3} = 283.53. \tag{16.109}$$

The thermal conductivity of silicon is $G_{th(Si)} = 1.5$ W/cmK and the thermal conductivity of silicon carbide is $G_{th(SiC)} = 4.56$ W/cmK. Thus, the thermal conductivity of silicon carbide is about 3 times higher than that of silicon. The thermal junction-to-case resistance

of silicon devices is typically $\theta_{JC(Si)} = 1.5^{\circ}$C/W and that of silicon carbide devices is $\theta_{JC(SiC)} = 0.02^{\circ}$C/W.

Most of the resistance that controls the drain current flow during conduction arises in the same portion of the power MOSFET that supports the high voltage during the blocking state. A high breakdown voltage requires a low doping concentration of the drift region, whereas a low resistance of the drift region requires a high doping concentration. Most power MOSFETs are n-channel devices because the mobility of electrons is higher than that of holes by a factor of $\mu_n/\mu_p = 1360/480 = 2.833$ for silicon.

Example 16.2

The breakdown voltage V_{BD} of a SiC power MOSFET is 500 V and $A = 0.1479\,\text{cm}^2$. Calculate N_D, W_D, S, and R_{DR}.

Solution. The required donor density in the drift region is

$$N_D = \frac{1.2974 \times 10^{19}}{V_{BD}} = \frac{1297.4 \times 10^{16}}{500} = 2.59 \times 10^{16}\,\text{cm}^{-3}. \tag{16.110}$$

The required thickness of the drift region is

$$W_{D(SiC)} = \frac{V_{BD}}{110}\ (\mu\text{m}) = \frac{500}{110} = 4.55\,\mu\text{m}. \tag{16.111}$$

The specific drift resistance is

$$S_{(SiC)} = AR_{DR} = 2.95 \times 10^{-9} V_{BD}^2\ (\Omega\text{cm}^2) = 2.95 \times 10^{-9} \times (500)^2 = 73.75 \times 10^{-5}\ \Omega\text{cm}^2. \tag{16.112}$$

Hence, the expected resistance of the drift region of the SiC power MOSFET is

$$R_{DR} = \frac{S}{A} = \frac{73.75 \times 10^{-5}}{0.1479} = 4.986 \times 10^{-3} \approx 5\,\text{m}\Omega. \tag{16.113}$$

16.12 Figures-of-merit

Baliga's figure-of-merit for semiconductor materials is given by [4]

$$BFOM = \epsilon_r \epsilon_0 \mu E_{BD}^3. \tag{16.114}$$

It can be used to compare the performance of various semiconductor materials for power device fabrication. For silicon at $T = 150^{\circ}\text{C} = 423$ K and $V_{BD} = 600$ V, $\mu_{n(BD)} = 40\,\text{cm}^2/$Vs. Hence,

$$BFOM_{(Si)} = \epsilon_{r(Si)} \epsilon_0 \mu_{n(Si)} E_{BD(Si)}^3 = 11.7 \times 8.8542 \times 10^{-14} \times 40 \times (2 \times 10^5)^3 = 0.332\,\text{MW/cm}^2. \tag{16.115}$$

For silicon carbide at $T = 423$ K and $V_{BD} = 600$ V, $\mu_n = 148\,\text{cm}^2/$Vs. Hence,

$$BFOM_{(SiC)} = \epsilon_{r(SiC)} \epsilon_0 \mu_{n(SiC)} E_{BD(SiC)}^3 = 9.7 \times 8.8542 \times 10^{-14} \times 148 \times (22 \times 10^5)^3 = 1353.5\,\text{MW/cm}^2. \tag{16.116}$$

The ratio of these two factors is

$$\frac{BFOM_{(SiC)}}{BFOM_{(Si)}} = \frac{\epsilon_{r(SiC)}}{\epsilon_{r(Si)}} \frac{\mu_{n(SiC)}}{\mu_{n(SiC)}} \left(\frac{E_{BD(SiC)}}{E_{BD(Si)}} \right)^3 = \frac{1353.5}{0.332} = 4080. \tag{16.117}$$

Another figure-of-merit of semiconductor materials is given by

$$F_M = \frac{V_{BD}^2}{S} = \frac{V_{BD}^2}{AR_{DR}} = \frac{\epsilon_r \epsilon_0 \mu_n E_{BD}^3}{4} = \frac{BFOM}{4} \left(\frac{\text{MW}}{\text{cm}^2} \right). \tag{16.118}$$

For silicon, $F_{M(Si)} = 0.083\,\text{MW/cm}^2$ and for silicon carbide, $F_{M(SiC)} = 338.37\,\text{MW/cm}^2$.

Jonhson's figure-of-merit for semiconductor materials is given by

$$JFM = \frac{E_{BD}^2 v_{sat}}{4\pi^2}. \tag{16.119}$$

The JFM for SiC is 260 time higher than that for Si.

A figure-of-merit for power MOSFETs is defined here as

$$K_M = \frac{V_{DSS} I_{DMAX}}{r_{DS}}, \tag{16.120}$$

where I_{DMAX} is the maximum drain current. For example, the IRF540 has $V_{DSS} = 100\,\text{V}$, $I_{DMAX} = 28\,\text{A}$, and $r_{DS} = 0.077\,\Omega$. Hence,

$$K_M = \frac{V_{DSS} I_{DMAX}}{r_{DS}} = \frac{100 \times 28}{0.077} = 36{,}364\,\text{A}^2. \tag{16.121}$$

A figure-of-merit that takes into account the capacitance C_{gs} is given by

$$K_C = \frac{V_{DSS} I_{DMAX}}{r_{DS} C_{gs}} = \frac{K_M}{C_{gs}}. \tag{16.122}$$

For example, the IRF540 has $C_{gs} = 1620$ pF, which gives

$$K_C = \frac{K_M}{C_{gs}} = \frac{36{,}364}{1620 \times 10^{-12}} = 22.447 \times 10^6\,\text{A}^2/\text{F}. \tag{16.123}$$

16.13 On-resistance of Power MOSFETs

The overall MOSFET on-resistance r_{DS} consists of the channel resistance R_{ch}, the accumulation region resistance R_a, the neck resistance R_n, and the drift resistance R_{DR},

$$r_{DS} = R_{Ch} + R_a + R_n + R_{DR}, \tag{16.124}$$

as shown in Figure 16.24. Additional resistances include the n^+ substrate resistance, n^+ source diffusion region resistance, die metalization resistances, bond wire resistances, and external lead resistances.

16.13.1 Channel Resistance

The large-signal channel resistance can be obtained from the MOSFET characteristics for the linear region,

$$R_{Ch} = \frac{v_{DS}}{i_D} = \frac{1}{K[2(v_{GS} - V_t) - v_{DS}]} \approx \frac{1}{2K(v_{GS} - V_t)} = \frac{L}{\mu_n C_{ox} W (v_{GS} - V_t)}, \tag{16.125}$$

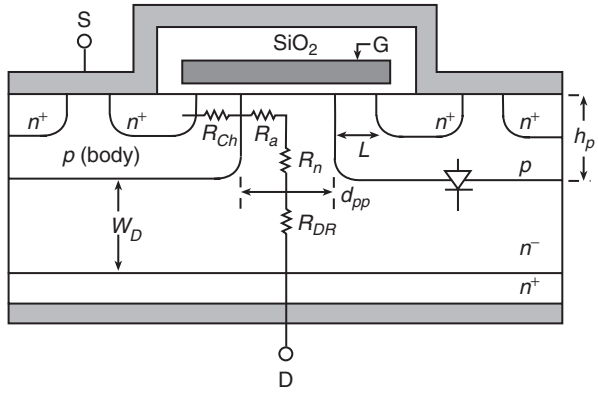


Figure 16.24 Components of on-resistance r_{DS} for power MOSFETs.

where $v_{DS} \ll 2(v_{GS} - V_t)$. The channel resistance R_{Ch} decreases as the channel length L decreases, the channel width W increases, and the gate-to-source voltage v_{GS} increases. Taking the short-channel effect into account, the channel resistance is given by

$$R_{Ch(sc)} = \frac{v_{DS}}{i_D} = \frac{1}{\mu_n C_{ox}} \left(\frac{L}{W}\right) \left(\theta + \frac{1}{v_{GS} - V_t}\right), \tag{16.126}$$

where $\theta = 0.01$ to $0.2\,\text{V}^{-1}$. Figure 16.25 show the long-channel resistance R_{Ch} and short-channel resistance $R_{Ch(sc)}$ as a function of voltage $v_{GS} - V_t$. The short-channel resistance is higher than the long-channel resistance.

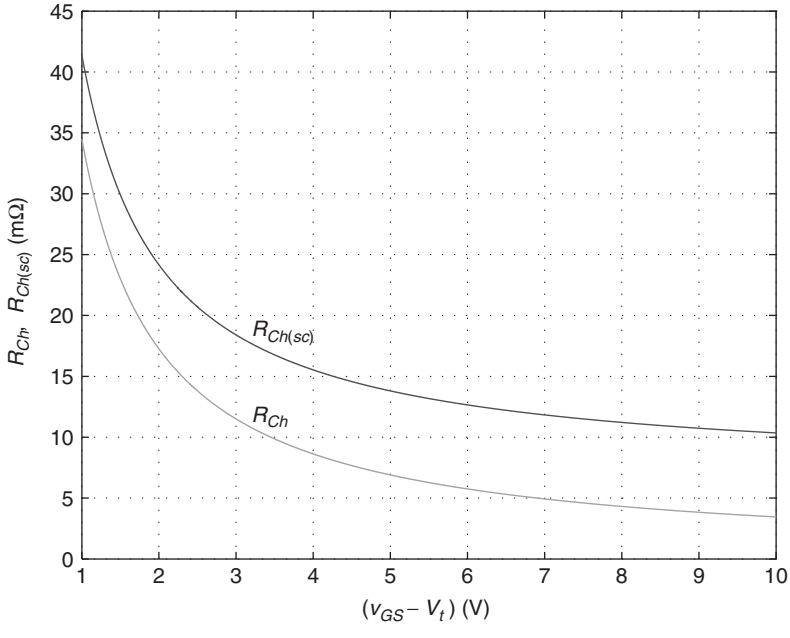


Figure 16.25 Long-channel resistance R_{Ch} and short-channel resistance $R_{Ch(sc)}$ as functions of voltage $v_{GS} - V_t$ at $\mu_n = 600\,\text{cm}^2/\text{Vs}$, $C_{ox} = 34.5\,\text{nF/cm}^2$, $W/L = 1.4 \times 10^6$, $V_t = 3.5\,\text{V}$, $\theta = 0.2\,\text{V}^{-1}$ for power MOSFET.

16.13.2 Accumulation Region Resistance

A top view of the accumulation region is shown in Figure 16.26. The resistance of the accumulation region can be determined using the equation for the channel resistance. The longest path for the drain current in the accumulation region is equal to $d_{pp}/2$ and the shortest path is zero, where d_{pp} is the distance between the p-wells. Therefore, the average length of the path for the drain current in the accumulation region is $L_{a(av)} = d_{pp}/4$. Hence, the resistance of the accumulation region is expressed by

$$R_a = \frac{v_a}{i_D} = \frac{L_{a(av)}}{\mu_n C_{ox} W (v_{GS} - V_t)} = \frac{d_{pp}}{4\mu_n C_{ox} W (v_{GS} - V_t)} = \frac{d_{pp}}{4k_p W (v_{GS} - V_t)}. \quad (16.127)$$

16.13.3 Neck Region Resistance

The neck region resistance is

$$R_n = \rho_n \frac{h_p}{A_n} = \frac{h_p}{q\mu_n N_D A_n} = \frac{h_p}{q\mu_n N_D (W d_{pp}/2 + n d_{pp}^2)} \quad (16.128)$$

where h_p is the height of the p-well, d_{pp} is the distance between the p-wells, W_1 is the channel width of a single cell, and n is the number of cells. The neck area of a single square cell is given by

$$A_{n1} = 2d_{pp}\left(\frac{W_1}{4}\right) + d_{pp}^2, \quad (16.129)$$

resulting in the neck area for n cells,

$$A_n = nA_{n1} = 2(nW_1 d_{pp}/4) + nd_{pp}^2 = Wd_{pp}/2 + nd_{pp}^2. \quad (16.130)$$

The resistivity of the neck and drift regions is

$$\rho_n = \frac{1}{q\mu_n N_D}. \quad (16.131)$$

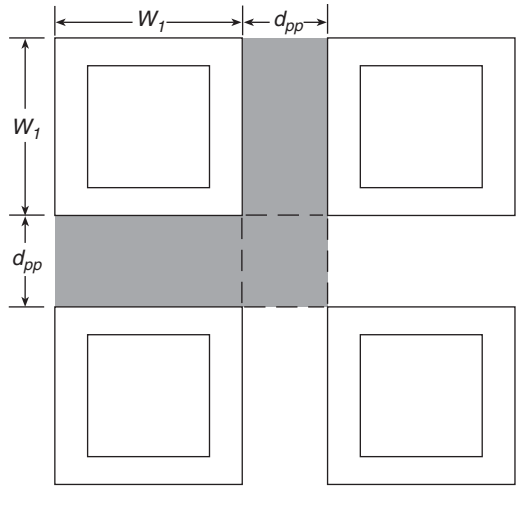


Figure 16.26 Top view of accumulation region.

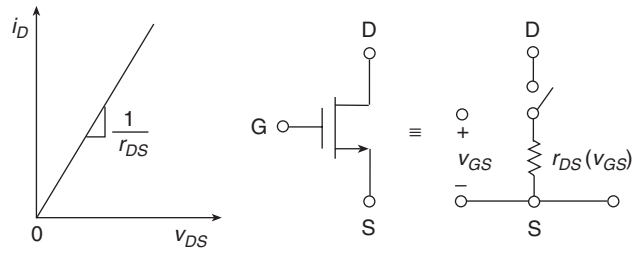


Figure 16.27 Piecewise linear model of the MOSFET operated as a switch in the linear and cutoff regions with the voltage-controlled on-resistance r_{DS}.

The drift region resistivity can be controlled by the addition of dopants into the silicon lattice that contribute either electrons or holes to the conduction process when ionized.

16.13.4 Drift Region Resistance

Assuming that the current through the drift region is uniformly distributed, the drift region resistance is described by

$$R_{DR} = \rho_n \frac{W_D}{A} = \frac{W_D}{q\mu_n N_D A} = \frac{W_D}{q\mu_{n0} N_D A} \left(\frac{T}{300}\right)^{2.4}, \tag{16.132}$$

where W_D is the drift region thickness and A is the drain area. In reality, the current density is higher between the p-wells and lower beneath the p-wells due to the current-spreading effect. Therefore, the effective cross-sectional area of the drift region A is smaller than the die area A_d and the drift region resistance is higher than that given by (16.132). For example, for MOSFETs with $V_{BD} = 200\,\text{V}$, the actual drift resistance R_{DR} is increased by about 70 %.

In high-voltage power MOSFETs with $V_{DSS} \geq 400\,\text{V}$, the drift region is lightly doped and thick, and therefore its resistance R_{DR} dominates the overall resistance r_{DS} in silicon MOSFETs. The drift resistance is independent of the gate-to-source voltage. For example, an IRFPG50 power MOSFET has $V_{DSS} = 1000\,\text{V}$, $I_{SMmax} = 6.1\,\text{A}$, and $r_{DS} = 2\,\Omega$. In low-voltage MOSFETs with $V_{DSS} \leq 100\,\text{V}$, the channel resistance R_c is from $0.3r_{DS}$ to $0.5r_{DS}$. The channel resistance depends on the gate-to-source voltage, and a stronger gate drive reduces R_c and therefore also r_{DS}.

Typically, the silicon MOSFET on-resistance r_{DS} doubles as the temperature rises by 100 °C because the electron mobility decreases with increasing temperature. As the temperature increases from T_1 to T_2, the increase in the silicon MOSFET on-resistance can be approximated by

$$r_{DS}(T_2) = r_{DS}(T_1) \times 2^{\frac{T_2 - T_1}{100}}. \tag{16.133}$$

Figure 16.27 shows a piecewise linear model of the MOSFET as a switch with on-resistance r_{DS}.

Example 16.3

Design a silicon power MOSFET with square cells to meet the following specifications: $V_{DSS} = 100\,\text{V}$, $I_{SMmax} = 28\,\text{A}$, $r_{DS} \leq 0.14\,\Omega$, and $k_p = \mu_n C_{ox} = 20.7\,\mu\text{A/V}^2$.

Solution. Assume $a = I_{SMmax}/I_{Dsat} = 0.05$, $V_t = 3.5\,\text{V}$, and $V_{GSmax} = 10\,\text{V}$. Hence, we obtain the saturation current

$$I_{Dsat} = \frac{I_{SMmax}}{a} = \frac{28}{0.05} = 560\,\text{A}, \tag{16.134}$$

and the minimum aspect ratio

$$\left(\frac{W}{L}\right)_{min} = \frac{I_{SMmax}}{\frac{1}{2}ak_p(V_{GSmax} - V_t)^2} = \frac{28}{\frac{1}{2} \times 0.05 \times 20.7 \times 10^{-6} \times (10 - 3.5)^2} = 1.28 \times 10^6. \tag{16.135}$$

Let $(W/L) = 1.4 \times 10^6$. Assume the channel length $L = 0.7\,\mu\text{m}$, the width of the p-well $W_p = 20\,\mu\text{m}$, and the distance between the p-wells $d_{pp} = 10\,\mu\text{m}$. Hence, the channel width is

$$W = (W/L)L = 1.4 \times 10^6 \times 0.7 = 1 \times 10^6\,\mu\text{m} = 1\,\text{m}. \tag{16.136}$$

The channel width of a single cell is

$$W_1 = 4W_p = 4 \times 20 = 80\,\mu\text{m}. \tag{16.137}$$

The number of cells is

$$n = \frac{W}{W_1} = \frac{1}{80 \times 10^{-6}} = 12{,}500. \tag{16.138}$$

The area of all cells is

$$\begin{aligned} A_c &= n(W_p + d_{pp})^2 = 1.25 \times 10^4 \times [(20 + 10) \times 10^{-6}]^2 = 11.25 \times 10^{-6}\,\text{m}^2 \\ &= 11.25 \times 10^{-2}\,\text{cm}^2 = 11.25\,\text{mm}^2. \end{aligned} \tag{16.139}$$

Assuming that the source and gate pads and the field guard rings will occupy 25 % of the chip, the die area is

$$A_{die} = 1.25A_c = 1.25 \times 11.25 = 14\,\text{mm}^2. \tag{16.140}$$

Since the surface electron mobility in the channel is $\mu_n = 600\,\text{cm}^2/\text{Vs} = 0.06\,\text{m}^2/\text{Vs}$, the oxide capacitance per unit area is

$$C_{ox} = \frac{k_p}{\mu_n} = \frac{20.7 \times 10^{-6}}{0.06} = 3.45 \times 10^{-4}\,\text{F/m}^2 = 34.5\,\text{nF/cm}^2. \tag{16.141}$$

Thus, the oxide thickness is

$$t_{ox} = \frac{\epsilon_{r(SiO_2)}\epsilon_0}{C_{ox}} = \frac{3.9 \times 8.8542 \times 10^{-14}}{34.5 \times 10^{-9}} = 0.1\,\mu\text{m}. \tag{16.142}$$

The maximum doping concentration of the drift region is given by

$$N_{Dmax(Si)} = \frac{1.293 \times 10^{17}}{V_{BD}} = \frac{1.293 \times 10^{17}}{100} = 1.293 \times 10^{15}\,\text{cm}^{-3}. \tag{16.143}$$

Pick $N_D = 10^{15}\,\text{cm}^{-3} = 10^{21}\,\text{m}^{-3}$ and doping concentration of the p-wells $N_A = 10^{16}\,\text{cm}^{-3} = 10^{22}\,\text{m}^{-3}$.

The minimum thickness of the drift region is

$$W_{Dmin} = \frac{V_{BD}}{10} = \frac{100}{10} = 10\,\mu\text{m}. \tag{16.144}$$

Pick $W_D = 12\,\mu\text{m}$.

The long-channel resistance at $V_{GS} = 10\,\text{V}$ is

$$R_{Ch} = \frac{1}{k_p\left(\frac{W}{L}\right)(V_{GS} - V_t)} = \frac{1}{20.7 \times 10^{-6} \times 1.4 \times 10^6 \times (10 - 3.5)} = 5.3\,\text{m}\Omega. \quad (16.145)$$

The resistance of the accumulation region is given by

$$R_a = \frac{1}{4k_p\left(\frac{W}{d_{pp}}\right)(v_{GS} - V_t)} = \frac{1}{4 \times 20.7 \times 10^{-6} \times (10^6/10) \times (10 - 3.5)} = 18.58\,\text{m}\Omega. \quad (16.146)$$

Assuming that the thickness of the p-wells is $h_p = 3\,\mu\text{m}$, and using the bulk mobility $\mu_n = 1360\,\text{cm}^2/\text{Vs}$, we can calculate the neck region resistances as

$$\begin{aligned} R_n &= \frac{h_p}{q\mu_n N_D(Wd_{pp}/2 + nd_{pp}^2)} \\ &= \frac{3 \times 10^{-6}}{1.602 \times 10^{-19} \times 0.136 \times 10^{21}[(1 \times 10 \times 10^{-6})/2 + 1.25 \times 10^4 \times (10 \times 10^{-6})^2)]}. \\ &= 22\,\text{m}\Omega. \end{aligned} \quad (16.147)$$

Assuming that $A = A_c$, the drift region resistance is given by

$$R_{DR} = \frac{W_D}{q\mu_n N_D A} = \frac{12 \times 10^{-6}}{1.602 \times 10^{-19} \times 0.136 \times 10^{21} \times 11.25 \times 10^{-6}} = 49\,\text{m}\Omega. \quad (16.148)$$

The current density in the drift region is not uniform due to current-spreading effect. Assuming the current-spreading coefficient $F_{cs} = 1.8$, the drift resistance is

$$R_{DR} = 1.8 \times 49 = 88.2\,\text{m}\Omega. \quad (16.149)$$

The MOSFET on-resistance is

$$r_{DS} = R_{Ch} + R_a + R_n + R_{DR} = 5.3 + 18.58 + 22 + 88.2 = 134.08\,\text{m}\Omega. \quad (16.150)$$

16.14 Capacitances of Power MOSFETs

Figure 16.28 shows capacitances of the power MOSFET. Conducting surfaces separated by a dielectric SiO_2 form capacitance. The body diode depletion layer also represents a junction capacitance. These capacitances govern the MOSFET transient performance because they are charged and discharged during turn-on and turn-off transitions. The rate of charging and discharging depends on the capacitance values and the impedances in the charging and discharging paths. MOSFETs exhibit no minority-carrier storage time.

16.14.1 Gate-to-source Capacitance

The gate-to-source capacitance C_{gs} consists of (1) the gate-to-source metal capacitance C_{gm}, (2) the gate-to-p-well capacitance C_{gp}, and (3) the gate-to-n^+ source diffusion overlap capacitance C_{gn}. The gate length of a single square cell is

$$l_g = d_{pp} + 2(L + L_n), \quad (16.151)$$

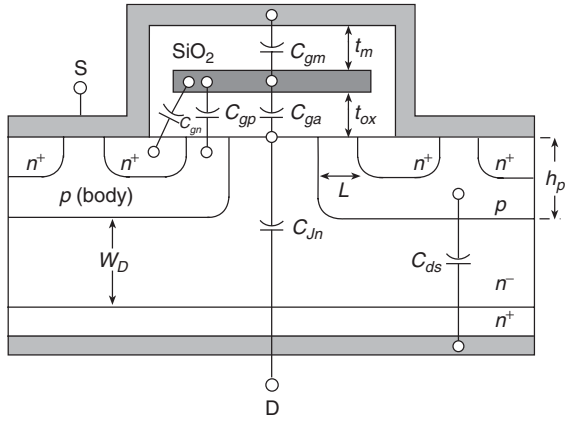


Figure 16.28 Capacitances of power MOSFET.

resulting in the gate area of a single square cell,

$$A_{G1} = l_g^2 = [d_{pp} + 2(L + L_n)]^2, \tag{16.152}$$

and the gate area of all cells,

$$A_G = nA_{G1} = n[d_{pp} + 2(L + L_n)]^2, \tag{16.153}$$

where d_{pp} is the distance between the p-wells, L is the channel length, L_n is the gate-to-source overlap length, and n is the total number of cells. The gate polysilicon-to-metal capacitance is given by

$$C_{gm} = \frac{\epsilon_{ox} A_G}{t_m} = \frac{\epsilon_{ox} n[d_{pp} + 2(L + L_n)]^2}{t_m}, \tag{16.154}$$

where $\epsilon_{ox} = \epsilon_{r(ox)}\epsilon_0$ and t_m is the distance between the gate and the upper source metallization. The capacitance C_{gm} is linear. To reduce this capacitance, the thickness of the insulating layer t_m should be large.

The gate-to-p-well capacitance is

$$C_{gp} = \frac{\epsilon_{ox} A_p}{t_{ox}} = \frac{\epsilon_{ox} LW}{t_{ox}} = C_{ox} LW, \tag{16.155}$$

where $A_p = LW$ is the channel area of all cells for any shape of the cells. When v_{DS} increases at $v_{GS} < V_t$, the depletion region in the p-type body diffusion widens. The further the depletion region moves towards the n^+ source diffusion, the lower C_{gp} becomes. Only the undepleted region of mobile charge at the surface of body diffusion below the polysilicon gate can form the lower plate of C_{gp}. Since the depletion region spreads less than 10 % across the width of the heavily doped p-type body region as v_{DS} is varied from zero to the rated breakdown value, the change in C_{gp} is small. For $v_{GS} < V_t$, the p-well and the n^+ source form a reverse-biased pn^+ junction diode. The junction capacitance of this diode decreases as the voltage v_{GS} becomes more negative. The junction capacitance and the capacitance C_{gp} are connected in series. This capacitance is nonlinear and decreases as v_{GS} decreases and is below V_t. For $v_{GS} > V_t$, the n-channel is formed, and C_{gp} is connected directly to the source. The capacitance C_{gp} is nonlinear.

The gate-to-n^+ source diffusion overlap capacitance is

$$C_{gn} = \frac{\epsilon_{ox} A_S}{t_{ox}} = \frac{\epsilon_{ox} WL_n}{t_{ox}} = C_{ox} WL_n, \tag{16.156}$$

where $A_S = WL_n$ is the overlapping area of the gate electrode over the n^+ source.

The gate-to-source capacitance is the parallel combination of the three capacitances,

$$C_{gs} = C_{gm} + C_{gp} + C_{gn}. \tag{16.157}$$

This capacitance is approximately linear.

16.14.2 Drain-to-source Capacitance

The drain-to-source capacitance C_{ds} is the body-to-drain capacitance, which is the body diode junction and diffusion capacitance. For the drain voltage $v_{DS} \geq 0$, the diode is reverse biased and the diode capacitance is dominated by the small-signal junction capacitance. The area of all p-wells is

$$A_J = n(W_p + 2h_p)^2, \tag{16.158}$$

where W_p is the width of the p-well and h_p is the thickness of the p-well. The zero-bias body diode junction capacitance is

$$C_{J0} = A_J\sqrt{\frac{q\epsilon_{r(Si)}\epsilon_0 N_D}{2V_{bi}}} = n(W_p + 2h_p)^2\sqrt{\frac{q\epsilon_{r(Si)}\epsilon_0 N_D}{2V_{bi}}}. \tag{16.159}$$

The junction body diode capacitance is given by

$$C_{ds} = C_J = \frac{C_{J0}}{\left(1 + \dfrac{V_{DS}}{V_{bi}}\right)^m} \tag{16.160}$$

where $m = \frac{1}{3}$ for linearly graded junctions and $m = \frac{1}{2}$ for step junctions. The minimum junction capacitance C_{dsmin} occurs at the maximum drain-to-source voltage v_{DSmax}. For $m = \frac{1}{2}$, the drain-to-source capacitance $C_{ds}(v_{DS})$ at the drain-to-source voltage is given by

$$C_{ds}(v_{DS}) = C_{dsmin}\sqrt{\frac{v_{DSmax} + V_{bi}}{v_{DS} + V_{bi}}} \approx C_{dsmin}\sqrt{\frac{v_{DSmax}}{v_{DS}}}. \tag{16.161}$$

For the drain voltage $v_{DS} < 0$, the diode is forward biased and the diode capacitance is dominated by the small-signal diffusion capacitance,

$$C_{ds} = C_D + C_J \approx C_D = \tau_p\frac{|I_D|}{nV_T}. \tag{16.162}$$

The body diode exhibits reverse recovery during the turn-off transition of transistor negative current due to the excess charge stored in the diffusion capacitance C_D. The capacitance C_{ds} is highly nonlinear.

16.14.3 Gate-to-drain Capacitance

The gate-to-drain capacitance C_{gd} varies with the drain-to-gate voltage v_{DG}. Three regions of the voltage v_{DG} should be considered for capacitance C_{gd}.

In the first region, the voltage range is $-v_{GS} \leq v_{DG} \leq 0$. Here, the MOSFET is ON, $v_{GS} \approx$ 8 to 10 V, $v_{DG} = v_{DS(ON)} - v_{GS} \approx -v_{GS} < 0$, the depletion region of the body diode is very narrow, and the width of the neck region is nearly d_{pp}. Hence, the area of the neck region A_n is large, resulting in a large gate polysilicon-oxide-neck semiconductor capacitance

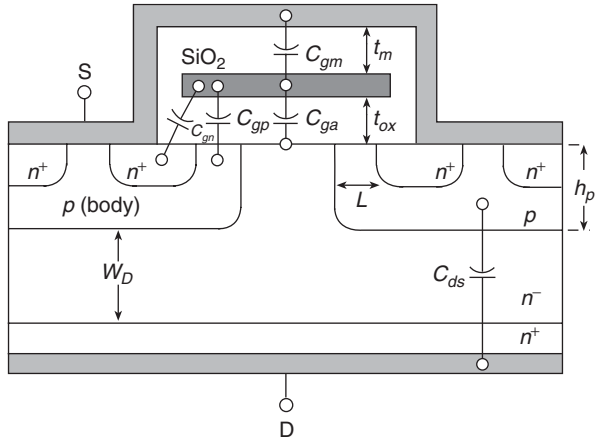


Figure 16.29 Gate-to-drain capacitance C_{gd} of power MOSFET for $v_{DS} = v_{DS(ON)}$, resulting in $x_n \approx 0$.

$C_{ga} = C_{gd}$. Figure 16.29 shows the gate-to-drain capacitance C_{gd} for $v_{DS} = v_{DS(ON)}$ and $v_{DG} \approx -v_{GS} < 0$. The area of the neck for the single square cell is

$$A_{n1} = \frac{2W_1 d_{pp}}{4} + d_{pp}^2 = \frac{W_1 d_{pp}}{2} + d_{pp}^2, \quad \text{for } -v_{GS} \leq v_{DG} \leq 0. \tag{16.163}$$

The area of the neck region for the square cells is

$$A_n = nA_{n1} = \frac{nW_1 d_{pp}}{2} + nd_{pp}^2 = \frac{Wd_{pp}}{2} + nd_{pp}^2, \quad \text{for } -v_{GS} \leq v_{DG} \leq 0 \tag{16.164}$$

and the gate-oxide-accumulation region capacitance (or the gate-oxide-neck region capacitance) is given by

$$C_{gd} = C_{ga} = \frac{\epsilon_r A_n}{t_{ox}} = C_{ox} A_n = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}} \left(\frac{Wd_{pp}}{2} + nd_{pp}^2 \right) = C_{gdh}, \quad \text{for } -v_{GS} \leq v_{DG} \leq 0, \tag{16.165}$$

where C_{gdh} denotes a high value of C_{gd}.

In the second region, the voltage range is $0 \leq v_{DG} \leq v_{DS(cr)}$. Here, the MOSFET is OFF, $2x_n < d_{pp}$, v_{GS} is at or near zero, and $v_{DG} = v_{DS} - v_{GS} \approx v_{DS}$. As the voltage $v_{DS} > 0$ increases, the voltage v_{DG} also increases. Figure 16.30 shows the components of the gate-to-drain capacitance C_{gd}, namely C_{ga1}, C_{ga2}, and C_{Dn}. The depletion region of the reverse-biased body diode extends into the neck region, and the effective width of the neck region is reduced to $d_{pp} - 2x_n$. Therefore, the area of the neck region that is not occupied by the depletion region of the body diode is reduced, reducing the capacitance C_{ga1}. The area of the neck region for the square cells is

$$\begin{aligned} A_{n(eff)} &= \frac{2nW_1(d_{pp} - 2x_n)}{4} + n(d_{pp} - 2x_n)^2 = \frac{W(d_{pp} - 2x_n)}{2} + n(d_{pp} - 2x_n)^2 \\ &= \frac{W}{2}\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}} \right) + n\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}} \right)^2, \\ &\qquad \text{for } 0 \leq v_{DS} \leq v_{DS(cr)}. \end{aligned} \tag{16.166}$$

At the critical value of the drain-to-source voltage $v_{DS(cr)}$, the effective neck area A_n is reduced to zero. As the voltage v_{DS} increases from zero to $v_{DS(cr)}$, A_n deceases from its

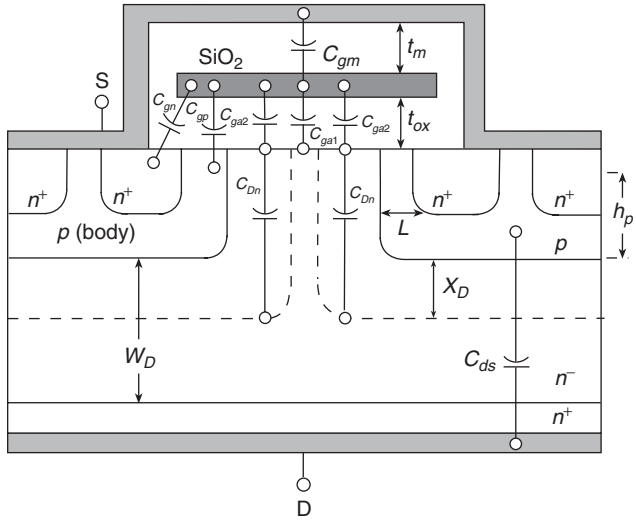


Figure 16.30 Components of gate-to-drain capacitance C_{gd} of power MOSFET for $2x_n < d_{pp}$, when v_{DS} is moderate.

maximum value to zero. The voltage v_{DS} modulates the effective area of the capacitor lower plate. The gate-oxide-neck capacitance is given by

$$C_{ga1} = \frac{\epsilon_{r(ox)}\epsilon_0 A_{n(eff)}}{t_{ox}} = C_{ox}A_{n(eff)} = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}} \times \left[\frac{W}{2}\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right) + n\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right)^2\right], \quad \text{for } 0 \le v_{DS} \le v_{DS(cr)}. \tag{16.167}$$

As the voltage v_{DS} increases from zero to $v_{DS(cr)}$, the capacitance C_{ga1} decreases from its maximum value to zero.

The second component of capacitance C_{gd} for $0 \le v_{DS} \le v_{DS(cr)}$ is formed by the gate polysilicon and the drain semiconductor separated by the SiO_2 and depletion region. It is a capacitance with two dielectric layers: the SiO_2 and the depletion region. This capacitance is equivalent to two capacitances C_{ga2} and C_{Dn} connected in series. The area of the silicon dioxide–depletion layer interface for a single square cell is

$$A_{x1} = W_1 x_n. \tag{16.168}$$

Hence, the area of the silicon dioxide–depletion layer interface for all cells is

$$A_x = nW_1 x_n = Wx_n. \tag{16.169}$$

The gate-oxide-depletion region capacitance is

$$C_{ga2} = \frac{\epsilon_{ox}A_x}{t_{ox}} = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}Wx_n = C_{ox}Wx_n = \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}W\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}, \quad \text{for } 0 \le v_{DS} \le v_{DS(cr)}. \tag{16.170}$$

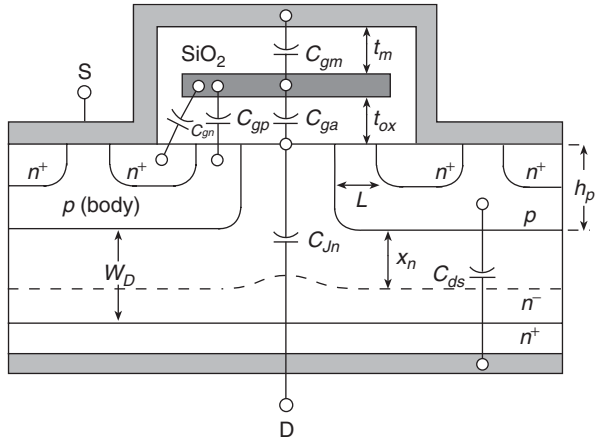


Figure 16.31 Components of gate-to-drain capacitance C_{gd} of power MOSFET for $2x_n = d_{pp}$, when v_{DS} is high.

The capacitance formed by the SiO_2, depletion layer, and the drain in the neck region is

$$C_{Dn} = \frac{\epsilon_{r(Si)}\epsilon_0 W x_n}{h_p + x_n} = \frac{\epsilon_{r(Si)}\epsilon_0 W}{1 + \dfrac{h_p}{x_n}} = \frac{\epsilon_{r(Si)}\epsilon_0 W}{1 + \dfrac{h_p q N_D}{2\epsilon_{r(Si)}\epsilon_0 (V_{bi} + v_{DS})}}$$

$$\approx \epsilon_{r(Si)}\epsilon_0 W x_n, \qquad \text{for } 0 \le v_{DS} \le v_{DS(cr)}. \tag{16.171}$$

The gate-to-drain capacitance for intermediate voltages v_{DS} is

$$C_{gd} = C_{ga1} + \frac{C_{ga2} C_{Dn}}{C_{ga2} + C_{Dn}}, \qquad \text{for } 0 \le v_{DS} \le v_{DS(cr)}. \tag{16.172}$$

In the third region, the voltage range is $v_{DS(cr)} \le v_{DG} \le V_{DSS}$ and the MOSFET is OFF or in the saturation region. When $2x_n \ge d_{pp}$, the entire neck area is occupied by the depletion region of the body diode. Figure 16.31 shows the components of the gate-to-drain capacitance C_{gd} for high voltages v_{DS}. The gate-to-drain capacitance C_{gd} is formed by the gate polysilicon, the drain metal, and the two-layer dielectric that consists of the dioxide and the depletion region below the dioxide–neck interface. The capacitor that contains a two-layer dielectric can be treated as a series combination of two capacitors: C_{gd} and C_{Jn}. The capacitance formed by the depletion region is

$$C_{Jn} = \frac{\epsilon_{r(Si)}\epsilon_0 A_n}{h_p + x_n}$$

$$= \frac{\epsilon_{r(Si)}\epsilon_0}{h_p + \sqrt{\dfrac{2\epsilon_{r(Si)}\epsilon_0 (V_{bi} + v_{DS})}{qN_D}}} \left(\frac{W d_{pp}}{2} + n d_{pp}^2 \right), \quad \text{for } v_{DS(cr)} \le v_{DS} \le V_{DSS}. \tag{16.173}$$

Using (16.165), one obtains the gate-to-source capacitance at high voltages v_{DS},

$$C_{gd} = \frac{C_{ga} C_{Jn}}{C_{ga} + C_{Jn}} \approx C_{gdl}, \qquad \text{for } v_{DS(cr)} \le v_{DS} \le V_{DSS}, \tag{16.174}$$

where C_{gdl} denotes a low value of capacitance C_{gd}. The capacitance C_{gd} is highly nonlinear. The capacitance C_{Jn} is a dominant component in C_{gd}. It can be approximated by $C_{gd} \approx C_{Jn}$. The ratio C_{gdh}/C_{gdl} ranges from 10 to 100. The gate-to-drain capacitance C_{gd} significantly

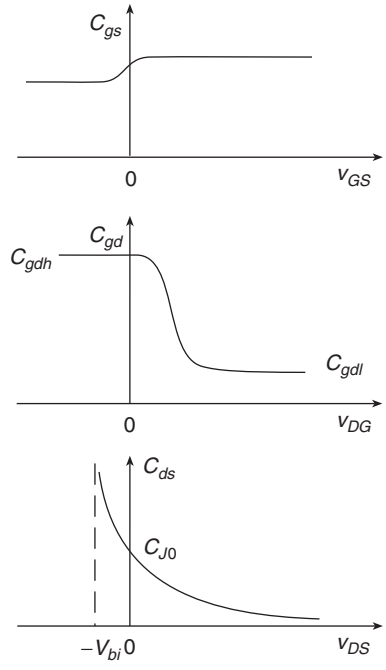


Figure 16.32 Power MOSFET capacitances as functions of transistor voltages.

increases the transistor input capacitance during off-to-on and on-to-off transitions due to *Miller's effect*. Figure 16.32 shows the power MOSFET capacitances as functions of the transistor voltages.

Manufacturers of power MOSFETs usually specify the capacitances $C_{rss} = C_{gd}$, $C_{iss} = C_{gs} + C_{gd}$ and $C_{oss} = C_{gd} + C_{ds}$ measured at $V_{DS} = 25\,\text{V}$, $V_{GS} = 0$, and $f = 1\,\text{MHz}$. Hence,

$$C_{gd} = C_{rss}, \tag{16.175}$$

$$C_{gs} = C_{iss} - C_{rss}, \tag{16.176}$$

and

$$C_{ds} = C_{oss} - C_{rss}. \tag{16.177}$$

Using the drain-to-source capacitance $C_{ds(25)}$ at $V_{DS} = 25\,\text{V}$ given in manufactures' data sheets, we can calculate

$$C_{J0} = C_{ds(25)}\sqrt{\frac{25}{V_{bi}} + 1} \approx 6.7C_{ds(25)} \tag{16.178}$$

and

$$C_{dsmin} = C_{ds(25)}\sqrt{\frac{25 + V_{bi}}{V_{DSmax} + V_{bi}}}. \tag{16.179}$$

Example 16.4

For the power MOSFET designed in Problem 16.3, calculate the capacitances.

Gate-to-source capacitance C_{gs}. Assuming that the gate-to-source overlap length is $L_n = 0.5\,\mu\text{m}$, and the distance between the gate and the metal is $t_m = 0.2\,\mu\text{m}$, the gate polysilicon-to-metal capacitance is given by

$$\begin{aligned} C_{gm} &= \frac{\epsilon_{r(ox)}\epsilon_0 n[d_{pp} + 2(L + L_n)]^2}{t_m} \\ &= \frac{3.9 \times 8.8542 \times 10^{-12} \times 1.25 \times 10^4 \times [10 \times 10^{-6} + 2 \times (0.7 + 0.5) \times 10^{-6}]^2}{0.2 \times 10^{-6}} \\ &= 331.85\,\text{pF}. \end{aligned} \tag{16.180}$$

The gate-to-p-well capacitance is

$$C_{gp} = \frac{\epsilon_{r(ox)}\epsilon_0 LW}{t_{ox}} = \frac{3.9 \times 8.8542 \times 10^{-12} \times 1 \times 0.7 \times 10^{-6}}{0.1 \times 10^{-6}} = 241.719\,\text{pF}. \tag{16.181}$$

The gate-to-n^+ source diffusion overlap capacitance is

$$C_{gn} = \frac{\epsilon_{r(ox)}\epsilon_0 WL_n}{t_{ox}} = \frac{3.9 \times 8.8542 \times 10^{-12} \times 1 \times 0.5 \times 10^{-6}}{0.1 \times 10^{-6}} = 172.65\,\text{pF}. \tag{16.182}$$

The gate-to-source capacitance is

$$C_{gs} = C_{gm} + C_{gp} + C_{gn} = 331.85 + 241.719 + 172.65 = 746.21\,\text{pF}. \tag{16.183}$$

Drain-to-source capacitance C_{ds}. The built-in-potential of the body diode is given by

$$V_{bi} = V_T ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.026\ln\left[\frac{10^{16} \times 10^{15}}{(1.5 \times 10^{10})^2}\right] = 0.6375\,\text{V}. \tag{16.184}$$

The area of all p-wells is given by

$$A_J = n(W_p + 2h_p)^2 = 1.25 \times 10^4 \times [(20 + 2 \times 3) \times 10^{-6}]^2 = 8.45 \times 10^{-6}\,\text{m}^2. \tag{16.185}$$

The zero-bias drain-to-source capacitance is

$$\begin{aligned} C_{J0} &= A_J\sqrt{\frac{q\epsilon_{r(Si)}\epsilon_0 N_D}{2V_{bi}}} = 8.45 \times 10^{-6}\sqrt{\frac{1.602 \times 10^{-19} \times 11.7 \times 8.8542 \times 10^{-12} \times 10^{21}}{2 \times 0.6375}} \\ &= 964\,\text{pF}. \end{aligned} \tag{16.186}$$

Assuming the step junction of the body diode, we obtain the drain-to-source capacitance at $V_{DS} = 1\,\text{V}$ when the MOSFET is ON,

$$C_{ds} = \frac{C_{J0}}{\sqrt{1 + \frac{v_{DS}}{V_{bi}}}} = \frac{964 \times 10^{-12} \times 10^{-9}}{\sqrt{1 + \frac{1}{0.6375}}} = 601.49\,\text{pF}, \tag{16.187}$$

and at $V_{DS} = 80\,\text{V}$ when the MOSFET is OFF,

$$C_{ds} = \frac{C_{J0}}{\sqrt{1 + \frac{v_{DS}}{V_{bi}}}} = \frac{964 \times 10^{-12}}{\sqrt{1 + \frac{80}{0.6375}}} = 85.71\,\text{pF}. \tag{16.188}$$

Thus, $C_{ds(1)}/C_{ds(80)} = 601.49/85.71 = 7.018$. Figure 16.33 shows the plot of the drain-to-source capacitance C_{ds} as a function of the drain-to-source voltage v_{DS}.

Gate-to-drain capacitance C_{gd}. When the MOSFET is ON and the drain-to-source voltage v_{DS} is low, the depletion region of the body diode that extends into the neck region can be

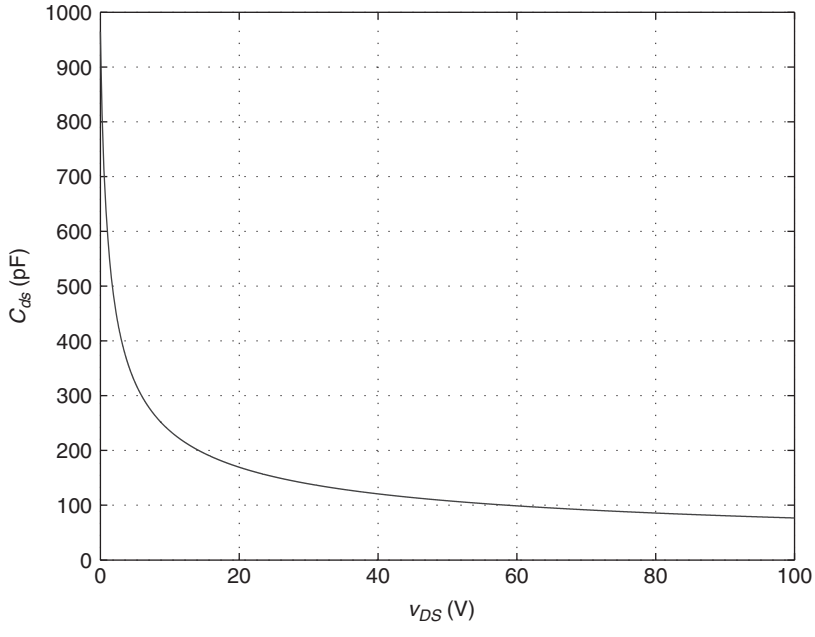


Figure 16.33 Drain-to-source capacitance C_{ds} as a function of the drain-to-source voltage v_{DS}.

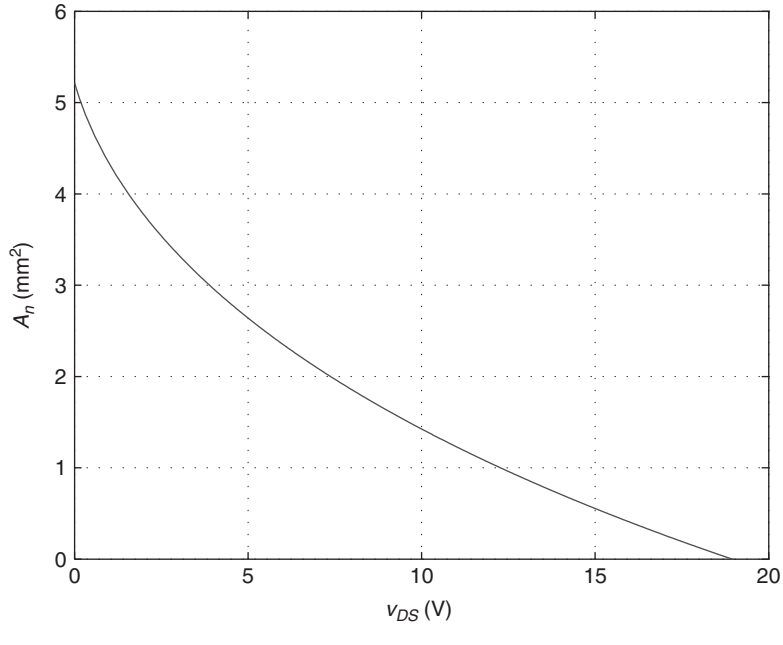


Figure 16.34 Area of the neck A_n as a function of the drain-to-source voltage v_{DS} for $2x_n < d_{pp}$, when v_{DS} is moderate ($0 \leq v_{DS} \leq v_{DS(cr)}$).

neglected. The area of the neck region for square cells is given by

$$A_n = \frac{Wd_{pp}}{2} + nd_{pp}^2 = \frac{1 \times 10 \times 10^{-6}}{2} + 1.25 \times 10^4 \times (10 \times 10^{-6})^2$$
$$= 6.25 \times 10^{-6}\,\text{m}^2. \tag{16.189}$$

The gate-to-accumulation region capacitance (or the gate-to-neck region capacitance) at $v_{DS} = 0$ is given by

$$C_{ga} = C_{gdh} = \frac{\epsilon_{r(ox)}\epsilon_0 A_n}{t_{ox}} = \frac{3.9 \times 8.8542 \times 10^{-12} \times 6.25 \times 10^{-6}}{0.1 \times 10^{-6}} = 2.158\,\text{nF}. \tag{16.190}$$

For $0 \le v_{DS} \le 20\,\text{V}$ when $0 \le 2x_n \le d_{pp}$,

$$C_{Dn} = W\epsilon_{r(Si)}\epsilon_0 = 1 \times 11.7 \times 8.8542 \times 10^{-12} = 103.6\,\text{pF} \tag{16.191}$$

and

$$A_n = \frac{W(d_{pp} - 2x_n)}{2} + n(d_{pp} - 2x_n)^2 = \frac{W}{2}$$
$$\times \left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right) + n\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right)^2. \tag{16.192}$$

Figure 16.34 shows a plot of A_n as a function of v_{DS}. The gate-to-accumulation region capacitance is

$$C_{ga1} = \frac{\epsilon_{r(ox)}\epsilon_0 A_n}{t_{ox}} = C_{ox}A_n$$
$$= \frac{\epsilon_{r(ox)}\epsilon_0}{t_{ox}}\left[\frac{W}{2}\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right)\right.$$
$$\left. + n\left(d_{pp} - 2\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}\right)^2\right]. \tag{16.193}$$

Figure 16.35 shows a plot of C_{ga1} as a function of v_{DS}. As the voltage v_{DS} increases, the area of the lower capacitor plate A_n decreases from the entire neck area to zero, reducing the capacitance C_{ga1}. At the critical voltage $v_{DS(cr)} = 19\,\text{V}$, $2x_n = d_{pp}$, and the entire neck area is occupied by the depletion region.

The capacitance C_{ga2} increases with increasing voltage v_{DS} because the area of the lower capacitor plate increases with v_{DS}. At $v_{DS} = 20\,\text{V}$, the gate-oxide-depletion region capacitance is given by

$$C_{ga2} = \frac{W\epsilon_{r(ox)}\epsilon_0}{t_{ox}}\sqrt{\frac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}} = \frac{1 \times 3.9 \times 8.8542 \times 10^{-12}}{0.1 \times 10^{-6}}$$
$$\times\sqrt{ds\,\frac{2 \times 11.7 \times 8.8542 \times 10^{-12}(0.3878 + 20)}{1.602 \times 10^{-19} \times 10^{21}}} = 1773\,\text{nF}. \tag{16.194}$$

The gate-to-drain capacitance C_{gd} at low values of voltage v_{DS} is given by

$$C_{gd} = C_{ga1} + \frac{C_{ga2}C_{Dn}}{C_{ga2} + C_{Dn}}. \tag{16.195}$$

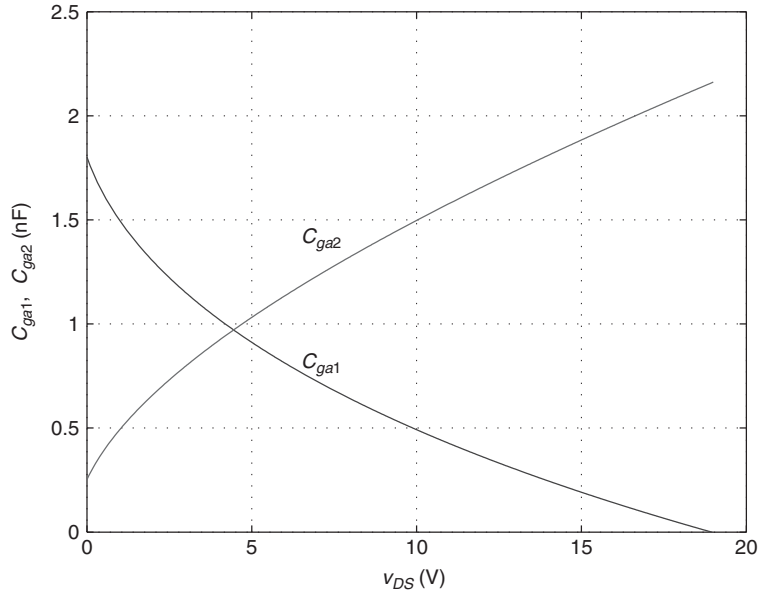


Figure 16.35 Capacitances C_{ga1} and C_{ga2} as functions of the drain-to-source voltage v_{DS} for $2x_n < d_{pp}$, when v_{DS} is moderate ($0 \leq v_{DS} \leq v_{DS(cr)}$).

Figure 16.35 shows a plot of C_{ga2} as a function of v_{DS}. The gate-to-source capacitance at $v_{DS} = 20\,\text{V}$ is

$$C_{gd} = \frac{C_{ga2}C_{Dn}}{C_{ga2} + C_{Dn}} = \frac{1773 \times 103.6}{1773 + 103.6} = 97.88\,\text{pF}. \tag{16.196}$$

Figure 16.36 shows a plot of C_{gd} as a function of v_{DS}. The large capacitance C_{gd} at low values of voltage v_{DS} dominates the MOSFET input capacitance during later stages of turn-on and the first stages of turn-off.

For $v_{DS} = 80\,\text{V}$, $2x_n > d_{pp}$. The capacitance formed by the depletion region is

$$\begin{aligned} C_{Jn} &= \frac{\epsilon_{r(Si)}\epsilon_0}{h_p + \sqrt{\dfrac{2\epsilon_{r(Si)}\epsilon_0(V_{bi} + v_{DS})}{qN_D}}} \left(\frac{Wd_{pp}}{2} + nd_{pp}^2\right) \\ &= \frac{11.7 \times 8.8542 \times 10^{-12}}{3 \times 10^{-6} + \sqrt{\dfrac{2 \times 11.7 \times 8.8542 \times 10^{-12}(0.3878 + 80)}{1.602 \times 10^{-19} \times 10^{15}}}} \times 6.25 \times 10^{-6} \\ &= 49\,\text{pF}. \end{aligned} \tag{16.197}$$

Figure 16.37 shows a plot of C_{Jn} as a function of v_{DS}. The gate-to-drain region capacitance at $V_{DS} = 80\,\text{V}$ is

$$C_{gd} = C_{gdl} = \frac{C_{ga}C_{Jn}}{C_{ga} + C_{Jn}} = \frac{2.398 \times 0.049}{2.398 + 0.049} = 48\,\text{pF}. \tag{16.198}$$

The ratio is $C_{gdh}/C_{gdl} = 2398/48 = 49.96$. Figure 16.38 shows a plot of C_{gd} as a function of v_{DS} for $2x_n = d_{pp}$, when v_{DS} is high. The gate-to-drain capacitance over a wide range of voltages v_{DS} is shown Figure 16.39. Figure 16.40 shows the MOSFET capacitances $C_{iss} = C_{gs} + C_{gd}$, $C_{rss} = C_{gd}$, and $C_{oss} = C_{ds} + C_{gd}$ as functions of v_{DS}. The plots of C_{iss}, C_{ess}, and C_{oss} are similar to the corresponding plots given in manufacturers' data sheets.

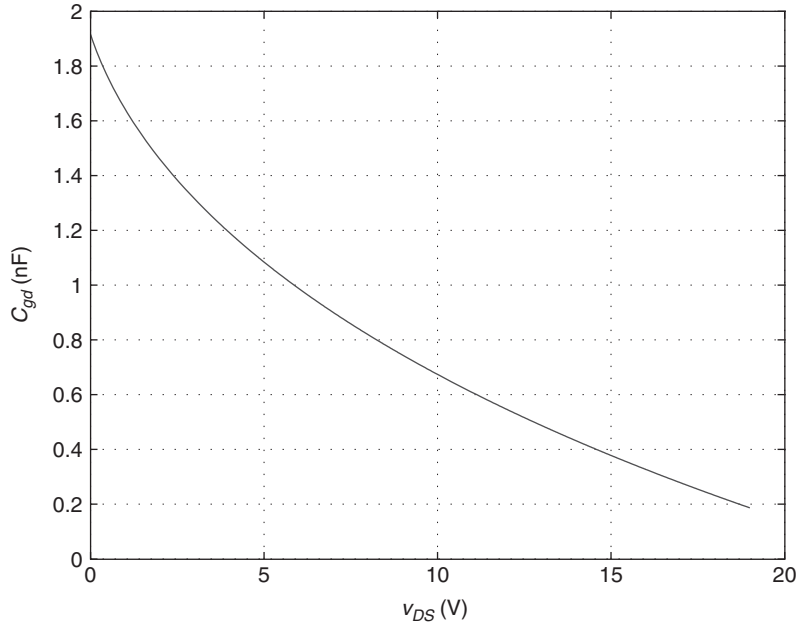


Figure 16.36 Gate-to-drain capacitance C_{gd} as a function of the drain-to-source voltage v_{DS} for $2x_n < d_{pp}$, when v_{DS} is moderate ($0 \leq v_{DS} \leq v_{DS(cr)}$).

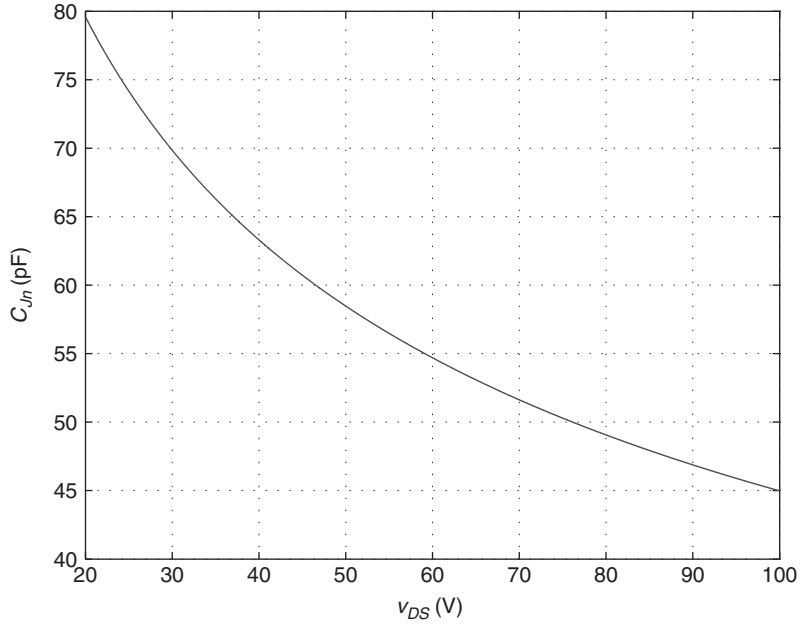


Figure 16.37 Capacitance C_{Jn} as a function of the drain-to-source voltage v_{DS} for $2x_n = d_{pp}$, when v_{DS} is high ($v_{DS(cr)} \leq v_{DS} \leq V_{DSS}$).

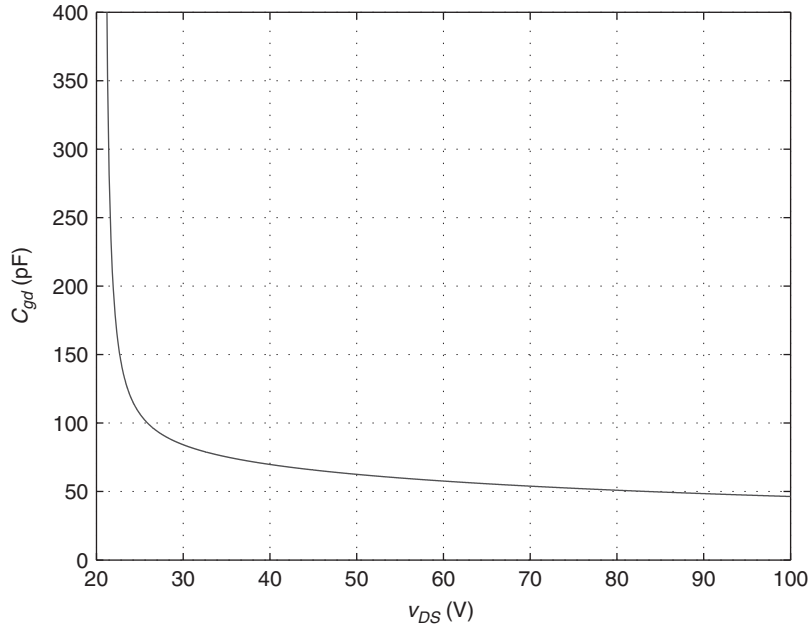


Figure 16.38 Gate-to-source capacitance C_{gd} as a function of the drain-to-source voltage v_{DS} for $2x_n = d_{pp}$, when v_{DS} is high ($v_{DS(cr)} \leq v_{DS} \leq V_{DSS}$).

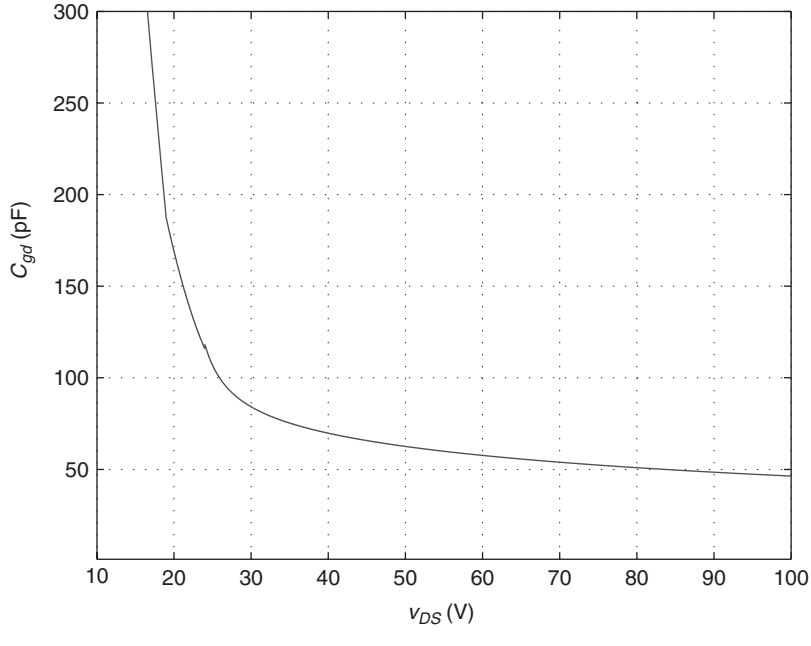


Figure 16.39 Gate-to-source capacitance C_{gd} as a function of the drain-to-source voltage v_{DS}.

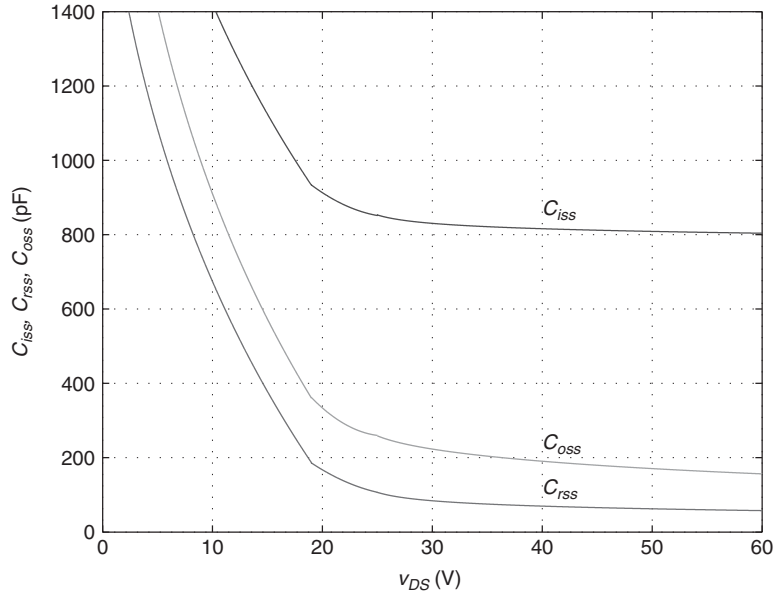


Figure 16.40 Capacitances C_{iss}, C_{rss}, and C_{oss} as functions of the drain-to-source voltage v_{DS}.

16.15 Switching Waveforms

The waveforms during the turn-on and turn-off transitions for the power MOSFET are shown in Figure 16.41. Let us assume that the MOSFET is driven by a square-wave voltage source with its internal resistance. The load is the resistance R_L. During the turn-on

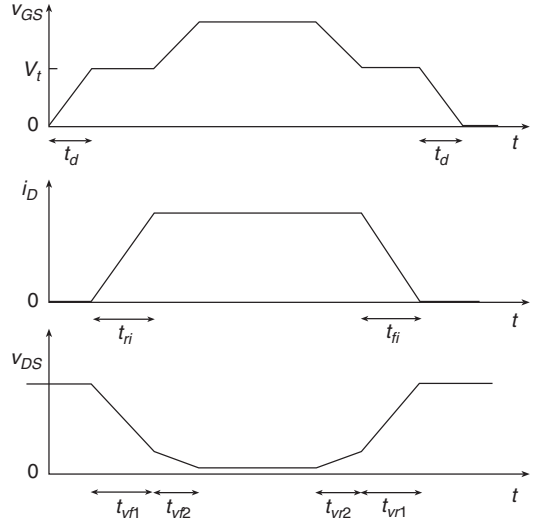


Figure 16.41 MOSFET waveforms during the turn-on and turn-off transitions.

transition, the first time interval is the *delay time* t_d, during which the gate-to-source voltage v_{GS} increases from zero or a negative value to the threshold voltage V_t, charging the capacitances C_{gs} and C_{gd} with the time constant $\tau_G = R_G(C_{gs} + C_{gd})$, where R_G is the MOSFET gate resistance connected in series with the drive source resistance. During the delay time, the MOSFET is in the *cutoff region*, the drain current i_D is zero, the drain-to-source voltage v_{DS} is constant, the voltage gain is zero, and Miller's effect does not exist.

The next time interval is the *drain current rise time* t_{ri}. When v_{GS} exceeds the threshold voltage V_t, the transistor turns on and is in the *saturation region*, the drain current i_D rises, the drain-to-source voltage decreases, the voltage gain $A_v = \Delta v_{DS}/\Delta v_{GS}$ is high, and Miller's effect is very strong. Therefore, Miller's capacitance $C_M = (1 - A_v)C_{gd}$ is reflected to the transistor input and is connected in parallel with capacitance C_{gs}. The total input capacitance $C_i = C_{gs} + (1 - A_v)C_{gd}$ is so large that the gate-to-source voltage v_{GS} increases very slowly.

The last time interval is the drain-to-source voltage fall time $t_{vf} = t_{v1} + t_{v2}$. During the fall time t_{v1}, the gate-to-drain capacitance is low, $C_{gd} = C_{gdl}$, and therefore the rate of change of v_{DS} is high. During the fall time t_{v2}, the gate-to-drain capacitance is high, $C_{gd} = C_{gdh}$, and therefore the rate of change of v_{DS} is low.

After the turn-on transition is completed, the MOSFET remains in the *linear region*. The turn-off transition consists of the drain-to-source voltage rise time t_{vr}, the drain current fall time t_{fi}, and the delay time t_d. Typical switching times are from 40 to 200 ns.

16.16 SPICE Model of Power MOSFETs

Figure 16.42 shows a SPICE large-signal model for n-channel enhancement MOSFETs. It is a model for integrated MOSFETs, which can be adopted to power MOSFETs. SPICE parameters for the level 1 large-signal model of MOSFETs are given in Table 16.1. The diode currents are

$$i_{BD} = IS\left(e^{\frac{v_{BD}}{V_T}} - 1\right) \tag{16.199}$$

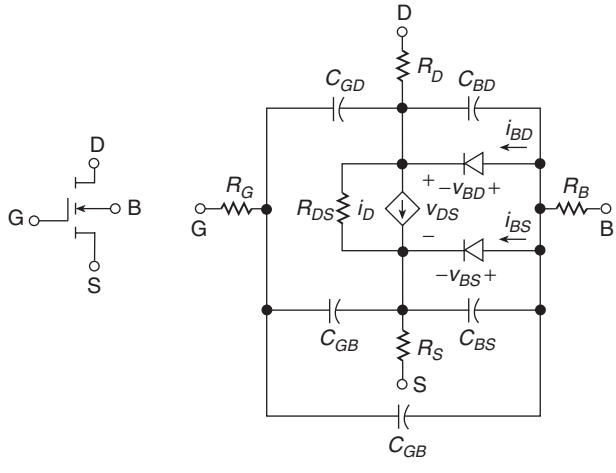


Figure 16.42 SPICE large-signal model for n-channel MOSFET (NMOS). The body B is short-circuited to the source S for power MOSFETs.

Table 16.1 Selected SPICE level 1 NMOS large-signal model parameters

Symbol	SPICE Symbol	Model parameter	Default value	Typical value
V_{to}	VTO	Zero-bias threshold voltage	0 V	0.3 to 3 V
μC_{ox}	KP	Process constant	2×10^{-5} A/V^2	20 to 346 μA/V^2
λ	Lambda	Channel-length modulation	0 V^{-1}	0.5 to 10^{-5} V^{-1}
γ	Gamma	Body-effect V_t parameter	0 V$^{\frac{1}{2}}$	0.35 V$^{\frac{1}{2}}$
$2\phi_F$	PHI	Surface potential	0.6 V	0.7 V
R_D	RD	Drain series resistance	0 Ω	0.2 Ω
R_S	RS	Source series resistance	0 Ω	0.1 Ω
R_G	RG	Gate series resistance	0 Ω	1 Ω
R_B	RB	Body series resistance	0 Ω	1 Ω
R_{DS}	RDS	Drain-to-source shunt R	∞	1 MΩ
R_{SH}	RSH	Drain-to-source diffusion sheet R	0	20 Ω/Sq.
I_S	IS	Saturation current	10^{-14} A	10^{-9} A
M_j	MJ	Grading coefficient	0.5	0.36
C_{j0}	CJ	Zero-bias bulk junction C/m^2	0 F/m^2	1 nF/m^2
V_{bi}	PB	Junction potential	1 V	0.72 V
M_{jsw}	MJSW	Grading coefficient	0.333	0.12
C_{j0sw}	CJSW	Zero-bias junc. perimeter C/m	0 F/m	380 pF/m
V_{BSW}	PBSW	Junction sidewell potential	1 V	0.42 V
C_{GDO}	CGDO	Gate–drain overlap C/m	0 F/m	220 pF/m
C_{GSO}	CGSO	Gate–source overlap C/m	0 F/m	220 pF/m
C_{GBO}	CGBO	Gate–bulk overlap C/m	0 F/m	700 pF/m
F_C	FC	Forward-biased C_J coefficient	0.5	0.5
t_{ox}	TOX	Oxide thickness	∞	4.1 to 100 nm
μ_{ns}	UO	Surface mobility	600 cm^2/Vs	600 cm^2/Vs
n_{sub}	NSUB	Substrate doping	0 cm^{-3}/Vs	0 cm^{-3}/Vs

and

$$i_{BS} = IS\left(e^{\frac{v_{BS}}{V_T}} - 1\right). \tag{16.200}$$

The junction capacitances in the voltage range close to zero are

$$C_{BD} = \frac{(CJ)(AD)}{\left(1 - \dfrac{v_{BD}}{PB}\right)^{MJ}}, \quad \text{for } v_{BD} \leq (FC)(PB), \tag{16.201}$$

and

$$C_{BS} = \frac{(CJ)(AS)}{\left(1 - \dfrac{v_{BS}}{PB}\right)^{MJ}}, \quad \text{for } v_{BS} \leq (FC)(PB), \tag{16.202}$$

where CJ is the zero-bias junction capacitance per unit area, AD is the drain area, AS is the source area, PB is the built-in potential, and MJ is the grading coefficient.

The junction capacitances in the voltage range far from zero are

$$C_{BD} = \frac{(CJ)(AD)}{(1-FC)^{1+MJ}}\left[1-(1+MJ)FC+MJ\frac{v_{BD}}{PB}\right], \quad \text{for } v_{BD} \geq (FC)(PB), \quad (16.203)$$

and

$$C_{BS} = \frac{(CJ)(AS)}{(1-FC)^{1+MJ}}\left[1-(1+MJ)FC+MJ\frac{v_{BD}}{PB}\right], \quad \text{for } v_{BS} \geq (FC)(PB). \quad (16.204)$$

Typical values of some parameter are as follows: $C_{ox} = 3.45 \times 10^{-5}$ pF/μm, $t_{ox} = 4.1 \times 10^{-3}$ μm, $\epsilon_{ox(SiO_2)} = 3.9\epsilon_0$, $C_{j0} = 2 \times 10^{-4}$ F/m^2, $C_{jsw} = 10^{-9}$ F/m, $C_{GBO} = 2 \times 10^{-10}$ F/m, $C_{GDO} = C_{GSO} = 4 \times 10^{-11}$ F/m.

Note that the NMOS syntax takes the form

Mxxxx D G S B MOS-model-name L = xxx W = yyy

for example

M1 2 1 0 0 M1-FET L = 0.18 μm W = 1800 μm

The NMOS model syntax takes the form

.model model-name NMOS (parameter = value . . .)

for example

model M1-FET NMOS (Vto = 1 V Kp = E-4)

The PMOS model syntax takes the form

.model model-name PMOS (parameter = value . . .)

Finally, the subcircuit model syntax takes the form

xname N1 N2 N3 model-name

for example

x1 2 1 0 IRF840

Copy and paste the obtained device model

.SUBCKT IRF840 1 2 3

and the content of the model.

16.17 Insulated Gate Bipolar Transistors

A cross section of the n-channel *insulated gate bipolar transistor* (IGBT) is shown in Figure 16.43. This device is obtained by replacing the n^+ substrate in the vertical double-diffusion power MOSFET by a p^+ substrate. The p^+ substrate, the n^- drift region, and the p-well form a pnp bipolar junction transistor (BJT). Figure 16.44 shows an equivalent circuit of the n-channel IGBT and its circuit symbols. It is a monolithically integrated connection of an n-channel MOSFET and a pnp BJT. The drain of the MOSFET is connected to the base of the BJT, and the source of the MOSFET is connected to the collector of the

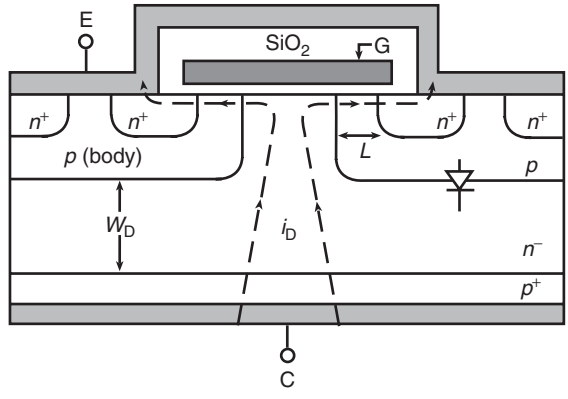


Figure 16.43 Cross section of the n-channel IGBT.

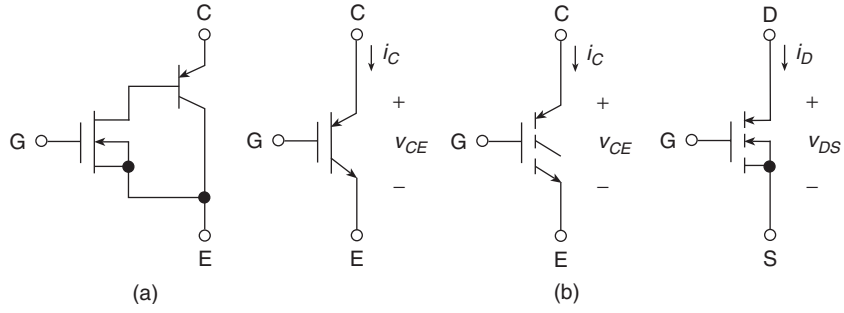


Figure 16.44 IGBT. (a) Equivalent circuit of n-channel IGBT, a composite device that consists of an n-channel MOSFET and a pnp BJT. (b) Symbols.

BJT. This topology is similar to the Darlington connection. The BJT is driven between the base and collector, as in the common-collector (CC) configuration. When the MOSFET is ON, the BJT is ON, and therefore the entire IGBT is ON. When the IGBT is ON, the BJT p^+n^- emitter junction is forward biased and injects hole minority carriers into the n^- drift region, causing conductivity modulation of the drift region. Therefore, the drift region resistance and the on-voltage drop are greatly reduced, lowering the conduction power loss. The injected holes move across the n^- drift region by diffusion and drift. The n^- drift region and the p-well form a collector junction of the BJT, which collects the holes. The on-voltage drop is usually 2 to 3 V. The breakdown voltage is up to 3.5 kV.

The advantages of IGBTs are the simplicity of driving a MOSFET and the low on-state voltage drop of a BJT due to conductivity modulation of the drift region, yielding a significant reduction in the drift region resistance of the MOSFET and the conduction power loss. Reversal of the doping types results in a p-channel MOSFET and an npn BJT. However, the p-channel MOSFET exhibits a higher on-resistance that the n-channel MOSFET. IGBTs combine the high speed and high input impedance of a MOSFET with the high current density and low conduction loss of a BJT. The BJT suffers from the storage time in the base during the turn-off transition. When the MOSFET is turned off, the negative base current cannot be used to remove the excess charge from the base of the BJT. Therefore, the IGBT output current slowly reduces to zero as the excess minority

carrier charge stored in the base gradually decreases by recombination. This effect is called *current tailing*. The switching times are typically 1–4 μs.

IGBTs are good devices for low-frequency, high-voltage, high-power applications, such as electric motor drives. The maximum operating frequency is usually 50 kHz. Electric motors for electric and hybrid cars are examples of applications of IGBTs. Example specifications for a dc–ac three-phase inverter with IGBTs for hybrid cars are: output power $P_O = 30\,\text{kW}$, $V_{DC} = 400\,\text{V}$, and $RPM = 3000$.

16.18 Heat Sinks

Power devices dissipate large amounts of power. The power losses are converted into heat, which increases the device junction temperature T_J. The junction temperature should not exceed the maximum junction temperature T_{Jmax},

$$T_J < T_{Jmax}, \tag{16.205}$$

because the device may suffer permanent damage. For silicon devices, the maximum operating junction temperature T_{Jmax} is usually 150°C to 200°C. For silicon carbide devices, the maximum operating junction temperature T_{Jmax} is usually 250°C to 600°C.

Heat transfer takes place by conduction, convection, and radiation. Conduction allows heat to be removed into a heat sink or chassis. Convection permits the removal of heat by moving air. Radiation allows for heat to be removed by infrared rays.

Let us consider heat conduction. The thermal resistance of a material is given by

$$\theta = \frac{\Delta T}{P} = \rho_T \frac{l}{A}, \tag{16.206}$$

where ΔT is the temperature difference across the material, P is the power flowing through the material, ρ_T is the thermal resistivity, l is the length of the power flow, and A is the cross-sectional area perpendicular to the power flow. The relationship (16.206) is of the same form as Ohm's law. The temperature T corresponds to voltage, power P flow to current I flow, and thermal resistivity ρ_T to electrical resistivity ρ. Convection is also used to transfer heat. The moving hot air is replaced by cold air. The air movement can be natural or forced. Heat spreaders such as fans are used for forced air movement.

Figure 16.45 shows an electrical equivalent circuit for the thermal conduction process in semiconductor devices for steady-state operation and for transients. The heat dissipated in

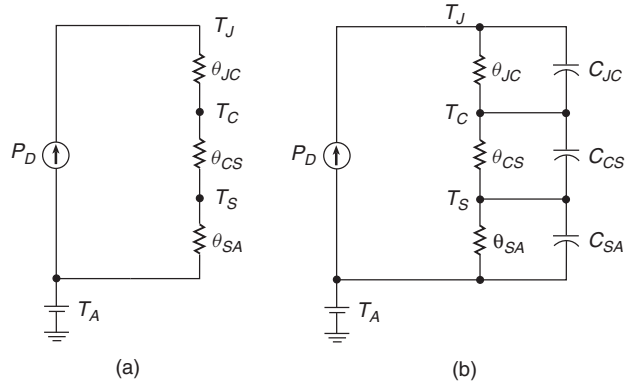


Figure 16.45 Electrical equivalent circuit for heat flow from the device to ambient in semiconductor devices. (a) Steady-state thermal model. (b) Transient thermal model.

a semiconductor device is conducted away from the junction to the case, from the case to the heat sink, and from the heat sink to the surrounding ambient. The junction temperature rise is given by

$$\Delta T_{JA} = T_J - T_A = \theta_{JA} P_D = (\theta_{JC} + \theta_{CS} + \theta_{SA}) P_D, \tag{16.207}$$

where P_D is the power dissipation, θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC} is the junction-to-case thermal resistance, θ_{CS} is the case-to-sink thermal resistance, and θ_{SA} is the sink-to-ambient thermal resistance. The maximum junction temperature is

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}}. \tag{16.208}$$

The typical junction-to-case thermal resistance is $\theta_{JC} = 1^\circ$C/W and the typical case-to-sink thermal resistance is $\theta_{CS} = 0.1^\circ$C/W. The die time constant is $\tau_D = \theta_{JC} C_{JC} = 50–500\,\mu$s and the case time constant is $\tau_C = \theta_{JC} C_{JC} = 1–5$ ms.

Example 16.5

A power MOSFET has $T_{Jmax} = 150^\circ$C and $T_A = 30^\circ$C.

(a) Find the maximum power dissipation P_{Dmax}, and the case temperature T_C, when no heat sink is used, for $\theta_{JC} = 1.5^\circ$C/W and $\theta_{CA} = 50^\circ$C/W.

(b) Find the maximum power dissipation P_{Dmax} when a heat sink is mounted on the transistor at $\theta_{JC} = 1.5^\circ$C/W, $\theta_{CS} = 1^\circ$C/W, and $\theta_{SA} = 5^\circ$C/W.

Solution. (a) The maximum power dissipation is

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JC} + \theta_{CA}} = \frac{150 - 30}{1.5 + 50} = 2.33\,\text{W}. \tag{16.209}$$

(b) The maximum power dissipation is

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{150 - 30}{1.5 + 1 + 5} = 16\,\text{W}. \tag{16.210}$$

When the heat sink is used, the maximum power dissipation increases by a factor of 6.87.

The heat sink temperature is

$$T_S = T_A + \theta_{SA} P_D = 30 + 5 \times 16 = 110^\circ\text{C}. \tag{16.211}$$

The case temperature is

$$T_C = T_A + (\theta_{SA} + \theta_{CS}) P_D = 30 + (5 + 1) \times 16 = 126^\circ\text{C}. \tag{16.212}$$

Manufacturers' data sheets usually give the maximum junction temperature T_{Jmax}, the thermal resistance from the junction to the case θ_{JC}, and the maximum safe power dissipation $P_{D0} = P_{D(rated)}$ of semiconductor devices rated at the case temperature $T_C = T_{A0} = 25^\circ$C, that is, for an ideal cooling of the case with zero thermal resistance between the case and ambient. Under this conditions, the rated power is relatively high and is given by

$$P_{D0} = P_{D(rated)} = \frac{T_{Jmax} - T_{A0}}{\theta_{JC}}. \tag{16.213}$$

In reality, the case temperature T_C is higher than the ambient temperature T_A and therefore the maximum power dissipation $P_{D(max)}$ is lower than the rated power P_{D0} and is

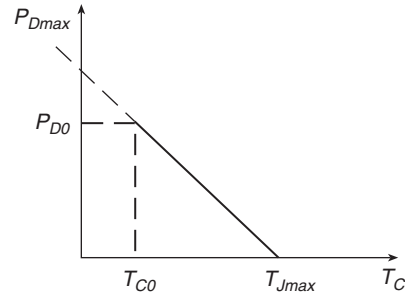


Figure 16.46 The maximum power dissipation P_{Dmax} as a function of the case temperature T_C.

given by

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = -\frac{T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} + \frac{T_{Jmax}}{\theta_{JC} + \theta_{CS} + \theta_{SA}}. \tag{16.214}$$

This equation describes the *power derating curve*, which is illustrated in Figure 16.46. The maximum power dissipation can also be expressed by

$$P_{D(max)} = P_{D0} - \frac{T_C - T_{C0}}{\theta_{JC}} = P_{D0} - DF(T_C - T_{C0}), \tag{16.215}$$

where the derating factor DF is $DF = 1/\theta_{JC}$.

Example 16.6

A power MOSFET is rated to dissipate 30 W at $T_C = T_{A0} = 25^\circ$. Its $T_{Jmax} = 175^\circ$, $\theta_{CS} = 1^\circ$C/W, and $\theta_{SA} = 4^\circ$C/W. Find P_{Dmax}.

Solution. The junction-to-case thermal resistance is

$$\theta_{JC} = \frac{T_{Jmax} - T_{A0}}{P_{D0}} = \frac{175 - 25}{30} = 5^\circ \text{ C/W}. \tag{16.216}$$

The maximum power dissipation is

$$P_{Dmax} = \frac{T_{Jmax} - T_{A0}}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{175 - 25}{5 + 1 + 4} = 15 \text{ W}. \tag{16.217}$$

Thus, the actual maximum safe power dissipation P_{Dmax} is much lower than the rated power P_{D0}.

16.19 Summary

- There are two types of MOSFETs: n-channel and p-channel.
- MOSFETs are unipolar semiconductor devices because the current transport in the channel is due to only one type of carrier, for example, electrons in n-channel MOSFETs, which are majority charge carriers.

- The conducting n-channel is formed in a MOSFET when $v_{GS} > V_t$ is applied and the electron density exceeds the hole density below the gate and the p-type semiconductor is inverted into the n-type inversion layer, connecting drain to source. The application of v_{GS} above V_t causes a build-up of free electrons in the inversion layer in direct proportion to the excess of v_{GS} above V_t.
- The enhancement-mode MOSFET is a normally-off device.
- A MOSFET channel should be wide and short to conduct a large drain current.
- The mobility of electrons decreases as the doping concentration, temperature, and electric field increase.
- When the electric field E is increased, the scattering rate dramatically increases, and the average electron drift velocity saturates, which appears as a decrease in mobility.
- High voltage MOSFETs have a high on-resistance, resulting in a high conduction loss.
- The high breakdown electric field allows SiC power devices to have thinner and more heavily doped voltage blocking layers, reducing the on-resistance.
- The heavily doped blocking layer with concentration increased by a factor of 10 provides 10 times lower resistance of SiC devices than that of Si devices. The 10 times thinner blocking layer of SiC devices reduces the specific on-resistance by a factor of 10. The combination of a tenth of the blocking layer thickness with the 10 times higher doping concentration can yield SiC devices with on-resistance 100 times lower than that of Si devices.
- The mobility of the charge carriers in the channel of a MOSFET is usually less than that found in the bulk of silicon because the charge carriers travel in a very thin layer just below the oxide, the oxide–silicon interface. The charge carrier collisions with interface defects reduce the mobility.
- MOSFETs have three regions of operation: the cutoff region (also called blocking region), linear region (also called ohmic region or triode region), and saturation region (also called pinch-off region).
- The carrier mobility in the channel decreases with increasing transverse electric field perpendicular to the gate oxide.
- For short channel lengths, the carriers travel at the saturation velocity v_{sat}.
- The drain current i_D is related to v_{GS} by the square-law characteristic for low values of v_{GS}. However, the $i_D - v_{GS}$ characteristic becomes linear for higher values of v_{GS} as a result of the high electric field along the channel, causing the drift carrier velocity to saturate.
- The MOSFET on-resistance increases as the breakdown voltage increases because the drift region thickness must be increased and the drift region doping concentration must be decreased.
- A power MOSFET at low drain currents exhibits a positive temperature coefficient, and therefore the transistor can suffer thermal runaway. The temperature coefficient at high currents is negative.
- The gate-to-source capacitance C_{gs} is essentially linear. The gate-to-drain capacitance C_{gd} and the drain-to-source capacitance C_{ds} are highly nonlinear.

- IGBTs are obtained by replacing the n^+ substrate in the power MOSFET with a p^+ substrate.
- IGBTs are easy to drive and have a large gate impedance, like MOSFETs.
- IGBTs have a low on-voltage drop due to conductivity modulation of the drift region, like BJTs.
- The turn-off switching time of IGBTs is long because the excess minority carrier charge cannot be actively removed from the BJT base and it slowly decays due to recombination.

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16.21 Review Questions

16.1 What is the physical structure of a power MOSFETs?

16.2 What the difference between the structure of an integrated MOSFET and a power MOSFET?

16.3 How can the MOSFET maximum drain current be increased?

16.4 How is a large value of the aspect ratio W/L is achieved in power MOSFETs?

16.5 What are the major components of the MOSFET on-resistance?

16.6 How is the MOSFET on-resistance related to the transistor breakdown voltage?

16.7 What is the channel-length modulation on the MOSFET channel resistance?

16.8 What is the short-channel effect on the MOSFET channel resistance?

16.9 Is the gate-to-source capacitance very nonlinear?

16.10 Compare Si and SiC power MOSFETs.

16.11 Compare the on-resistance for low-voltage and high-voltage power MOSFETs.

16.22 Problems

16.1 The drift velocity of silicon electrons at $E = 100\,\text{kV/cm}$ is 10^7 cm/s. Find μ_n.

16.2 Calculate the minimum thickness of the drift region for the power MOSFET with the breakdown voltage $V_{BD} = 50\,\text{V}$, 100 V, 200 V, and 400 V.

16.3 Calculate the maximum doping density of the drift region for the n-channel power MOSFET with the breakdown voltage $V_{BD} = 50\,\text{V}$, 100 V, 200 V, and 400 V.

16.4 The donor concentration in the silicon n-channel power MOSFET is (a) $N_D = 10^{14}\,\text{cm}^{-3}$, (b) $N_D = 10^{15}\,\text{cm}^{-3}$, and (c) $N_D = 10^{16}\,\text{cm}^{-3}$. Find the breakdown voltage.

16.5 The donor concentration in the silicon-carbide n-channel power MOSFET is (a) $N_D = 10^{14}\,\text{cm}^{-3}$, (b) $N_D = 10^{15}\,\text{cm}^{-3}$, and (c) $N_D = 10^{16}\,\text{cm}^{-3}$. Find the breakdown voltage.

16.6 A silicon MOSFET channel has $\mu_n = 600\,\text{cm}^2/\text{Vs}$. Calculate C_{ox} and k_p for: (a) $t_{ox} = 1\,\mu\text{m}$, (b) $t_{ox} = 0.1\,\mu\text{m}$, and (c) $t_{ox} = 0.01\,\mu\text{m}$.

16.7 A power MOSFET has $\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, $W/L = 10^4$, $V_t = 3\,\text{V}$, $\theta = 0.1$, and $V_{GS} = 10\,\text{V}$. Find the drain saturation current at the boundary between the linear and the saturation region I_{Dsat} for a long-channel MOSFET, the long-channel resistance R_c, the short-channel resistance $R_{c(sc)}$, and the ratio $R_{c(sc)}/R_c$.

16.8 A power MOSFET has $L = 1\,\mu\text{m}$, $W/L = 1.6 \times 10^6$, $W_p = 4\,\mu\text{m}$, and $d_{pp} = 2\,\mu\text{m}$. Find the overall channel width W, the number of cells n, the area of all cells A_c, the channel width per unit area D, the cell density CD, and the chip area utilization U. Assume that the source pads, gate pads, and the field guard rings increase the chip area by 25 %.

16.9 Derive an expression for the channel width per unit area D for a power HEXFET and compare it to that of the power MOSFET with square cells.

16.10 Design a SiC n-channel power MOSFET for switching applications to meet the flowing specifications: $V_{DSS} = 1\,\text{kV}$, $I_{SMmax} = 10\,\text{A}$, $r_{DS} \leq 0.2\,\Omega$, $\mu_n = 400\,\text{cm}^2/\text{Vs}$, $V_t = 2\,\text{V}$, and $V_{GSmax} = 10\,\text{V}$.

17

Soft-switching DC–DC Converters

17.1 Introduction

Conventional PWM converters are operated under *hard switching* conditions, where rectangular voltages and currents of semiconductor devices are changed abruptly from high values to zero and vice versa at turn-on and turn-off, causing switching losses and generating a substantial amount of electromagnetic interference. Existing semiconductor power devices and magnetic components do not allow for perfect implementation of PWM converter topologies. Switching losses are due to transistor output capacitance, diode capacitance, diode reverse recovery, and transformer leakage inductance. The energy stored in the transistor output capacitance C_o just before the transistor turns on is given by

$$W_{C_o} = \tfrac{1}{2} C_o V_{off}^2, \tag{17.1}$$

where V_{off} is the transistor off-state voltage. When the transistor turns on, this energy is lost in the transistor, resulting in the transistor switching loss

$$P_{sw(FET)} = \tfrac{1}{2} f_s C_o V_{off}^2. \tag{17.2}$$

Since switching losses are proportional to the switching frequency f_s, they limit the maximum switching frequency. A high level of EMI is due to a wide spectrum of harmonics contained in rectangular PWM waveforms. In addition, high current spikes caused by diode reverse recovery generate a large spectrum of harmonics. In isolated converters, the transformer leakage inductance forms resonant circuits with the transistor and diode output capacitances, causing ringing.

Switching losses and EMI level in dc–dc power converters can be reduced by *soft-switching* techniques [1]–[31] at the expense of increased device stresses and conduction loss. Since semiconductor devices turn on or turn off at zero voltage or zero current, the product of the device voltage and current during the transitions is zero, eliminating switching losses. This allows for high switching frequencies, reducing the size and weight

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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of the soft-switching converters due to lower values of reactive components. The harmonic content of the current and voltage waveforms is also reduced, yielding a lower level of EMI.

The soft-switching techniques can be divided into two categories: *zero-voltage switching* (ZVS) and *zero-current switching* (ZCS).

These were first introduced in the 1970s and early 1980s in Class E ZVS and ZCS amplifiers and oscillators [20]–[23].

In the ZVS technique, the voltage across the transistor is zero when the transistor is turned on. Therefore, the energy stored in the transistor output capacitance is zero at turn-on. Hence, the turn-on switching loss is also zero, yielding high efficiency.

Topologies of soft-switching converters absorb many parasitic components, such as transistor output capacitance, diode capacitance, and transformer leakage inductance. In the ZVS technique, a semiconductor device turns on at zero voltage. In the ZCS technique, a semiconductor device turns off at zero current. For example, the diode turns off at zero current in PWM converters for DCM operation. There are ZVS and ZCS quasi-resonant PWM dc–dc converters. In ZVS quasi-resonant converters, the transistor turns on at zero voltage. In ZCS quasi-resonant converters, the transistor turns off at zero current. The disadvantage of many soft-switching dc–dc converters is variable switching frequency to control the dc output voltage.

17.2 Zero-voltage-switching DC–DC Converters

A family of ZVS quasi-resonant converters is shown in Figure 17.1. These converters are obtained by adding a resonant capacitor C_r in parallel with the switch and a resonant inductor L_r in series with the parallel combination of the switch and the resonant capacitor in the conventional PWM converters. The transistor output capacitance is absorbed into the resonant capacitance C_r. The diode lead inductance is absorbed into the resonant inductance L_r. A power MOSFET contains an antiparallel body diode, which does not allow for a negative switch voltage lower than -0.7 V. Such a switch is unidirectional for the voltage and bidirectional for current. The ZVS quasi-resonant converters with a unidirectional switch for the voltage are called *half-wave ZVS converters*. A diode can be added in series with the transistor to block a negative switch voltage. Such a switch is bidirectional for the voltage and unidirectional for current. Some IGBTs can also be used as bidirectional switches for voltage and unidirectional for current. The ZVS quasi-resonant converters with a bidirectional switch for the voltage are called *full-wave ZVS converters*. A high-frequency equivalent circuit for ZVS converters is shown in Figure 17.2. This circuit is obtained by reducing to zero low-frequency and dc components. The filter inductor L is replaced by an open circuit, the filter capacitor C is replaced by a short circuit, and the input dc source V_I is replaced by a short circuit.

17.3 Buck ZVS Quasi-resonant DC–DC Converter

17.3.1 Waveforms

The circuit, models, and waveforms for the buck ZVS quasi-resonant converter are shown in Figure 17.3. The current through the filter inductance L for CCM is approximately constant. Therefore, the filter inductance L, the filter capacitance C, and the load resistance R_L are modeled as a current sink I_O, as shown in Figure 17.3(b)–(e).

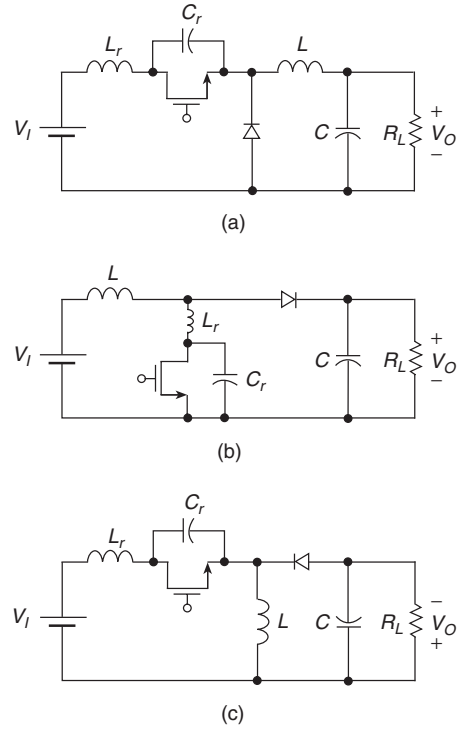


Figure 17.1 Half-wave ZVS quasi-resonant dc–dc converters. (a) Buck converter. (b) Boost converter. (c) Buck-boost converter. In full-wave quasi-resonant ZVS converters, a diode is added in series with the transistor to block a negative switch voltage.

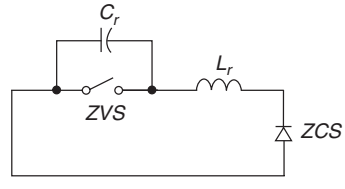


Figure 17.2 High-frequency equivalent circuit of ZVS quasi-resonant dc–dc converters.

The following definitions will be used in the subsequent analysis. The resonant frequency of the L_r–C_r circuit is

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}. \tag{17.3}$$

The normalized switching frequency is

$$A = \frac{f_s}{f_0}. \tag{17.4}$$

The characteristic impedance of the resonant circuit is

$$Z_o = \sqrt{\frac{L_r}{C_r}} = \omega_0 L_r = \frac{1}{\omega C_r}. \tag{17.5}$$

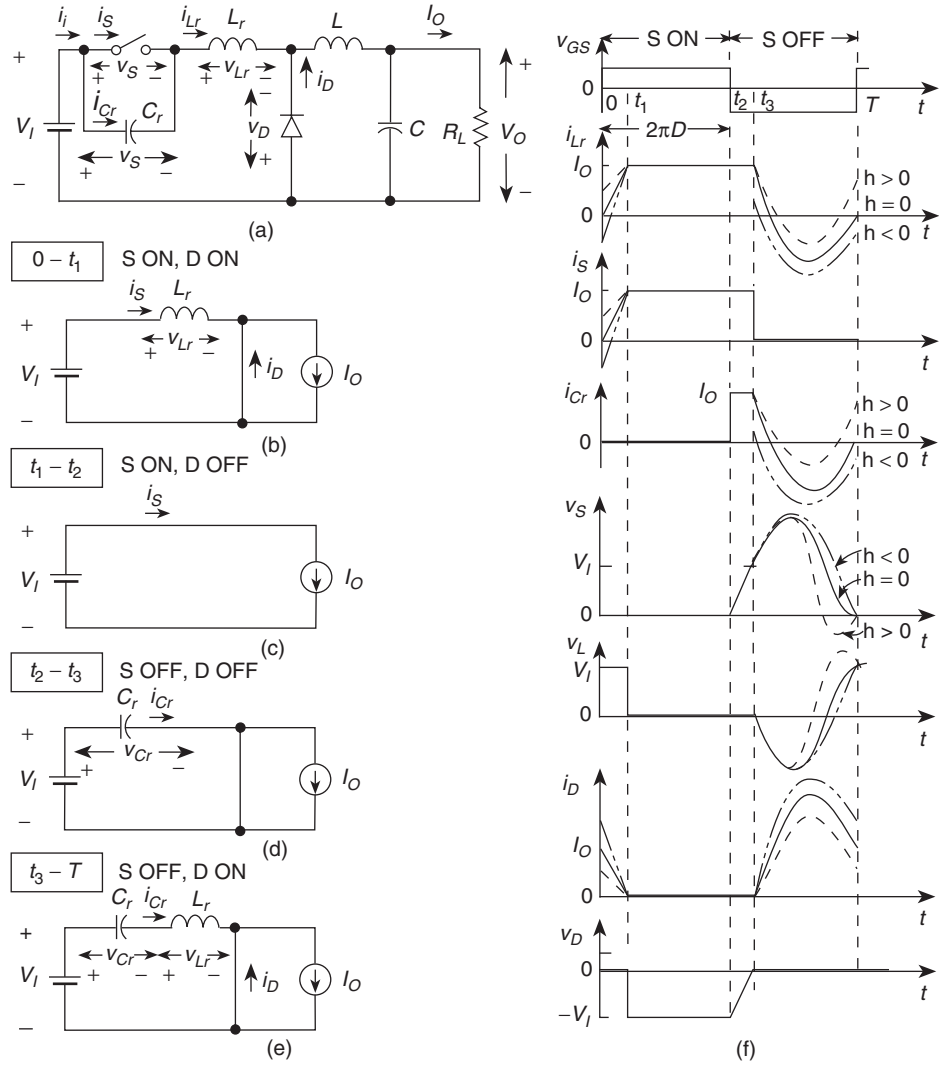


Figure 17.3 Buck ZVS quasi-resonant dc–dc converter. (a) Circuit. (b)–(e) Models for four time intervals. (f) Waveforms.

The normalized load resistance is

$$Q = \frac{R_L}{Z_o} = \frac{R_L}{\sqrt{\dfrac{L_r}{C_r}}} = \frac{R_L}{\omega_0 L_r} = \omega_0 C_r R_L = \frac{A R_L}{\omega_s L_r} = \frac{\omega_s C_r R_L}{A}. \tag{17.6}$$

The dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I}. \tag{17.7}$$

The normalized initial resonant inductor and switch currents when the switch turns on are

$$h = \frac{i_{Lr}(0)}{I_O} = \frac{i_S(0)}{I_O}. \tag{17.8}$$

The operation of the ZVS quasi-resonant converter consists of four time intervals during the switching cycle $T = 1/f_s$.

1. For the resonant inductor charging time interval $0 < t \le t_1$, both the switch and diode are ON. The converter model is shown in Figure 17.3(b). During this time interval, $v_S = 0$, $v_D = 0$, $i_C = 0$, $v_{Lr} = V_I$, and

$$i_{Lr} = \frac{1}{\omega_s L_r}\int_0^{\omega_s t} v_{Lr}\,d(\omega_s t) + i_{Lr}(0) = \frac{1}{\omega_s L_r}\int_0^{\omega_s t} V_I\,d(\omega_s t) + i_{Lr}(0) = \frac{V_I}{\omega_s L_r}\omega_s t + i_S(0). \tag{17.9}$$

Since $V_O = R_L I_O$ and $V_I/(\omega_s L_r) = V_O/(A\omega_o L_r M_{VDC}) = I_O Q/(AM_{VDC})$, we obtain

$$\frac{i_{Lr}(\omega_s t)}{I_O} = \frac{i_S(\omega_s t)}{I_O} = \frac{Q}{AM_{VDC}}\omega_s t + h. \tag{17.10}$$

Because $i_D = I_O - i_S = I_O(1 - i_S/I_O)$,

$$\frac{i_D(\omega_s t)}{I_O} = -\frac{Q}{AM_{VDC}}\omega_s t - h + 1. \tag{17.11}$$

This time interval ends when the diode current reaches zero, that is, when $i_D(\omega_s t_1) = 0$. Hence,

$$\omega_s t_1 = (1 - h)\frac{AM_{VDC}}{Q}. \tag{17.12}$$

2. For the idle time interval $t_1 < t \le t_2$, the switch is ON and the diode is OFF. The converter model is shown in Figure 17.3(c). During this time interval, $v_S = 0$, $i_{Cr} = C_r dv_S/dt = 0$, $i_D = 0$, $i_S = i_{Lr} = I_O$, $v_{Lr} = L_r di_{Lr}/dt = 0$, and $v_D = -V_I$. This time interval ends at $\omega_s t_2 = 2\pi D$, when the transistor is turned off by the gate driver.

3. For the resonant capacitor charging time interval $t_2 < t \le t_3$, both the switch and the diode are OFF. The converter model is shown in Figure 17.3(d). During this time interval, $i_S = 0$, $i_D = 0$, $i_{Lr} = i_{Cr} = I_O$, $v_{Lr} = 0$, and

$$\begin{aligned} v_S = v_{Cr} &= \frac{1}{\omega_s C_r}\int_{2\pi D}^{\omega_s t} v_{Cr}\,d(\omega_s t) + v_{Cr}(2\pi D) = \frac{I_O}{\omega_s C_r}(\omega_s t - 2\pi D) \\ &= \frac{V_O}{\omega_s C_r R_L}(\omega_s t - 2\pi D), \end{aligned} \tag{17.13}$$

where $v_{Cr}(2\pi D) = 0$. Because $V_O/(\omega_r C_r R_L) = M_{VDC}V_I/(AQ)$ and $I_O = V_O/R_L$, we get

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{AQ}(\omega_s t - 2\pi D) \tag{17.14}$$

and

$$\frac{v_D}{V_I} = \frac{M_{VDC}}{AQ}(\omega_s t - 2\pi D) - 1. \tag{17.15}$$

This time interval ends when the diode voltage reaches zero, that is, when $v_D(\omega_s t_3) = 0$. Hence,

$$\omega_s t_3 = 2\pi D + \frac{AQ}{M_{VDC}}. \tag{17.16}$$

4. For the resonant time interval $t_3 < t \le T$, the switch is OFF and the diode is ON. The converter model is shown in Figure 17.3(e). During this time interval, $i_S = 0$ and

$v_D = 0$. The initial conditions are $i_{Lr}(\omega_s t_3) = I_O$ and $v_{Cr}(\omega_s t_3) = v_S(\omega_s t_3) = V_I$. Using the Laplace transform technique,

$$I_{Cr}(s) = I_{Lr}(s) = \frac{L_r I_O e^{-st_3}}{sL_r + \dfrac{1}{sC_r}} = I_O \frac{s}{s^2 + \omega_0^2} e^{-st_3}, \tag{17.17}$$

resulting in

$$\frac{i_{Lr}}{I_O} = \frac{i_{Cr}}{I_O} = \cos \frac{\omega_s t - \omega_s t_3}{A}. \tag{17.18}$$

For steady-state operation, $i_{Lr}(2\pi) = i_{Lr}(0) = hI_O$. Hence,

$$\cos\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right] = h. \tag{17.19}$$

Because $i_D = I_O - i_{Lr} = I_O(1 - i_{Lr}/I_O)$, the diode current waveform is

$$\frac{i_D}{I_O} = 1 - \cos \frac{\omega_s t - \omega_s t_3}{A}. \tag{17.20}$$

Since $\omega_s L_r I_O / A = V_O M_{VDC}/Q$, we have

$$v_{Lr} = \omega_s L_r \frac{di_{Lr}}{d(\omega_s t)} = -\frac{M_{VDC} V_I}{Q} \sin \frac{\omega_s t - \omega_s t_3}{A}. \tag{17.21}$$

The switch voltage waveform is

$$v_S = v_{Cr} = \frac{1}{\omega_s C_r} \int_{\omega_s t_3}^{\omega_s t} i_{Cr} d(\omega_s t) + v_{Cr}(\omega_s t_3) = \frac{V_I M_{VDC}}{Q} \sin \frac{\omega_s t - \omega_s t_3}{A} + V_I, \tag{17.22}$$

yielding

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{Q} \sin \frac{\omega_s t - \omega_s t_3}{A} + 1. \tag{17.23}$$

For ZVS operation, $v_S(2\pi) = v_S(0) = 0$. Hence,

$$\sin\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right] = -\frac{Q}{M_{VDC}}. \tag{17.24}$$

Equations (17.19) and (17.24) along with the trigonometric identity yield

$$\left(\frac{Q}{M_{VDC}}\right)^2 + h^2 = 1, \tag{17.25}$$

which gives

$$\frac{Q}{M_{VDC}} = \sqrt{1 - h^2} \tag{17.26}$$

or

$$h = \pm\sqrt{1 - \left(\frac{Q}{M_{VDC}}\right)^2} = \pm\sqrt{1 - \left(\frac{R_L}{Z_o M_{VDC}}\right)^2}. \tag{17.27}$$

Hence, $-1 \le h \le 1$ and $0 \le Q \le M_{VDC}$, that is, $0 \le R_L \le Z_o M_{VDC}$. Therefore, ZVS operation can be achieved for the load resistance range from 0 to $R_{Lmax} = Z_o M_{VDC} = \omega_0 L_r M_{VDC} = M_{VDC}/(\omega_0 C_r)$. In most applications, the range of R_L is $R_{Lmin} \le R_L < \infty$. Therefore, an impedance inverter should be added to remove the impedance

incompatibility, similar to that used in Class E dc–dc converters [24], [25]. Current and voltage waveforms are shown in Figure 17.3(f). In all three cases, the transistor turns on at zero voltage and the diode turns off at zero current.
From (17.19) and (17.26), we obtain the duty cycle

$$D = \frac{t_2}{T} = 1 - \frac{A}{2\pi}\left[2\pi n + \sqrt{1-h^2} - \arccos\ h\right]$$
$$= 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2n\pi + \frac{Q}{M_{VDC}} - \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]. \quad (17.28)$$

where $n = 1, 2, 3, \ldots$. There are multiple cycle modes of operation for $n \geq 2$. The duty cycle decreases with increasing f_s/f_0 and h. For $h = 0$,

$$D = 1 - \frac{(4n-1)\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right), \quad (17.29)$$

yielding, for $n = 1$,

$$D = 1 - \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right) \approx 1 - 0.9092\left(\frac{f_s}{f_0}\right). \quad (17.30)$$

Three cases can be identified for the voltage and current waveforms:

1. For $h = 0$, both the switch voltage v_S and its derivative dv_S/dt are zero when the switch turns on. Thus, both the ZVS and zero-derivative switching (ZDS) conditions are satisfied. In addition, both the switch voltage v_S and switch current i_S have only positive values.
2. For $-1 \leq h < 0$, when the switch turns on, the switch voltage v_S is zero and the switch voltage derivative dv_S/dt is negative. The switch voltage v_S is always positive, and the switch current has both positive and negative values. Therefore, the switch must be unidirectional for voltage and bidirectional for current. A power MOSFET with its antiparallel body diode form such a switch. Since the switch voltage is only positive, the circuit is called a *half-wave ZVS converter*.
3. For $0 < h \leq 1$, the switch voltage v_S has both positive and negative values, and the switch current is only positive. Therefore, the switch must be bidirectional for voltage and unidirectional for current. A power MOSFET in series with a diode forms such a switch. The series diode will prevent the flow of negative current through the antiparallel body diode. However, the switch on-voltage drop across the MOSFET and the series diode is increased, causing high conduction loss. In addition, the output capacitance of the transistor has no path to discharge. Because the switch voltage v_S has both positive and negative values, the circuit is called a *full-wave ZVS converter*.

17.3.2 DC Voltage Transfer Function

The dc input current is given by

$$I_I = \frac{1}{2\pi}\int_0^{2\pi D} i_S\, d(\omega_s t) = I_O\left[D - \frac{A(1-h)^2}{4\pi\sqrt{1-h^2}}\right]. \quad (17.31)$$

For a lossless converter, $I_O V_O = I_I V_I$. Hence, the dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = D - \frac{A(1-h)^2}{4\pi\sqrt{1-h^2}}$$
$$= 1 - \frac{A}{2\pi}\left[2\pi n + \sqrt{1-h^2} - \arccos\ h + \frac{A(1-h)^2}{2\sqrt{1-h^2}}\right]. \tag{17.32}$$

Hence,

$$M_{VDC} = 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left\{(2n-1)\pi + \frac{Q}{M_{VDC}} + \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right.$$
$$\left. + \frac{M_{VDC}}{2Q}\left[1 + \sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]\right\}, \quad \text{for } h \le 0, \tag{17.33}$$

and

$$M_{VDC} = 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left\{2n\pi + \frac{Q}{M_{VDC}} - \arccos\sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right.$$
$$\left. + \frac{M_{VDC}}{2Q}\left[1 - \sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2}\right]\right\}, \quad \text{for } h \ge 0. \tag{17.34}$$

For $h \ge 0$,

$$M_{VDC} = 1 - \frac{(4n-1)n+2}{4\pi}\left(\frac{f_s}{f_0}\right), \tag{17.35}$$

giving, for $n = 1$,

$$M_{VDC} = D = 1 - \frac{3\pi+2}{4\pi}\left(\frac{f_s}{f_0}\right) = 1 - 0.9092\left(\frac{f_s}{f_0}\right). \tag{17.36}$$

The dc voltage transfer function M_{VDC} is illustrated in Figure 17.4. The maximum frequency f_{1max} is the frequency at which $t_1 = t_2$ (or $\omega_s t_1 = 2\pi D$). Above this frequency, the idle time interval does not exists and the switch current waveform becomes triangular.

17.3.3 Voltage and Current Stresses

The peak switch current I_{SM} and the peak switch voltage V_{SM} are

$$I_{SM} = I_O \tag{17.37}$$

and

$$V_{SM} = \left(\frac{M_{VDC}}{Q} + 1\right)V_I = \left(\frac{1}{Q} + \frac{1}{M_{VDC}}\right)V_O = \left(\frac{Z_o}{R_L} + \frac{1}{M_{VDC}}\right)V_O. \tag{17.38}$$

For $h = 0$, $Q = M_{VDC}$ and

$$V_{SM} = 2V_O. \tag{17.39}$$

The peak switch voltage V_{SM} increases from $2V_I$ as Q decreases from M_{VDC} to zero. The peak diode current I_{DM} and the peak diode voltage V_{DM} are

$$I_{DM} = 2I_O \tag{17.40}$$

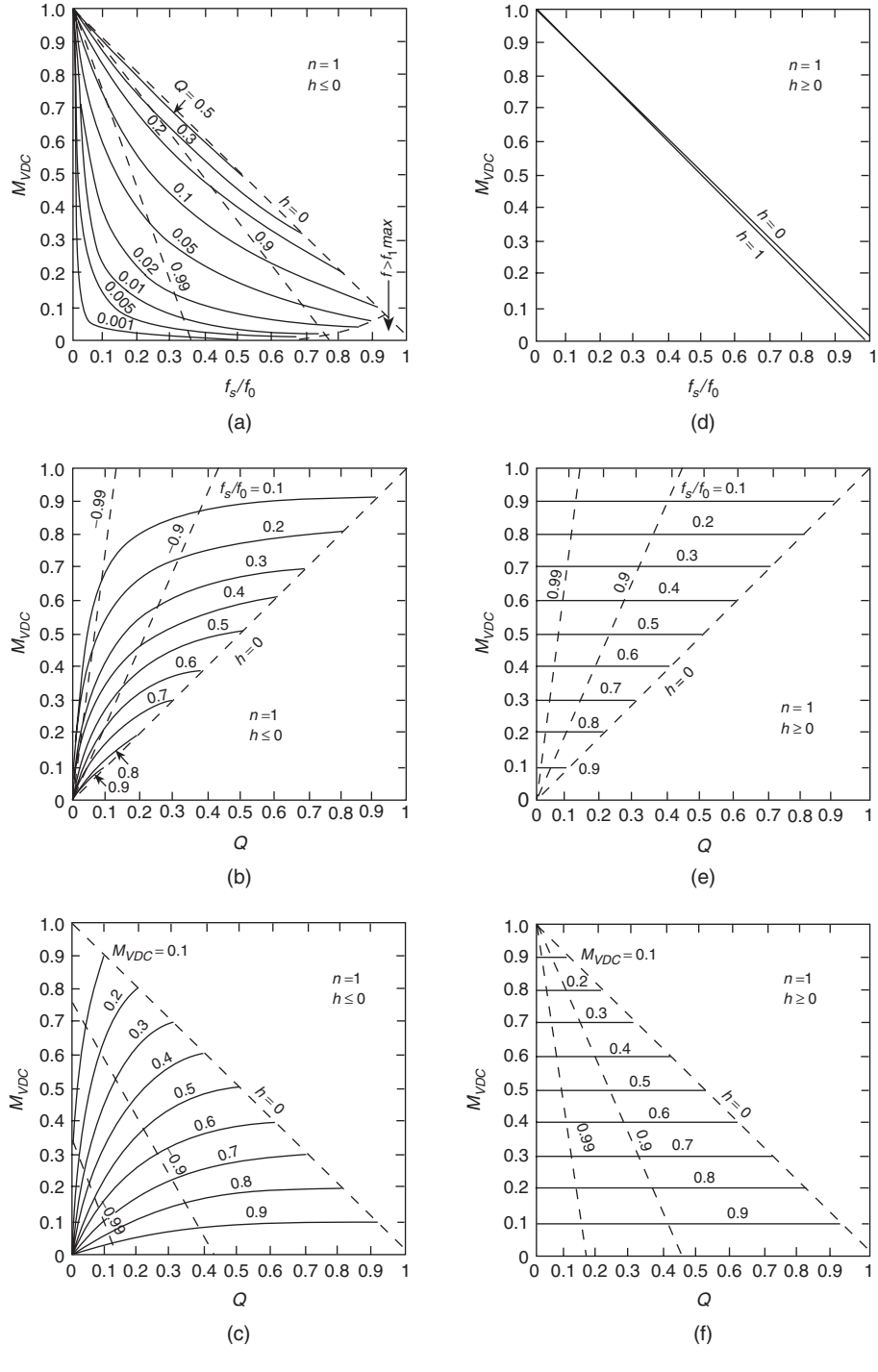


Figure 17.4 DC voltage transfer function for the buck ZVS quasi-resonant converter at $n = 1$. (a)–(c) For half-wave converter ($h \leq 0$). (d)–(f) For full-wave converter ($h \geq 0$).

and

$$V_{DM} = V_I = \frac{V_O}{M_{VDC}}. \tag{17.41}$$

Example 17.1

Design a dc–dc converter to meet the following specifications: $V_I = 20\,\text{V}$, $V_O = 10\,\text{V}$, and $P_O = 10\,\text{W}$.

Solution. We will design a buck ZVS quasi-resonant half-wave converter. The load resistance is

$$R_L = \frac{V_O^2}{P_O} = \frac{10^2}{10} = 10\,\Omega. \tag{17.42}$$

The load current is

$$I_O = \frac{V_O}{R_L} = \frac{10}{10} = 1\,\text{A}. \tag{17.43}$$

The dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{10}{20} = \frac{1}{2}. \tag{17.44}$$

Let us use the buck half-wave ZVS converter with $n = 1$, $Q = M_{VDC} = 0.5$, and $f_s = 1\,\text{MHz}$. In this case, both the ZVS and ZDS conditions are satisfied. The characteristic impedance of the resonant circuit is

$$Z_o = \frac{R_L}{Q} = \frac{10}{0.5} = 20\,\Omega. \tag{17.45}$$

The resonant frequency of the resonant circuit is

$$f_0 = \frac{0.9092 f_s}{1 - M_{VDC}} = \frac{0.9092 \times 10^6}{1 - 0.5} = 1.8184\,\text{MHz}. \tag{17.46}$$

The duty cycle at $h = 0$ is

$$D = 1 - \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right) \approx 1 - 0.9092 \times \left(\frac{f_s}{f_0}\right) = 1 - 0.9092 \times 0.5 = 0.5454. \tag{17.47}$$

The resonant inductance is

$$L_r = \frac{R_L}{\omega_0 Q} = \frac{10}{2\pi \times 1.8184 \times 10^6 \times 0.5} = 1.75\,\mu\text{H}, \tag{17.48}$$

and the resonant capacitance is

$$C_r = \frac{Q}{\omega_0 R_L} = \frac{0.5}{2\pi \times 1.8184 \times 10^6 \times 10} = 4.376\,\text{nF}. \tag{17.49}$$

Pick $L_r = 1.8\,\mu\text{H}$ and $C_r = 3.9\,\text{nF}$.

The peak switch current is

$$I_{SM} = I_O = 1\,\text{A}. \tag{17.50}$$

The peak switch voltage is

$$V_{SM} = \left(\frac{M_{VDC}}{Q} + 1\right) V_I = 2V_I = 2 \times 20 = 40\,\text{V}. \tag{17.51}$$

The peak diode current is

$$I_{DM} = 2I_O = 2 \times 1 = 2\,\text{A}. \tag{17.52}$$

The peak diode voltage is

$$V_{DM} = V_I = 20\,\text{V}. \tag{17.53}$$

17.4 Boost ZVS Quasi-resonant DC–DC Converter

17.4.1 Waveforms

The circuit, models, and waveforms for the boost ZVS quasi-resonant converter are shown in Figure 17.5 The following definitions will be used in the subsequent analysis. The resonant frequency of the L_r–C_r circuit is

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}. \tag{17.54}$$

The normalized switching frequency is

$$A = \frac{f_s}{f_0}. \tag{17.55}$$

The loaded-quality factor is

$$Q = \frac{R_L}{\omega_0 L_r} = \omega_0 C_r R_L = \frac{R_L}{\sqrt{\dfrac{L_r}{C_r}}} = \frac{AR_L}{\omega_s L_r} = \frac{\omega_s C_r R_L}{A}. \tag{17.56}$$

The dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I}. \tag{17.57}$$

The normalized initial resonant inductor and switch current when the switch turns on are

$$h = \frac{i_L(0)}{I_I} = \frac{i_S(0)}{I_I}. \tag{17.58}$$

1. For the resonant inductor charging time interval $0 < t \le t_1$, both the switch and diode are ON. The converter model is shown in Figure 17.5(b). During this time interval, $v_S = 0$, $v_D = 0$, $i_C = 0$, $v_{Lr} = V_O$, and

$$i_{Lr} = \frac{1}{\omega_s L_r}\int_0^{\omega_s t} v_{Lr}\, d(\omega_s t) + i_{Lr}(0) = \frac{V_O \omega_s t}{\omega_s L_r} + i_S(0). \tag{17.59}$$

Since $V_O = R_L I_O$ and $V_O/(\omega_s L_r) = I_I Q/(AM_{VDC})$,

$$\frac{i_{Lr}(\omega_s t)}{I_I} = \frac{i_S(\omega_s t)}{I_I} = \frac{Q}{AM_{VDC}}\omega_s t + h. \tag{17.60}$$

The diode current waveform is given by

$$\frac{i_D(\omega_s t)}{I_I} = -\frac{Q}{AM_{VDC}}\omega_s t - h + 1 \tag{17.61}$$

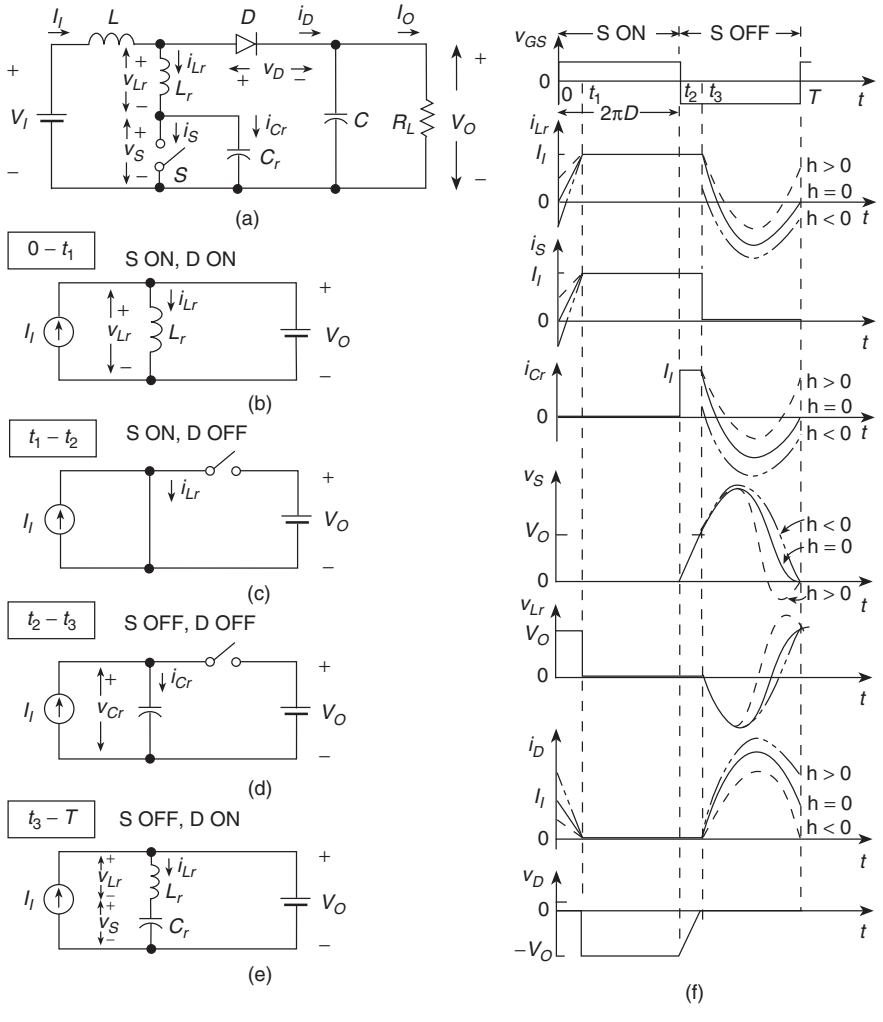


Figure 17.5 Boost ZVS quasi-resonant dc–dc converter. (a) Circuit. (b)–(e) Models for four time intervals. (f) Waveforms.

At the end of this time interval, $i_D(\omega_s t_1) = 0$. Hence,

$$\omega_s t_1 = \frac{AM_{VDC}}{Q}(1 - h). \tag{17.62}$$

2. For the idle time interval $t_1 < t \leq t_2$, the switch is ON and the diode is OFF. The converter model is shown in Figure 17.5(c). During this time interval, $v_S = 0$, $i_{Cr} = 0$, $i_D = 0$, $v_{Lr} = 0$, $i_S = i_{Lr} = I_I$, and $v_D = -V_O$. This time interval ends at $\omega_s t_2 = 2\pi D$, when the transistor is turned off by the gate driver.

3. For the resonant capacitor charging time interval $t_2 < t \leq t_3$, both the switch and the diode are OFF. The converter model is shown in Figure 17.5(d). During this time interval, $i_S = 0$, $i_D = 0$, $i_{Lr} = i_{Cr} = I_I$, $v_{Lr} = 0$, and

$$v_S = \frac{1}{\omega_s C_r}\int_{2\pi D}^{\omega_s t} v_{Cr}\, d(\omega_s t) + v_{Cr}(2\pi D) = \frac{I_I}{\omega_s C_r}(\omega_s t - 2\pi D). \tag{17.63}$$

Because $I_I/(\omega_r C_r) = M_{VDC}V_O/(AQ)$ and $I_O = V_O/R_L$, we get

$$\frac{v_S}{V_O} = \frac{M_{VDC}}{AQ}(\omega_r t - 2\pi D) \tag{17.64}$$

and

$$\frac{v_D}{V_O} = \frac{M_{VDC}}{AQ}(\omega_r t - 2\pi D) - 1. \tag{17.65}$$

The end of this time interval is determined by $v_D(\omega t_3) = 0$. Hence,

$$\omega_s t_3 = 2\pi D + \frac{AQ}{M_{VDC}}. \tag{17.66}$$

4. For the time interval $t_3 < t \leq T$, the switch is OFF and the diode is ON. The converter model is shown in 17.5(e). During this time interval, $i_S = 0$ and $v_D = 0$. The initial conditions are $i_L(\omega_s t_3) = I_I$ and $v_S(\omega_s t_3) = V_I$. Using the Laplace transform technique,

$$i_{Lr}(s) = \frac{s}{s^2 + \omega_0^2} I_I e^{-st_3}, \tag{17.67}$$

resulting in

$$\frac{i_{Lr}}{I_I} = \frac{i_{Cr}}{I_I} = \cos\frac{\omega_s t - \omega_s t_3}{A}. \tag{17.68}$$

The diode current waveform is

$$\frac{i_D}{I_I} = 1 - \cos\frac{\omega_s t - \omega_s t_3}{A}. \tag{17.69}$$

Since $I_O = V_O/R_L$ and $\omega_s L_r I_I/A = V_O M_{VDC}/Q$, we have

$$v_L = \omega_s L\frac{di_L}{d(\omega_s t)} = -\frac{M_{VDC}V_O}{Q}\sin\frac{\omega_s t - \omega_s t_3}{A}. \tag{17.70}$$

The switch voltage waveform is

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{Q}\sin\frac{\omega_s t - \omega_s t_3}{A} + 1. \tag{17.71}$$

For ZVS operation, $v_S(2\pi) = v_S(0) = 0$. Also, $i_{Lr}(2\pi) = i_{Lr}(0) = I_O$. Hence, the relationships among M_{VDC}, Q, and h are given by a set of equations:

$$h = \cos\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right] \tag{17.72}$$

and

$$\frac{Q}{M_{VDC}} = -\sin\left[\frac{2\pi(1-D)}{A} - \frac{Q}{M_{VDC}}\right]. \tag{17.73}$$

This set of equations and the trigonometric identity yield

$$\left(\frac{Q}{M_{VDC}}\right)^2 + h^2 = 1, \tag{17.74}$$

which gives

$$\frac{Q}{M_{VDC}} = \sqrt{1 - h^2} \tag{17.75}$$

or

$$h = \pm\sqrt{1 - \left(\frac{Q}{M_{VDC}}\right)^2}. \tag{17.76}$$

The duty cycle is given by

$$D = 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n - \arccos\ h + \sqrt{1-h^2}\right]$$
$$= 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n - \arccos\ \sqrt{1-\left(\frac{Q}{M_{VDC}}\right)^2} + \frac{Q}{M_{VDC}}\right]. \quad (17.77)$$

For $h = 0$,

$$D = 1 - \frac{(4n-1)\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right). \quad (17.78)$$

For $n = 1$,

$$D = 1 - \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right) = 1 - 0.9092\left(\frac{f_s}{f_0}\right). \quad (17.79)$$

17.4.2 DC Voltage Transfer Function

$$I_O = \frac{1}{2\pi}\int_0^{2\pi} i_D d(\omega_s t) = I_I\left[1 - D + \frac{(1-h^2)}{4\pi\sqrt{1-h^2)}}\right]. \quad (17.80)$$

Assuming that the converter is lossless, $I_O V_O = I_I V_I$. Hence, the dc voltage transfer function is given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1 - D + \dfrac{A(1-h^2)}{4\pi\sqrt{1-h^2}}}$$
$$= \frac{2\pi}{A\left[2\pi n - \arccos\ h + \sqrt{1-h^2} + \dfrac{(1-h)^2}{2\sqrt{1-h^2}}\right]}. \quad (17.81)$$

Thus,

$$M_{VDC} = \frac{2\pi}{\left(\dfrac{f_s}{f_0}\right)\left\{\begin{array}{c}(2n-1)\pi + \dfrac{Q}{M_{VDC}} + \arccos\sqrt{1-\left(\dfrac{Q}{M_{VDC}}\right)^2} \\ + \dfrac{M_{VDC}}{2Q}\left[1 + \sqrt{1-\left(\dfrac{Q}{M_{VDC}}\right)^2}\right]\end{array}\right\}}, \quad \text{for } h \le 0, \quad (17.82)$$

and

$$M_{VDC} = \frac{2\pi}{\left(\dfrac{f_s}{f_0}\right)\left\{\begin{array}{c}2n\pi + \dfrac{Q}{M_{VDC}} - \arccos\sqrt{1-\left(\dfrac{Q}{M_{VDC}}\right)^2} \\ + \dfrac{M_{VDC}}{2Q}\left[1 - \sqrt{1-\left(\dfrac{Q}{M_{VDC}}\right)^2}\right]\end{array}\right\}} \quad \text{for } h \ge 0. \quad (17.83)$$

For $h = 0$,

$$M_{VDC} = \frac{1}{1-D} = \frac{4\pi}{[(4n-1)\pi + 2)]\left(\frac{f_s}{f_0}\right)}, \tag{17.84}$$

which for $n = 1$ becomes

$$M_{VDC} = \frac{1}{1-D} = \frac{4\pi}{(3\pi+2)\left(\frac{f_s}{f_0}\right)} = \frac{1.1}{\left(\frac{f_s}{f_0}\right)}. \tag{17.85}$$

The dc voltage transfer function M_{VDC} is illustrated in Figure 17.6.

17.4.3 Current and Voltage Stresses

The switch peak current and voltage are

$$I_{SM} = I_I = M_{VDC} I_O \tag{17.86}$$

and

$$V_{SM} = \left(\frac{M_{VDC}}{Q} + 1\right) V_O. \tag{17.87}$$

The diode peak current and voltage are

$$I_{DM} = 2I_I = 2M_{VDC} I_O \tag{17.88}$$

and

$$V_{DM} = V_O. \tag{17.89}$$

Example 17.2

Design a dc–dc converter to meet the following specifications: $V_I = 156\,\text{V}$, $V_O = 400\,\text{V}$, and $I_O = 1\,\text{A}$.

Solution. We shall design a boost ZVS quasi-resonant half-wave converter. The load resistance is

$$R_L = \frac{V_O}{I_O} = \frac{400}{1} = 400\,\Omega. \tag{17.90}$$

The dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{400}{156} = 2.564. \tag{17.91}$$

Let us use the boost half-wave ZVS converter with $n = 1$, $Q = M_{VDC} = 2.564$, and $f_s = 1\,\text{MHz}$. In this case, both the ZVS and ZDS conditions are satisfied. Since

$$M_{VDC} = \frac{1.1}{f_s/f_0} = 2.564 \tag{17.92}$$

we obtain the resonant frequency

$$f_0 = \frac{M_{VDC} f_s}{1.1} = \frac{2.564 \times 1}{1.1} = 2.33\,\text{MHz}. \tag{17.93}$$

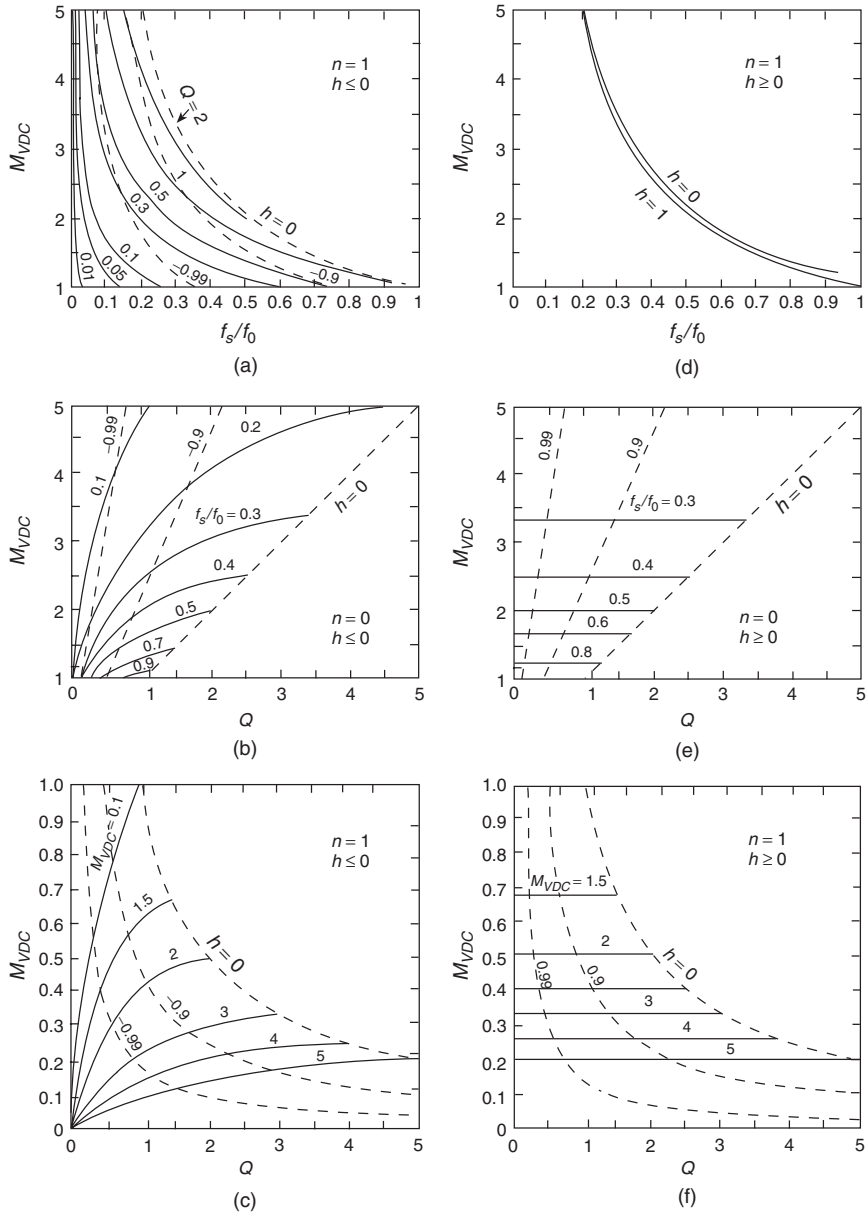


Figure 17.6 DC voltage transfer function for the boost ZVS quasi-resonant converter at $n = 1$. (a)–(c) For half-wave converter ($h \leq 0$). (d)–(f) For full-wave converter ($h \geq 0$).

The characteristic impedance of the resonant circuit is

$$Z_o = \frac{R_L}{Q} = \frac{400}{2.564} = 156\,\Omega. \tag{17.94}$$

The duty cycle at $h = 0$ is

$$D = 1 - \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right) \approx 1 - 0.9092\left(\frac{f_s}{f_0}\right) = 1 - 0.9092 \times 0.429 = 0.61. \tag{17.95}$$

The resonant inductance is

$$L_r = \frac{R_L}{\omega_0 Q} = \frac{400}{2\pi \times 2.33 \times 10^6 \times 2.564} = 10.656\,\mu\text{H} \tag{17.96}$$

and the resonant capacitance is

$$C_r = \frac{Q}{\omega_0 R_L} = \frac{2.564}{2\pi \times 2.33 \times 10^6 \times 400} = 437.8\,\text{pF}. \tag{17.97}$$

Pick $L_r = 10\,\mu\text{H}$ and $C_r = 470\,\text{pF}$.

The peak switch current is

$$I_{SM} = M_{VDC} I_O = 2.564 \times 1 = 2.654\,\text{A}. \tag{17.98}$$

The peak switch voltage is

$$V_{SM} = \left(\frac{M_{VDC}}{Q} + 1\right) V_I = 2V_O = 2 \times 400 = 800\,\text{V}. \tag{17.99}$$

The peak diode current is

$$I_{DM} = 2M_{VDC} I_O = 2 \times 2.564 \times 1 = 5.128\,\text{A}. \tag{17.100}$$

The peak diode voltage is

$$V_{DM} = V_O = 400\,\text{V}. \tag{17.101}$$

17.4.4 Generalization

It can be observed from the analysis of the ZVS quasi-resonant buck and boost converters that the expressions for the dc voltage transfer function are similar to those of PWM converters. The dc transfer function for the buck ZVS quasi-resonant converter is

$$M_{VDC} = D - \gamma_v, \tag{17.102}$$

for the boost ZVS quasi-resonant converter is

$$M_{VDC} = \frac{1}{1 - (D - \gamma_v)}, \tag{17.103}$$

and for the buck-boost ZVS quasi-resonant converter is

$$M_{VDC} = \frac{D - \gamma_v}{1 - (D - \gamma_v)}, \tag{17.104}$$

where

$$\gamma_v = \frac{(1-h)^2}{4\pi\sqrt{1-h^2}}\left(\frac{f_s}{f_0}\right) = \frac{M_{VDC}}{2Q}\left[1 \pm \sqrt{1 - \left(\frac{Q}{M_{VDC}}\right)^2}\right]\left(\frac{f_s}{f_0}\right). \tag{17.105}$$

17.5 Zero-current-switching DC–DC Converters

A family of zero-current-switching quasi-resonant converters is shown in Figure 17.7. These circuits are obtained by adding a resonant inductor L_r in series with the transistor and a resonant capacitor C_r in parallel with the series combination of the transistor and the resonant

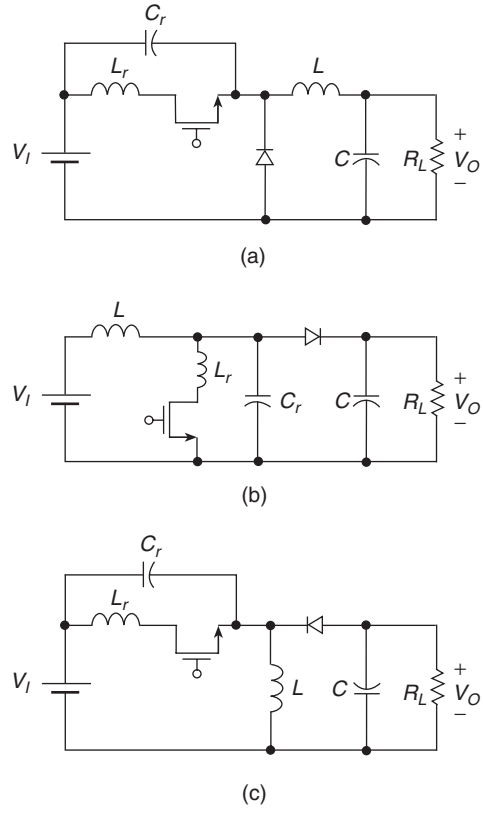


Figure 17.7 Full-wave ZCS quasi-resonant dc–dc converters. (a) Buck converter. (b) Boost converter. (c) Buck-boost converter.

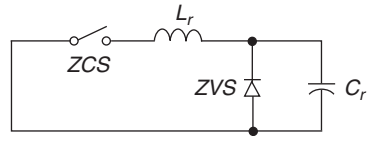


Figure 17.8 High-frequency equivalent circuit of ZCS quasi-resonant dc–dc converters.

inductor L_r. When a power MOSFET with its body diode is used, it acts as a bidirectional switch for the current and unidirectional switch for the voltage. In this case, the circuits are *full-wave ZCS converters*. When a diode is connected in series with the MOSFET, the switch is unidirectional for current and bidirectional for voltage. Circuits with such a switch are called *half-wave ZCS converters*. A high-frequency model is depicted in Figure 17.8. One terminal of the resonant capacitor C_r must be connected to the source of the MOSFET and the other terminal should be connected to the ac ground. Therefore, C_r can also be connected in parallel with the diode or with the filter inductor L. Furthermore, C_r can be split into three capacitors connected as described above [8]. The diode capacitance and the parasitic capacitance of the filter inductor L are absorbed into the resonant capacitance C_r.

17.6 Boost ZCS Quasi-resonant DC–DC Converter

17.6.1 Waveforms

The circuits models and waveforms for the boost ZCS quasi-resonant converter are shown in Figure 17.9. The normalized initial voltage across the resonant capacitor C_r and the switch is

$$h = \frac{v_{Cr}(0)}{V_O} = \frac{v_S(0)}{V_O}. \tag{17.106}$$

The on-switch duty cycle is

$$D = 1 - \frac{t_2}{T}. \tag{17.107}$$

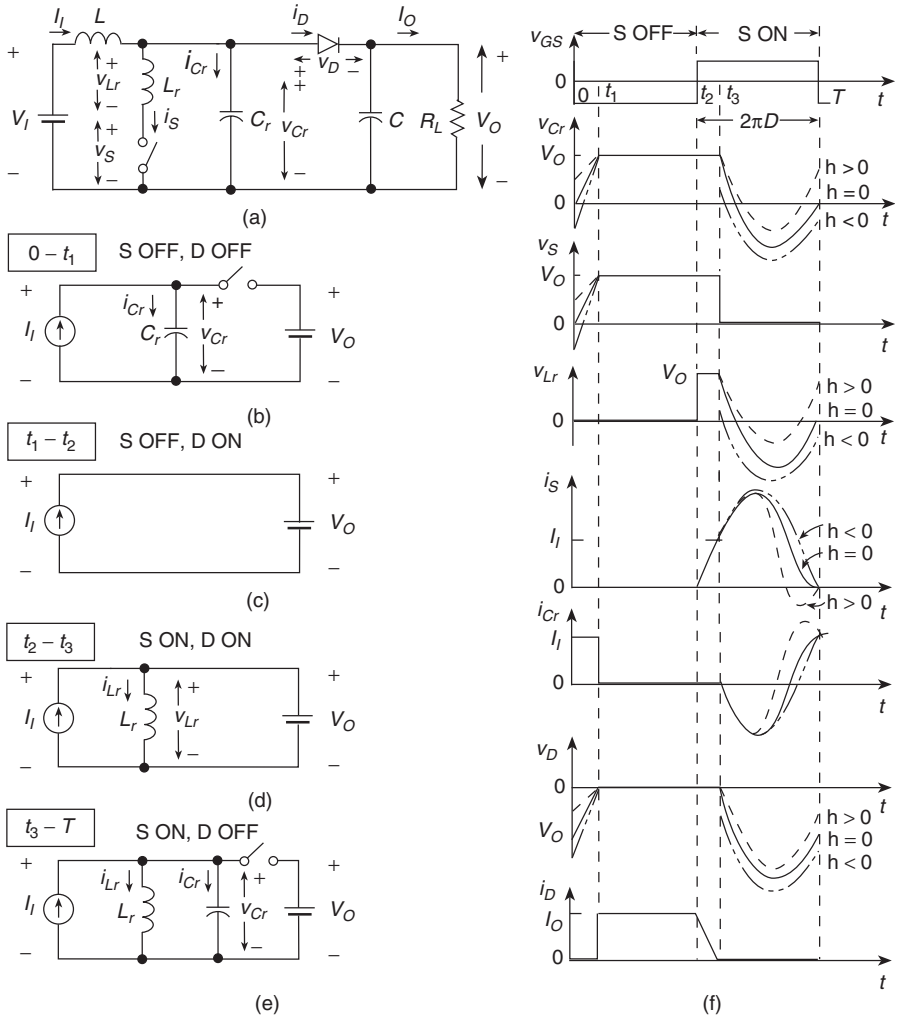


Figure 17.9 Boost ZCS quasi-resonant dc–dc converters. (a) Circuit. (b)–(e) Models. (f) Waveforms.

1. For the resonant capacitor charging time interval $0 < t \leq t_1$, both the switch and the diode are OFF. The converter model is depicted in Figure 17.9(b). During this time interval, $i_S = 0$, $i_D = 0$, $v_{Lr} = 0$, and $i_{Cr} = I_I$. The voltage across the resonant capacitor and the switch is

$$v_{Cr} = v_S = \frac{1}{\omega_s C_r} \int_0^{\omega_s t} i_{Cr} d(\omega_r t) + v_{Cr}(0) = \frac{I_I}{\omega_s C_r} \omega_s t + v_{Cr}(0), \tag{17.108}$$

where

$$\frac{I_I}{\omega_r C_r} = \frac{M_{VDC} I_O}{A \omega_o C_r} = \frac{M_{VDC} V_O}{A \omega_0 C_r R_L} = \frac{M_{VDC} V_O}{AQ}. \tag{17.109}$$

Thus,

$$\frac{v_{Cr}}{V_O} = \frac{v_S}{V_O} = \frac{M_{VDC}}{AQ} \omega_s t + h. \tag{17.110}$$

Since $v_D = v_{Cr} - V_O = V_O(v_{Cr} - 1)$,

$$\frac{v_D}{V_O} = \frac{M_{VDC}}{AQ} \omega_s t + h - 1. \tag{17.111}$$

This time interval ends when $v_D(\omega_s t_1) = 0$. Hence,

$$\omega_s t_1 = \frac{AQ(1-h)}{M_{VDC}}. \tag{17.112}$$

2. For the idle time interval $t_1 < t \leq t_2$, the switch is OFF and the diode is ON. The converter model is depicted in Figure 17.9(c). During this time interval, $i_S = 0$, $v_D = 0$, $v_{Lr} = 0$, $v_{Cr} = v_S = V_O$, $i_{Cr} = 0$, and $i_D = I_I$. This time interval ends at $\omega_s t_2 = 2\pi(1 - D)$ when the transistor is turned off by the gate driver.

3. For the resonant inductor charging time interval $t_2 < t \leq t_3$, both the switch and the diode are ON. The converter model is depicted in Figure 17.9(d). During this time interval, $v_S = 0$, $v_D = 0$, $v_{Lr} = v_{Cr} = V_O$, and $i_{Cr} = 0$. The voltage across the resonant capacitor and the switch current is

$$i_S = i_{Lr} = \frac{1}{\omega_s L_r} \int_{2\pi(1-D)}^{\omega_s t} v_{Cr} d(\omega_s t) = \frac{V_O}{\omega_s L_r} [\omega_s t - 2\pi(1 - D)], \tag{17.113}$$

where

$$\frac{V_O}{\omega_s L_r} = \frac{V_O}{A \omega_0 L_r} = \frac{Q I_O}{A} = \frac{Q I_I}{A M_{VDC}}. \tag{17.114}$$

Thus,

$$\frac{i_S}{I_I} = \frac{Q}{A M_{VDC}} [\omega_s t - 2\pi(1 - D)]. \tag{17.115}$$

Because $i_D = I_I - i_S = I_I(1 - i_S/I_I)$,

$$\frac{i_D}{I_I} = 1 - \frac{Q}{A M_{VDC}} [\omega_s t - 2\pi(1 - D)]. \tag{17.116}$$

This time interval ends when $i_D(\omega_s t_3) = 0$. Hence,

$$\omega_s t_3 = 2\pi(1 - D) + \frac{A M_{VDC}}{Q}. \tag{17.117}$$

4. For the resonant time interval $t_3 < t \le T$, both the switch and the diode are OFF. The converter model is depicted in Figure 17.9(e). During this time interval, $v_S = 0$ and $i_D = 0$, $v_{Lr} = 0$. The initial conditions are $i_{Lr}(\omega_s t_3) = i_S(\omega_s t_3) = I_I$ and $v_{Cr}(\omega_s t_3) = V_O$. Using the Laplace transform method, we have

$$I_{Cr}(s) = -\frac{V_O}{L(s^2 + \omega_0^2)} e^{-st_3}, \tag{17.118}$$

yielding

$$\frac{i_{Cr}}{I_I} = -\frac{Q}{M_{VDC}} \sin \frac{\omega_s t - \omega_s t_3}{A}. \tag{17.119}$$

Since $i_S = I_I - i_{Cr}$,

$$\frac{i_S}{I_I} = \frac{Q}{M_{VDC}} \sin \frac{\omega_s t - \omega_s t_3}{A} + 1. \tag{17.120}$$

Imposing the ZCS condition that $i_S(2\pi) = i_S(0) = 0$, we get

$$\sin \frac{2\pi - \omega_s t_3}{A} = -\frac{M_{VDC}}{Q}. \tag{17.121}$$

The voltage across the parallel resonant circuit is

$$v_{Cr} = v_{Lr} = \omega_s L_r \frac{di_S}{d(\omega_s t)} = V_O \cos \frac{\omega_s t - \omega_s t_3}{A}. \tag{17.122}$$

To achieve ZCS operation, the condition $v_{Cr}(2\pi) = v_{Cr}(0) = hV_O$ must be satisfied, resulting in

$$\cos \frac{2\pi - \omega_s t_3}{A} = h. \tag{17.123}$$

The on-duty cycle is given by

$$\begin{aligned} D = \frac{t_2}{T} &= \frac{A}{2\pi}\left[2\pi n - \arccos\ h + \sqrt{1 - h^2}\right] \\ &= \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n + \frac{M_{VDC}}{Q} - \arccos \sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2}\right]. \end{aligned} \tag{17.124}$$

For $h = 0$,

$$D = \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_0}\right) \approx 0.9092\left(\frac{f_s}{f_0}\right) \tag{17.125}$$

Applying the trigonometric identity to (17.121) and (17.123), we obtain

$$h^2 + \left(\frac{M_{VDC}}{Q}\right)^2 = 1, \tag{17.126}$$

from which

$$\frac{M_{VDC}}{Q} = \sqrt{1 - h^2} \tag{17.127}$$

or

$$h = \pm\sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2} = \pm\sqrt{1 - \left(\frac{Z_o M_{VDC}}{R_L}\right)^2}. \tag{17.128}$$

Hence, $-1 \le h \le 1$ and $Q \ge M_{VDC}$, that is, $R_L \ge R_{Lmin} = Z_o M_{VDC} = \omega_o L_r M_{VDC} = M_{VDC}/(\omega_o C_r)$. This range of the load resistance is an important advantage of ZCS converters because the load resistance for most power supplies is in the range $R_{Lmin} \le R_L < \infty$.

In addition, ZCS converters can be designed so that the maximum output power occurs at $h = 0$, that is, at $Q = M_{VDC}$. In this case, both i_S and di_S/dt are zero when the switch turns off. Because $v_D = v_{Lr} - V_O$,

$$\frac{v_D}{V_O} = \cos\frac{\omega_s t - \omega_s t_3}{A} - 1. \tag{17.129}$$

Voltage and current waveforms are depicted in Figure 17.9(f) for ZCS operation.

1. For $h = 0$, both the switch current i_S and its derivative di_S/dt are zero when the transistor turns off.
2. For $-1 \le h < 0$, the derivative of the switch current di_S/dt when the transistor turns off is negative, and the switch current i_S is always positive. The circuit is called a *half-wave ZCS converter*.
3. For $0 < h \le 1$, the derivative of the switch current di_S/dt when the transistor turns off is positive, and the switch current i_S has positive and negative values. The circuit is called a *full-wave ZCS converter*.

17.6.2 Voltage Transfer Function

The dc output current is

$$I_O = \frac{1}{2\pi}\int_{\omega_s t_1}^{\omega_s t_3} i_D\, d(\omega_s t) = I_I\left[1 - D - \frac{A(1-h)^2}{4\pi\sqrt{1-h^2}}\right]. \tag{17.130}$$

For a lossless converter, $V_O I_O = I_I V_I$. Thus, the dc voltage transfer function is

$$\begin{aligned} M_{VDC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} &= \frac{1}{1 - D - \dfrac{A(1-h)^2}{4\pi\sqrt{1-h^2}}} \\ &= \frac{1}{1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\left[2\pi n - \arccos\ h + \sqrt{1-h^2} + \dfrac{(1-h)^2}{2\sqrt{1-h^2}}\right]}. \end{aligned} \tag{17.131}$$

Thus,

$$\begin{aligned} M_{VDC} = \Bigg\{1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\Bigg\{(2n-1)\pi + \frac{M_{VDC}}{Q} + \arccos\sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2} \\ + \frac{M_{VDC}}{2Q}\left[1 + \sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2}\right]\Bigg\}\Bigg\}^{-1}, \quad \text{for } h \le 0 \end{aligned} \tag{17.132}$$

and

$$\begin{aligned} M_{VDC} = \Bigg\{1 - \frac{1}{2\pi}\left(\frac{f_s}{f_0}\right)\Bigg\{(2n\pi + \frac{M_{VDC}}{Q} - \arccos\sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2} \\ + \frac{M_{VDC}}{2Q}\left[1 - \sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2}\right]\Bigg\}\Bigg\}^{-1}, \quad \text{for } h \ge 0. \end{aligned} \tag{17.133}$$

For $h = 0$,

$$M_{VDC} = \frac{1}{1 - \dfrac{(4n-1)\pi + 2}{4\pi}\left(\dfrac{f_s}{f_0}\right)}, \tag{17.134}$$

yielding, for $n = 1$,

$$M_{VDC} = \frac{1}{1 - \dfrac{3\pi + 2)}{4\pi}\left(\dfrac{f_s}{f_0}\right)} = \frac{1}{1 - 0.9092\left(\dfrac{f_s}{f_0}\right)}. \tag{17.135}$$

The dc voltage transfer function M_{VDC} is illustrated in Figure 17.10.

17.6.3 Current and Voltage Stresses

The peak switch current and voltage are given by

$$I_{SM} = (Q + M_{VDC})I_O = \left(\frac{1}{Z_o} + \frac{M_{VDC}}{R_L}\right)V_O \tag{17.136}$$

and

$$V_{SM} = V_O. \tag{17.137}$$

The switch peak current I_{SM} decreases as R_L increases from R_{Lmin}. The peak diode current and voltage are given by

$$I_{SM} = I_I = M_{VDC}I_O \tag{17.138}$$

and

$$V_{DM} = 2V_O. \tag{17.139}$$

Example 17.3

Design a dc–dc converter to meet the following specifications: $V_I = 10\,\text{V}$, $V_O = 20\,\text{V}$, and $P_O = 40\,\text{W}$.

Solution. A boost ZCS quasi-resonant full-wave converter will be designed. The load resistance is

$$R_L = \frac{V_O^2}{P_O} = \frac{20^2}{40} = 10\,\Omega. \tag{17.140}$$

The load current is

$$I_O = \frac{V_O}{R_L} = \frac{20}{10} = 2\,\text{A}. \tag{17.141}$$

The dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{20}{10} = 2. \tag{17.142}$$

Let us use the half-wave ZVS buck converter with $Q = M_{VDC} = 2$, $n = 1$, and $f_s = 1\,\text{MHz}$. The characteristic impedance of the resonant circuit is

$$Z_o = \frac{R_L}{Q} = \frac{10}{2} = 5\,\Omega. \tag{17.143}$$

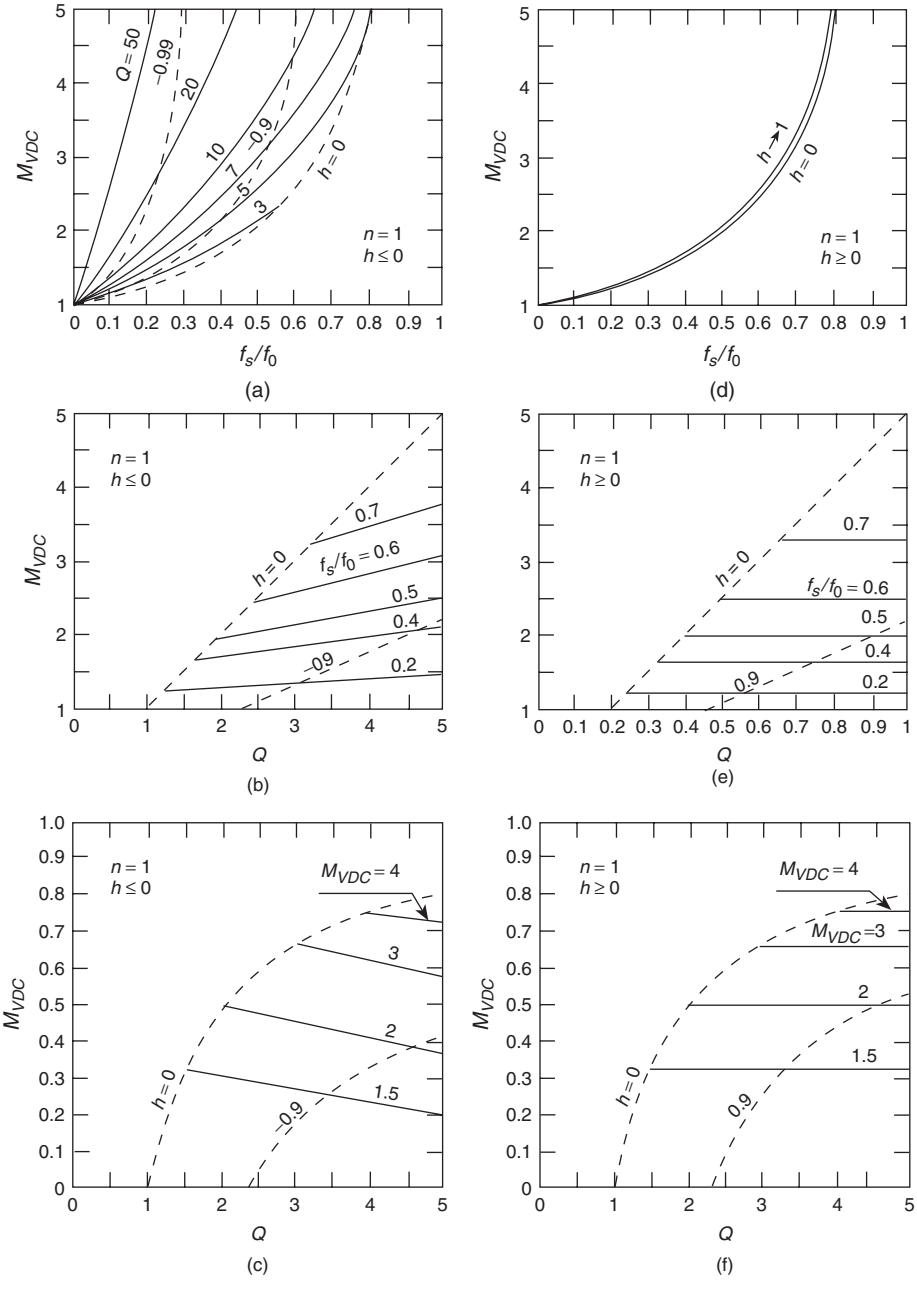


Figure 17.10 DC voltage transfer function for the boost ZCS quasi-resonant converter at $n = 1$. (a)–(c) For half-wave converter ($h \leq 0$). (d)–(f) For full-wave converter ($h \geq 0$).

Assume $Q = M_{VDC} = 2$ and $f_s = 1\,\text{MHz}$. In this case, both the ZCS and ZDS conditions are are satisfied when the transistor turns on. The switching frequency is

$$f_0 = \frac{0.9092 f_s}{1 - \dfrac{1}{M_{VDC}}} = \frac{0.9092 \times 10^6}{1 - \dfrac{1}{2}} = 1.8184\,\text{MHz}. \tag{17.144}$$

The duty cycle is

$$D = 0.9092 \times \left(\frac{f_s}{f_0}\right) = 0.9092 \times \frac{1}{1.8184} = 0.5. \tag{17.145}$$

The resonant inductance is

$$L_r = \frac{R_L}{\omega_0 Q} = \frac{10}{2\pi \times 1.81814 \times 10^6 \times 2} = 0.4376\,\mu\text{H}, \tag{17.146}$$

and the resonant capacitance is

$$C_r = \frac{Q}{\omega_0 R_L} = \frac{2}{2\pi \times 1.8184 \times 10^6 \times 10} = 17.5\,\text{nF}. \tag{17.147}$$

Pick $L_r = 0.39\,\mu\text{H}$ and $C_r = 18\,\mu\text{F}$.

The peak switch current is

$$I_{SM} = (Q + M_{VDC})I_O = (2 + 2) \times 2 = 8\,\text{A}. \tag{17.148}$$

The peak switch voltage is

$$V_{SM} = V_O = 20\,\text{V}. \tag{17.149}$$

The peak diode current is

$$I_{DM} = I_I = M_{VDC}I_O = 2 \times 2 = 4\,\text{A}. \tag{17.150}$$

The peak diode voltage is

$$V_{DM} = 2V_O = 2 \times 20 = 40\,\text{V}. \tag{17.151}$$

17.6.4 Generalization

The dc transfer function for the buck ZCS quasi-resonant converter is

$$M_{VDC} = D - \gamma_i, \tag{17.152}$$

for the boost ZCS quasi-resonant converter is

$$M_{VDC} = \frac{1}{1 - (D - \gamma_i)}, \tag{17.153}$$

and for the buck-boost ZCS quasi-resonant converter is

$$M_{VDC} = \frac{D - \gamma_i}{1 - (D - \gamma_i)}, \tag{17.154}$$

where

$$\gamma_v = \frac{(1-h)^2}{4\pi\sqrt{1-h^2}}\left(\frac{f_s}{f_0}\right) = \frac{M_{VDC}}{2Q}\left[1 \pm \sqrt{1 - \left(\frac{M_{VDC}}{Q}\right)^2}\right]\left(\frac{f_s}{f_0}\right). \tag{17.155}$$

17.7 Multiresonant Converters

A family of multi-resonant ZVS dc–dc converters is shown in Figure 17.11. It is obtained by adding a resonant capacitor C_{rd} in parallel with the diode to the ZVS quasi-resonant

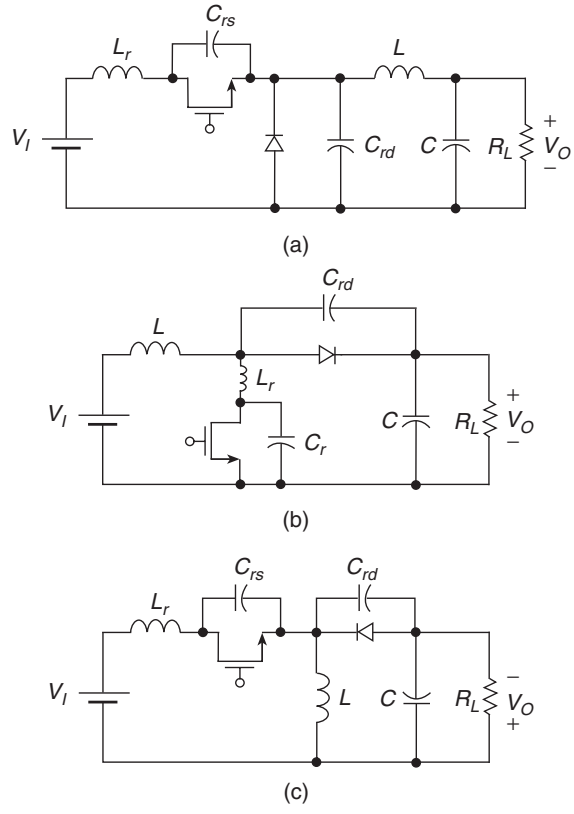


Figure 17.11 Multiresonant ZVS dc–dc converters. (a) Buck converter. (b) Boost converter. (c) Buck-boost converter.

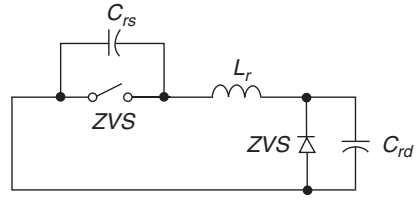


Figure 17.12 High-frequency equivalent circuit of ZVS multiresonant dc–dc converters.

converter. As a result, both the transistor and the diode turn on at zero voltage. A high-frequency equivalent circuit of the ZVS multi-resonant converters is shown in Figure 17.12.

A family of multi-resonant ZCS converters is shown in Figure 17.13. In these converters, a resonant inductor L_{rd} is connected in series with the switch and a resonant inductor L_{sd} is connected in series with the diode. A resonant capacitor C_r is connected in parallel with the series combination of the diode and L_{rd} or with the series combination of the switch and the inductor L_{rs}. In the ZCS multiresonant converters, both switch and the diode turn off at zero current. A high-frequency equivalent circuit of the multi-resonant ZCS converters is depicted in Figure 17.14.

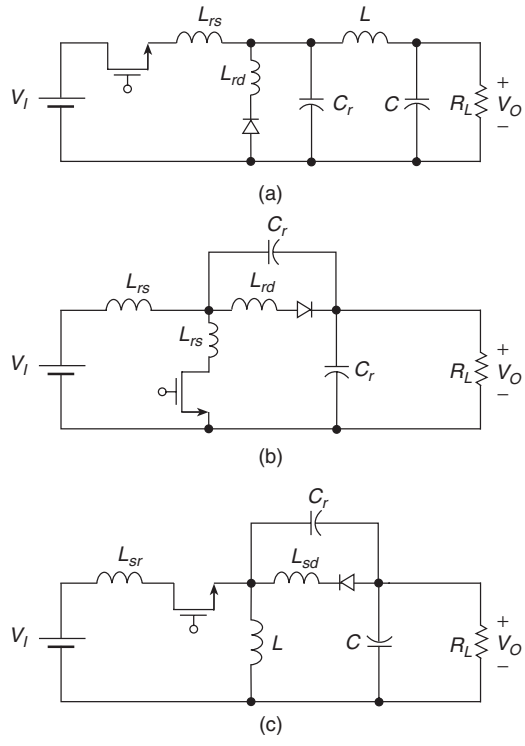


Figure 17.13 Multiresonant ZCS dc–dc converters. (a) Buck converter. (b) Boost converter. (c) Buck-boost converter.

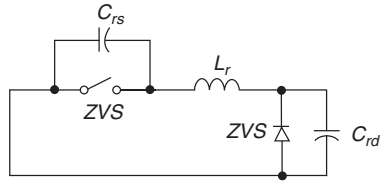


Figure 17.14 High-frequency equivalent circuit of ZCS multiresonant dc–dc converters.

There are also zero-voltage transition, zero-current transition dc–dc PWM converters [26], and active-clamping ZVS PWM converters [27]. Resonant dc–dc power converters operate under ZVS or ZCS conditions [25].

17.8 Summary

- In the ZVS quasi-resonant converters, the transistor turns on at zero voltage, and the diode turns on at zero current.
- Quasi-resonant converter topologies absorb many parasitic components into the resonant circuit.

- In the ZVS quasi-resonant converters, the transistor output capacitance is absorbed into the resonant capacitance and the lead diode inductance is absorbed into the resonant inductance.
- In isolated ZVS quasi-resonant converters, the transformer leakage inductance is absorbed into the resonant inductance.
- In ZVS quasi-resonant converters, the peak transistor current is identical to that of PWM converters. However, the peak transistor voltage is much higher than that of PWM converters, leading to a higher MOSFET on-resistance and higher conduction loss.
- In the ZCS quasi-resonant converters, the transistor turns off at zero current, and the diode turns on at zero voltage.
- In the ZCS quasi-resonant converters, the diode capacitance is absorbed into the resonant capacitance.
- In the ZCS quasi-resonant converters, the transistor peak current is much higher than that of PWM converters, causing higher conduction loss.
- In the multiresonant converters, both the transistor and the diode turn on at zero voltage.

17.9 References

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17.10 Review Questions

17.1 What is the ZVS technique?

17.2 Which parasitic components are included in the topology of ZVS quasi-resonant converters?

17.3 What is the ZCS technique?

17.4 Which parasitic components are included in the topology of ZCS quasi-resonant converters?

17.5 What is the multiresonant ZVS technique?

17.6 Which parasitic components are included in the topology of multiresonant ZVS converters?

17.7 What is the multiresonant ZCS technique?

17.8 Which parasitic components are included in the topology of ZCS multiresonant converters?

17.11 Problems

17.1 Design a ZVS quasi-resonant converter to meet the following specifications: $V_O = 28\,\text{V}$, $V_I = 42\,\text{V}$, and $I_O = 2\,\text{A}$.

17.2 Design a ZVS quasi-resonant converter to meet the following specifications: $V_O = 42\,\text{V}$, $V_I = 28\,\text{V}$, and $I_O = 5\,\text{A}$.

17.3 Design a ZVS quasi-resonant converter to meet the following specifications: $V_O = 12\,\text{V}$, $V_I = 24\,\text{V}$, and $I_O = 2\,\text{A}$.

17.4 Design a ZCS quasi-resonant converter to meet the following specifications: $V_O = 12\,\text{V}$, $V_I = 24\,\text{V}$, and $I_O = 1\,\text{A}$.

A

Introduction to SPICE

SPICE is an abbreviation for *Simulation Program for Integrated Circuits Emphasis*. PSPICE is the PC version of SPICE. Analog and digital electronic circuit designs are verified widely by both industries and academia using PSPICE. It is used to predict circuit behavior.

Passive Components: Resistors, Capacitors, and Inductors

Rname N + N − Value [IC = TC1]
Lname N + N − Value [IC = Initial Voltage Condition]
Cname N + N − Value [IC = Initial Current Condition]
Examples:
R1 1 2 10 K
L2 2 3 2 M
C3 3 4 100 P

Transformer

Lp Np + Np − Lpvalue
Ls Ns + Ns − Lsvalue
Kname Lp Ls K
Example:
Lp 1 0 1 mH
Ls 2 4 100 µH
Kt Lp Ls 0.999

Temperature

.TEMP list of temperatures

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Example:
.TEMP 27 100 150

Independent DC Sources

Vname N + N − DC Value
Iname N + N − DC Value
Examples:
Vin 1 0 DC 10 V
Is 1 0 DC 2 A

DC Sweep Analysis

.DC Vsource-name Vstart Vstop Vstep
Example:
.DC VD 0 V 0.75 V 1 mV

Independent Pulse Source for Transient Analysis

Vname N + N − PULSE (VL VH td tr tf PW T)
Example:
VGS 1 0 PULSE(0 1E-6 0 1 1 10E-6 100e-6)

Transient Analysis

.TRAN time-step time-stop
Example:
.TRAN 0.1 ms 100 ms 0 ms 0.2 ms

Independent AC Sources for Frequency Response

Vname N + N − AC Vm Phase
Iname N + N − AC Im Phase
Example:
Vs 2 3 AC 2 30
Is 2 3 AC 0.5 30

Independent Sinusoidal AC Sources for Transient Analysis

Vname N + N − SIN (Voffset Vm f T-delay Damping-Factor Phase-delay)
Iname N + N − SIN (Ioffset Im f T-delay Damping-Factor Phase-delay)
Examples:
Vin 1 0 SIN (0 170 V 60 Hz 0 − 120)
Is 1 0 SIN (0 2 A 120 Hz 0 45)

AC Frequency Analysis

.AC DEC points-per-decade fstart fstop
Example:
.AC DEC 100 20 20 kHz

Operating Point

.OP

Getting Started with the SPICE Program

1. Open the PSpice A/D Lite window (**Start > Programs > Orcad9.2 Lite Edition > PSpice AD Lite**).
2. Create a new text file (**File > New > Text File**).
3. Type the example code.
4. Save the file as fn.cir (for example, Lab1.cir), file type: all files, and simulate by pressing the appropriate icon.
5. To include the SPICE code for a commercial device model, visit the website, e.g., http://www.irf.com, http:www.onsemi.com, or http://www.cree.com. For example, for IRF devices, click on (**Design > Support > Models > Spice Library**).

Example Program

```
Diode I-V Characteristics
*Joe Smith
VD 1 0 DC 0.75 V
D1N4001 1 0 Power-Diode
.model Power-Diode D (Is = 195 pA n = 1.5)
.DC VD 0 V 0.75 V 1 mV
.TEMP 27 C 50 C 100 C 150 C
.probe
.end
```

B

Introduction to MATLAB

MATLAB is an abbreviation for MATrix LABoratory. It is a very powerful mathematical tool used to perform numerical computation using matrices and vectors to obtain two- and three-dimensional graphs. MATLAB can also be used to perform complex mathematical analysis.

Getting Started

1. Open MATLAB by clicking **Start > Programs > MATLAB > R2006a > MATLAB R2006a**.
2. Open a new M-file by clicking **File > New > M-File**.
3. Type the code in the M-File.
4. Save the file as fn.m (e.g., Lab1.m).
5. Simulate the code by doing one of the following:
   (a) Click on **Debug > Run**.
   (b) Press F5
   (c) On the tool bar, click the icon **Run**.

Use **HELP** by pressing F1.
Use % at the beginning of a line for comments.

Generating x-axis Data

x = Initial-Value: Increment:Final-Value;
Example:
x = 1:0.001:5;
or

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x = [list of all the values];
Example:
x = [1, 2, 3, 5, 7, 10];
or
x = linspace(start-value, stop-value, number-of-points);
Example:
x = linspace(0, 2*pi, 90);
or x = logspace(start-power, stop-power, number-of-points);
Example:
x = logspace(1, 5, 1000);

Semilogarithmic Scale

semilogx(x-variable, y-variable);
grid on

Log-log Scale

loglog(x, y);
grid on

Generate y-axis Data

y = f(x);
Example:
y = cos(x);
z = sin(x);

Multiplication and Division

A dot should be used in front of the operator for matrix multiplication and division.
c = a.*b;
or
c = a./b;

Symbols and Units

Math symbols should be in italic. Math signs (like ( ), =, and +) and units should not be in italic. Leave one space between a symbol and a unit.

x-axis and y-axis Labels

xlabel('{ \it x} (unit) ')
ylabel('{ \it y} (unit) ')

Example:
xlabel('{\it v_{GS}} (V)')
ylabel('{\it i_{DS} } (A)')
set(gca, 'ylim', [1, 10])
set(gca, 'ytick', [0:2:10])

Greek Symbols

Type: \alpha, \beta, \Omega, \omega, \pi, \phi, \psi, \gamma, \theta, and \circ to obtain: α, β, Ω, ω, π, ϕ, ψ, γ, θ, and $\circ$.

Plot Commands

plot (x, y, '.-', x, z, '- -')
set(gca, 'xlim', [x1, x2]);
set(gca, 'ylim', [y1, y2]);
set(gca, 'xtick', [x1:scale-increment:x2]);
text(x, y, '{\it symbol} = 25 V');
Examples:
set(gca, 'xlim', [4, 10]);
set(gca, 'ylim', [1, 8]);
set(gca, 'xtick', [4:1:10]);
text(x, y, '{\it V} = 25 V');

3D Plot Commands

plot3(x1, y1, z1);
Example:
t = linespace(0, 9*pi);
xlabel('sin(t)')
ylabel('cos(t)')
zlabel('t')
plot(sin(t), cos(t), t)

Bode Plots

f = logspace(start-power, stop-power, number-of-points)
NumF = [a1 a2 a3]; %Define the numerator of polynomial in s-domain.
DumF = [a1 a2 a3]; %Define the denominator of polynomial in s-domain.
[MagF, PhaseF] = bode(NumF, DenF, (2*pi*f));
figure(1)
semilogx(f, 20*log10(MagF))
F = tf(NumF, DenF) %Converts the polynomial into transfer function.
[NumF, DenF] = tfdata(F) %Converter transfer function into polynomial.

Step Response

```
NumFS = D*NumF;
t = [0:0.000001:0.05];
[x, y] = step(NumFS, DenF, t);
figure(2)
plot(t, Initial-Value + y);
```

To Save Figure

Go to File, click Save as, go to EPS file option, type the file name, and click Save.

Example Program

```
clear all
clc
x = linspace(0, 2*pi, 90);
y = sin(x);
z = cos(x);
grid on
xlabel('{\it x}')
ylabel(' {\it y }, {\it z }')
plot(x , y, '-.', x, z, '- -')
```

Polynomial Curve Fitting

```
x = [0 0.5 1.0 1.5 2.0 2.5 3.0];
y = [10 12 16 24 30 37 51];
p = polyfit(x, y, 2)
yc = polyval(p, x);
plot(x, y, 'x', x, yc)
xlabel('x')
ylabel('y'), grid
legend('Actual data', 'Fitted polynomial')
```

Answers to Problems

1.1 $LNR = 10\,\text{mV/V}$, $PLNR = 0.303\,\%$.

1.2 $LOR = 0.2\,\text{mV/mA}$, $PLOR = 0.2\,\%$, $R_o = 0.2\,\Omega$, $LLR = 4$.

1.3 $\eta_{FL(min)} = 22\,\%$, $\eta_{FL(max)} = 55\,\%$.

1.4 $R_{in(DC)} = 36\,\Omega$.

2.2 $L_{min} = 492.2\,\mu\text{H}$.

2.3 $I_{SMmax} = 2.179\,\text{A}$, $V_{SMmax} = 32\,\text{V}$.

2.4 $V_r = 3.214\,\text{mV}$, $V_{Cpp} = 1\,\text{mV}$, $f_0 = 1.592\,\text{kHz}$.

2.5 $V_r = 5.3\,\text{mV}$.

2.6 (a) $D = 0.5$ at $\eta = 100\,\%$. (b) $D = 0.625$ at $\eta = 80\,\%$.

2.7 For $D = 0.1$, $P_{rDS} = 0.25\,\text{W}$. For $D = 0.9$, $P_{rDS} = 2.25\,\text{W}$.

2.8 For $D = 0.1$, $P_D = 4.95\,\text{W}$. For $D = 0.9$, $P_D = 0.55\,\text{W}$.

2.9 $C_{J0} = 585.95\,\text{pF}$, $C_{ds}(V_I) = 25.35\,\text{pF}$, $Q(V_I) = 20.32\,\text{nC}$, $P_{sw} = 8.112\,\text{W}$, $P_{turnoff} = 5.408\,\text{W}$, $P_{sw(FET)} = 2.704\,\text{W}$.

2.10 $L_{max} = 25.6\,\mu\text{H}$.

2.13 $L_{max} = 0.2\,\mu\text{H}$, $C_{min} = 589\,\mu\text{F}$, $r_{Cmax} = 3\,\text{m}\Omega$.

2.14 $L_{max} = 8.2\,\mu\text{H}$, $C_{min} = 228\,\mu\text{F}$, $r_{Cmax} = 37\,\text{m}\Omega$.

3.2 $V_{SMmax} = V_{DMmax} = 380\,\text{V}$, $I_{SMmax} = I_{DMmax} = 0.574\,\text{A}$.

3.3 $L_{min} = 44.44\,\mu\text{H}$.

3.4 $L_{min} = 40.8\,\mu\text{H}$.

3.5 (a) $D = 0.5$ at $\eta = 100\,\%$. (b) $D = 0.6$ at $\eta = 80\,\%$.

Pulse-width Modulated DC–DC Power Converters Marian K. Kazimierczuk
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3.6 $P_{rDS} = 0.247\,\text{W}$, $P_{rDS} = 0.625\,\text{W}$, $P_{rDS} = 1.224\,\text{W}$, $P_{rDS} = 2.222\,\text{W}$, $P_{rDS} = 4\,\text{W}$, $P_{rDS} = 7.5\,\text{W}$, $P_{rDS} = 15.556\,\text{W}$, $P_{rDS} = 40\,\text{W}$, $P_{rDS} = 180\,\text{W}$.

3.7 $P_{RF} = 2.222\,\text{W}$, $P_{RF} = 2.5\,\text{W}$, $P_{RF} = 4\,\text{W}$, $P_{RF} = 10\,\text{W}$, $P_{RF} = 20\,\text{W}$.

3.8 $P_{rL} = 2.469\,\text{W}$, $P_{rL} = 3.125\,\text{W}$, $P_{rL} = 4.082\,\text{W}$, $P_{rL} = 5.556\,\text{W}$, $P_{rL} = 8\,\text{W}$, $P_{rL} = 12.5\,\text{W}$, $P_{rL} = 22.22\,\text{W}$, $P_{rL} = 50\,\text{W}$, $P_{rL} = 200\,\text{W}$.

3.9 $L_{max} = 2.22\,\mu\text{H}$.

4.1 $L_{min} = 304\,\mu\text{H}$.

4.2 $L_{min} = 283.15\,\mu\text{H}$.

4.3 $V_{SMmax} = V_{DMmax} = 235\,\text{V}$, $I_{SMmax} = I_{DMmax} = 3.666\,\text{A}$.

4.4 $C_{min} = 61\,\mu\text{F}$, $r_{Cmax} = 81.85\,\text{m}\Omega$.

4.5 $P_{rC} = 0.111\,\text{W}$, $P_{rC} = 0.25\,\text{W}$, $P_{rC} = 0.429\,\text{W}$, $P_{rC} = 0.667\,\text{W}$, $P_{rC} = 1\,\text{W}$, $P_{rC} = 1.5\,\text{W}$, $P_{rC} = 2.333\,\text{W}$, $P_{rC} = 4\,\text{W}$, $P_{rC} = 9\,\text{W}$.

4.6 $L_{max} = 126.39\,\mu\text{H}$.

4.7 $L_{max} = 115\,\mu\text{H}$.

5.1 $n = 1/3$, $D_{max} = 0.6885$.

5.2 $V_{SMmax} = 454\,\text{V}$, $V_{DMmax} = 1361\,\text{V}$.

5.3 $L_{m(min)} = 711\,\mu\text{H}$.

5.4 $I_{SMmax} = 5.183\,\text{A}$, $I_{DMmax} = 1.728\,\text{A}$.

5.5 $C_{min} = 1.4\,\mu\text{F}$, $r_{Cmax} = 1.736\,\Omega$.

5.7 (a)$L_{m(max)} = 172.5\,\mu\text{H}$. (b)$L_{m(max)} = 57.849\,\mu\text{H}$.

6.1 (a) $D_{MAX} = 0.6667$. (b) $D_{MAX} = 0.3333$. (c) $D_{MAX} = 0.2$.

6.2 (a) $V_{SM} = 3\,V_I$. (b) $V_{SM} = 1.5\,V_I$. (c) $V_{SM} = 1.25\,V_I$.

6.3 (a) $V_{D3M} = 1.5\,V_I$. (b) $V_{D3M} = 3\,V_I$. (c) $V_{D3M} = 5\,V_I$.

6.4 $n_1 = 8$.

6.5 $D_{MAX} = 0.5$.

6.6 $D_{min} = 0.3119$, $D_{nom} = 0.3428$, $D_{max} = 0.381$.

6.7 $V_{SMmax} = 684\,\text{V}$, $V_{D1Mmax} = 42.75\,\text{V}$, $V_{D2Mmax} = 42.75\,\text{V}$, $V_{D3Mmax} = 684\,\text{V}$.

6.8 $L_{min} = 13.762\,\mu\text{H}$.

6.9 $C_{min} = 229\,\mu\text{F}$, $f_o = 2.055\,\text{kHz}$, $r_{Cmax} = 21.8\,\text{m}\Omega$.

6.10 $I_{D1Mmax} = I_{D2Mmax} = 42.75\,\text{A}$.

6.11 $L_{m(min)} = 2.219\,\text{mH}$.

6.12 $I_{SMmax} = 5.985\,\text{A}$.

6.13 $L_{max} = 12.38\,\mu\text{H}$.

7.2 $n = 9$, $D_{min} = 0.3424$, $D_{max} = 0.4193$.

7.3 $V_{SMmax} = 324\,\text{V}$, $V_{DMmax} = 38\,\text{V}$.

7.4 $L_{min} = 18.9\,\mu\text{H}$.

7.5 $C_{min} = 41.93\,\mu\text{F}$, $f_o = 4.5\,\text{kHz}$.

7.6 $L_{m(min)} = 5.08\,\text{mH}$.

7.7 $L_{max} = 0.6858\,\mu\text{H}$.

8.2 $n = 2$, $D_{min} = 0.27021$, $D_{max} = 0.3968$.

8.3 For the transformer center-tapped rectifier, $V_{SMmax} = V_{DMmax} = 187\,\text{V}$. For the transformer bridge rectifier, $V_{SMmax} = V_{DMmax} = 93.5\,\text{V}$.

8.4 $\Delta i_{Lmax} = 31.543\,\text{A}$, $\Delta i_{Lmax}/I_{Omax} = 60.6\,\%$.

8.5 $L_{min} = 60.65\,\mu\text{H}$.

8.6 $C_{min} = 75.58\,\mu\text{F}$, $f_o = 1.9\,\text{kHz}$.

8.7 $L_{m(min)} = 425.788\,\mu\text{H}$.

8.8 $I_{SM} = 35.58\,\text{A}$, $I_{DM} = 67.7714\,\text{A}$.

8.9 $n = 1/10$, $D_{min} = 0.2815$, $D_{max} = 0.4144$.

8.10 $V_{SMnom} = 187\,\text{V}$, $V_{DM} = 1870\,\text{V}$.

8.11 $L_{min} = 21.86\,\text{mH}$.

8.12 $C_{min} = 82.88\,\mu\text{F}$, $r_{Cmax} = 57.18\,\Omega$.

9.1 $n = 1/5$.

9.2 $D_{min} = 0.3509$, $D_{max} = 0.4511$.

9.3 $V_{SMmax} = 108\,\text{V}$, $V_{DMmax} = 270\,\text{V}$.

9.4 $L_{min} = 2\,\text{mH}$.

9.5 $C_{min} = 5.639\,\mu\text{F}$, $f_o = 1.125\,\text{kHz}$, $f_{ripple}/f_o = 71.11$.

9.6 $I_{DM} = 2.168\,\text{A}$, $I_{SM} = 16.26\,\text{A}$.

9.8 $L_{min} = 6.874\,\mu\text{H}$, $C_{min} = 24.8\,\mu\text{F}$, $V_{Imax} = 31.2\,\text{V}$, $I_{SMmax} = 500.52\,\text{A}$, $V_{DMmax} = 124.8\,\text{V}$, $I_{DMmax} = 54.91\,\text{A}$.

9.9 $L = 1.5\,\mu\text{H}$.

10.1 $I_S = 0.4 I_L$, $V_{LD} = 0.4\,V_{SD}$.

10.2 $r_{DSAV(S)} = 2.5\,\Omega$, $R_{FAV(D)} = 40\,\text{m}\Omega$, $V_{FAV(D)} = 0.7\,\text{V}$.

10.3 $r_{DSAV(L)} = 0.4\,\Omega$, $R_{FAV(L)} = 14.4\,\text{m}\Omega$, $V_{FAV(L)} = 0.42\,\text{V}$.

10.4 $r_{DSAV(S)} = 2.5\,\Omega$, $R_{FAV(S)} = 90\,\text{m}\Omega$, $V_{FAV(S)} = 1.05\,\text{V}$.

10.5 $r_{DSAV(D)} = 1.1111\,\Omega$, $R_{FAV(D)} = 40\,\text{m}\Omega$, $V_{FAV(D)} = 0.7\,\text{V}$.

10.6 $r = 0.6144\,\Omega$.

10.7 $r_{L(S)} = 1.25\,\Omega$, $r_{L(D)} = 0.556\,\Omega$.

10.8 $Di_l = 0.4 i_l\,\text{A}$, $I_L d = 1.8d\,\text{A}$, $Dv_{ds} = 0.4\,v_{ds}\,\text{V}$, $V_{DS}\,d = 24d\,\text{V}$, $r = 0.6144\,\Omega$.

11.1 $M_{VDC} = 9.06\,\text{dB}$, $\eta = 98.38\,\%$.

11.2 $z_n = -10^6$ rad/s, $z_p = 7.1683$ krad/s, $f_0 = 323.55$ Hz, $\xi = 0.162$, $Q = 3.086$, p_1, $p_2 = -329.3 \pm j2006.07$ rad/s, $f_d = 319.27$ Hz.

11.3 $T_{po} = 61.05$ dBV, $|T_p(\infty)| = -3.84$ dBV.

11.4 $M_{vo} = 9$ dB.

11.5 $Z_i(0) = 220.384\,\Omega$.

11.6 $Z_o(0) = 22.216\,\Omega$, $Z_o(\infty) = 1\,\Omega$.

11.7 $Z_o(0) = 3.4\,\Omega$, $Z_o(0) = 10.96\,\Omega$, $Z_o(0) = 66.329\,\Omega$, $Z_o(0) = 238.61\,\Omega$.

11.8 $\xi_{lossy}/\xi_{lossless} = 1.165$, $Q = 3.597$, $\xi = 0.139$.

12.1 $T_m = 0.2\,\text{V}^{-1}$.

12.2 $V_R = 3.25$ V.

12.3 $\beta = 1/123 = -41.8$ dB. $R_B = 1\,\text{k}\Omega$, $R_A = 120\,\text{k}\Omega$, $h_{11} = 992\,\Omega$.

12.4 $T_k = 5.162$ dB.

12.6 $T_{clo} = 41.8$ dB.

12.7 $R_{icl}(0) = -215\,\Omega$ at R_{Lmin}, $R_{icl}(0) = -2175\,\Omega$ at R_{Lmax}.

13.1 $V_I > 2\,V_O = 10$ V.

13.2 $V_I > 11.11$ V.

13.3 Stable. $M_1 = 76.41 \times 10^3$ A/s.

13.4 Unstable. The converter requires slope compensation.

13.5 $V_{Tm} = 0.664$ V, $M_{3opt} = 66.45 \times 10^3$ A/s.

13.6 $M_{3nom} = 46.847 \times 10^3$ A/s, $I_{pk} = 0.468$ A.

13.7 $H_{icl}(z) = 13z/(z + 0.3)$, $H_{icl}(s) = 120 \times 10^{10}/(s^2 + 323,076.9s + 12 \times 10^{10})$, $T_{i(s)} = 12 \times 10^{10}/[s(s + 323076.9)]$.

13.8 $V_O = -31.154$ V.

14.1 $z_{i1} = -1124$ rad/s, $f_{zi1} = 178.8$ Hz.

14.2 $T_{pio} = 11.19$ dBA, $T_{pix} = 142.5$ dBA.

14.3 $M_{vio} = -46.78$ dBA/V, $f_{zi2} = 89.46$ Hz.

14.4 $A_{io} = 9$ dB, $f_{zn} = 159$ kHz.

15.1 $p = 1.5 \times 10^{16}$ holes/cm^3, $\rho_p = 0.868\,\Omega$cm, $\sigma_p = 1.152\,(\Omega\text{cm})^{-1}$, silicon-to-boron atoms $= 3.333 \times 10^6$, $p/n = 10^{12}$, $\rho_{Si}/\rho_p = 2.058 \times 10^5$.

15.2 $x_p = 0.32\,\mu$m, $x_p = 32\,\mu$m, $W = 32.32\,\mu$m, $x_n/x_p = 100$.

15.3 $x_p = 0.272\,\mu$m, $x_n = 0.00272\,\mu$m, $W = 0.2747\,\mu$m, $x_n/x_p = 100$.

15.4 $x_n = 88\,\mu$m, $x_p = 0.88\,\mu$m, $W = 88.88\,\mu$m, $x_n/x_p = 100$, $E_m = 135.53$ kV/cm.

15.7 $t_{10\,\%} = 2.3\tau_p$.

15.8 $P_{RR} = 5$ W.

15.9 $A_J = 0.05\,\text{cm}^2$, $N_{Dmin} = 2.1623 \times 10^{16}\text{cm}^{-3}$, $l_n = 5.45\,\mu\text{m}$, $C_{J0} = 864.2\,\text{pF}$, $R_{DR} = 0.3849\,\mu\Omega$.

16.1 $\mu_n = 100\,\text{cm}^2/\text{Vs}$.

16.2 $W_D = 5\,\mu\text{m}$, $W_D = 10\,\mu\text{m}$, $W_D = 20\,\mu\text{m}$, $W_D = 40\,\mu\text{m}$.

16.3 $N_D = 2.586 \times 10^{15}\,\text{cm}^{-3}$, $N_D = 1.293 \times 10^{15}\text{cm}^{-3}$, $N_D = 6.465 \times 10^{14}\text{cm}^{-3}$, $N_D = 3.232 \times 10^{14}\text{cm}^{-3}$.

16.4 $V_{BD} = 1295\,\text{V}$, $V_{BD} = 129.5\,\text{V}$, $V_{BD} = 12.95\,\text{V}$.

16.5 $V_{BD} = 129.9\,\text{kV}$, $V_{BD} = 12.99\,\text{kV}$, $V_{BD} = 1.299\,\text{kV}$.

16.6 (a) $C_{ox} = 34.53\,\mu\text{F/m}^2$, $k_p = 2.07\,\mu\text{A/V}^2$. (b) $C_{ox} = 345.3\,\mu\text{F/m}^2$, $k_p = 20.7\,\mu\text{A/V}^2$. (b) $C_{ox} = 3453\,\mu\text{F/m}^2$, $k_p = 207\,\mu\text{A/V}^2$.

16.7 $I_{Dsat} = 4.9\,\text{A}$, $R_c = 0.714\,\Omega$, $R_{c(sc)} = 1.214\,\Omega$.

16.8 $W = 1.6 \times 10^6\,\mu\text{m}$, $n = 10^5$, $A_c = 3.6\,\text{mm}$, $CD = 27,778\,\text{cells/mm}^2$, $SD = 0.444\,\text{m/mm}^2$, $U = 0.3556\,\text{m/mm}^2$.

16.10 $C_{ox} = 34.53\,\text{nF/cm}^2$, $k_p = 13.812\,\text{nF/cm}^2$, $(W/L)_{min} = 4.525 \times 10^5$, $L = 1\,\mu\text{m}$, $W = 0.4525\,\text{m}$, $n = 5.656 \times 10^3$.

17.1 $f_0 = 3\,\text{MHz}$, $D = 0.667$, $L_r = 1.2\,\mu\text{H}$, $C_r = 2.7\,\text{nF}$, $I_{SM} = 2\,\text{A}$, $V_{SM} = 84\,\text{V}$, $I_{DM} = 4\,\text{A}$, $V_{DM} = 42\,\text{V}$.

17.4 $f_0 = 2\,\text{MHz}$, $D = 0.5$, $L_r = 0.21\,\mu\text{H}$, $C_r = 33\,\text{nF}$, $I_{SM} = 20\,\text{A}$, $V_{SM} = 24\,\text{A}$, $I_{DM} = 10\,\text{A}$, $V_{DM} = 48\,\text{V}$.

INDEX

Acceptor, 630, 633, 638
Active clamping, 232, 281, 282, 283
Ambient temperature, 729
Amorphous material, 628
Antiparallel diode, 123, 679
Apparent power, 129
Aspect ratio, 684, 699
Asymmetrical junction, 633
Audio susceptibility, 450, 495, 552, 616
Avalanche breakdown, 637, 642, 668, 699, 701
Average power, 18, 129
Averaged circuit model, 397, 407, 414, 415, 416, 417, 418, 419, 428

Baliga, 704
Band gap energy, 629, 631, 632, 668
Bandwidth, 448, 453
Battery charger, 1
Beveled edge, 645
Bidirectional converter, 123, 174, 229
Bode plots, 448, 449, 451, 452, 474, 475, 477, 482, 492, 533, 538, 570
Body diode, 677, 679, 685, 699, 700, 710, 711, 712, 713, 715
Boost converter, 16, 17, 85, 642, 552, 616
Boost-buck converter, 16, 17, 177, 643
Breakdown voltage, 627, 632, 637, 645, 699, 701, 704, 727
Bridge converter, 17, 289, 325
Bridge rectifier, 132, 290, 326
Buck converter, 16, 23
Buck-boost converter, 16, 17, 129
Built-in potential barrier, 39, 641, 646, 647

Cascade, 73, 178
CCM, 23, 30, 85, 139, 191, 239, 398
Channel-length modulation, 683
Characteristic impedance, 230, 737
Charge carrier, 629, 648, 659, 660, 665, 686
Charge neutrality, 630
Chopper, 24
Circuit averaging, 397
Clamp diode, 233
Class E amplifier, 736
Closed loop, 493, 495, 496, 500, 506, 518, 526, 528, 530, 531, 543, 552, 592, 553, 559
CMOS, 70, 179
Complex power, 129
Comparator, 512
Compensator, 512
Conducted interference, 19
Conduction loss, 43, 49
Conductivity modulation, 636, 680, 727
Constant-frequency control, 512, 561
Continuous conduction mode, 23
Continuous-time model, 399
Control, 257, 469, 512,
Controller, 480
Control voltage, 566, 567, 568
Conversion ratio, 5
Converter, 23, 85, 139
Crossover frequency, 484
Current-mode control, 511, 551, 554, 557
Current probe, 512
Current programming, 511
Current ripple, 33, 294

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Current source, 25
Current transformer, 512
Ćuk converter, 16, 17, 177

DCM, 23, 30, 103, 159, 201, 261, 421
Deadbeat control, 526
Delay time, 448, 576
Depletion region, 633, 638, 683
Diode, 23, 627, 629
Discontinuous conduction mode, 23, 51
Discrete-time model, 530
Displacement factor, 130
Dissipation, 43
Distortion factor, 130
Disturbance, 464, 546
Donor, 630, 633
Drain, 41, 674
Drift current, 629, 660
Drift region, 674, 679, 701, 702, 708, 710, 726
Dual converter, 17, 127
Duality, 127
Duty cycle, 24
Duty ratio, 24,

Efficiency, 5, 9, 42, 61, 95, 112, 140, 166, 201, 219, 250, 270, 301, 336, 374
Electromagnetic interference, 19
EMI, 19, 232, 735, 669
Energy, 18, 28, 41, 189, 192, 240, 403, 434, 647
Equivalent series resistance, 33
Error amplifier, 478, 548
Error voltage, 534, 478
ESR, 33, 37, 80, 146
Extrinsic semiconductor, 630, 633, 661
Excess charge, 648, 650, 654

Feedback network, 488, 609
Filter, 24, 69, 192, 530
Flip-flop, 512
Flyback converter, 16, 17, 189
Forced response, 528
Forward converter, 16, 17, 239
Fourier series, 32, 567
Freewheeling diode, 23

Gain margin, 480, 484, 538
Gate, 43, 47, 674
Gate drive, 43, 47
Gate oxide, 674, 701, 784
Gate threshold voltage, 701, 784
Grading coefficient, 647

Half-bridge converter, 17, 289
Harmonics, 32, 411
Heatsink, 728
Heat transfer, 728
  conduction, 728
  convection, 728
  radiation, 728
Hole, 630, 631, 656, 674, 686

Ideal transformer, 190, 193, 242
IGBT, 726
Impact ionization, 637
Incremental capacitance, 646, 649
Inductance, 32, 59, 93, 146, 166, 199, 248, 270, 299, 320, 335, 355, 372, 292
Inductor, 23, 25, 74, 76, 124, 126, 181
Instability, 518, 521
Insulated gate bipolar transistor, 726
Integral control, 480, 485, 488, 611
Integral-lead controller, 480, 485, 488, 611
Intrinsic semiconductor, 628, 667
Inverse converter, 17, 126
Isolated converter, 17, 192, 229

Junction, 632, 637, 645, 647
  capacitance, 646, 662
  breakdown, 642, 633, 662
  temperature, 627, 631, 628, 687, 729

Laplace, 503, 568, 569, 588, 749, 747
Latch, 512, 514
Leakage inductance, 191, 229, 230, 231, 241
Line regulation, 6, 8
Linear model, 411, 415, 417
Linear region, 678, 686
Linearization, 399, 413
Linearized averaged circuit, 397, 415, 417
Load regulation, 7, 8
Loop, 518, 524, 526, 530, 531, 537, 543, 546, 552
Loop gain, 492, 537, 611, 548
Loss, 5, 37, 61, 95, 201, 250, 270, 301, 336, 374, 628
Low-pass filter, 25, 280, 530

Majority carrier device, 656
Metal-oxide-semiconductor field effect transistor, 673
Minority carrier devices, 659
Minority carrier lifetime, 648, 656, 662
Magnetic core, 82, 134, 241
Magnetizing inductance, 191, 198,199, 218, 242, 243, 245, 265, 290, 294, 296, 315, 328, 331, 386
Metal-semiconductor junction, 659

Mobility, 674, 680, 686, 687, 692, 696, 699, 710
Mobility degradation coefficient, 696
Model, 6, 397, 405, 408, 414, 415, 416, 417, 418
Modulated signal, 567
Modulating signal, 567
MOSFET, 18, 23, 289, 325, 363, 673, 684, 686, 701, 708, 710
Multiphase converter, 77
Multiple outputs, 228, 280
Multi-resonant converter, 759

n-type, 630, 633, 638, 640, 648, 659, 661
Natural frequency, 442
Natural response, 526
Noise, 15, 19
Nonlinear capacitance, 39
Nonlinear circuit, 397, 400, 413, 415, 418
Nonlinearity, 39
Nyquist frequency, 413, 433, 531

Off-state, 627
Ohmic region, 678, 679
On-resistance, 42, 403, 627, 705, 708, 727
On-state, 627
On-voltage, 627
Output voltage, 6, 7, 8, 24
Op-amp, 512
Open loop, 437, 440, 450, 453, 455, 458, 571, 576, 581, 585, 588, 590
Overshoot, 459, 462i, 464, 586, 589, 591

p-type, 631, 633, 640, 648, 660, 674
Parasitic capacitances, 710
Perturbation, 413, 518, 519, 520, 521, 525, 526, 527
PFC, 129, 132
Phase, 191, 326, 442, 455, 458, 540, 549
Phase control, 357
Phase margin, 480, 484, 538, 541, 550
Phase shift, 191
Pinch-off region, 678
Pole, 442, 531, 544, 574, 575
Polyphase converter, 77
Polysilicon, 674, 714, 715
Power factor, 129
Power factor correction, 129, 132
Power quality, 131
Primary winding, 190, 229, 230, 290, 330, 363
Punch-through breakdown, 642, 643
Push-pull converter, 17, 263
Pulse-width modulation, 1, 65, 289, 471
PWM, 1, 65, 289, 325, 471, 551

Quality factor, 442, 446, 574, 575, 743
Quasi-resonant converter, 736, 745, 753

Rational function, 532
Real power, 129
Reference voltage source, 13
Regulation, 6, 7, 8
Reverse recovery, 650, 651, 662, 669
Richardson constant, 661
RHP, 442, 444, 530, 546
Right-hand plane zero, 442, 464
Ripple, 32, 93, 146, 218, 248, 299, 335, 372

SH, 526
Sampling-and-hold, 511, 526, 536, 544, 548, 566
Saturation, 635, 678, 685, 678, 692, 695, 696, 698, 710
Saturation region, 678, 686, 715
Sawtooth voltage, 473
Schottky diode, 18, 632, 635, 649, 659, 670
Secondary winding, 190, 296, 329, 363
Second-order filter, 24, 69, 530
Semiconductor, 628, 630
Semiconductor device, 627, 673
SEPIC, 16, 17, 666, 724, 726, 765
Shoot-through, 70
Short-channel effect, 697
Silicon, 627, 628, 631, 673
Silicon carbide, 627, 628, 631, 662, 668, 673,
Single-ended converter, 16, 17, 339, 440, 436
Single phase, 17
Slope compensation, 521, 523, 525, 526, 544, 554, 557, 560
Soft switching, 735
Stability, 480, 519, 523, 524, 534
State-space averaging, 397
Stored charge, 650, 679
Stored energy, 28, 220, 240
Switch, 23, 627, 737
Switching frequency, 24
Switching loss, 38, 39, 43, 654, 735
Synchronous rectifier, 69, 124, 178, 179, 180, 281

THD, 130
Thermal management, 632, 728
Thermal model, 728
Thermal resistance, 728
Thermal resistivity, 728
Threshold voltage, 12, 635, 677, 685, 686
Topology, 17, 727, 736
Total harmonic distortion, 130
Transfer function, 441, 448, 450, 472, 552, 559

Transform, 503, 567, 568, 569, 588, 747, 749
Transformer, 17, 189, 190, 192, 193, 239, 289, 290, 326, 363
Triode region, 678
Transient response, 458, 502, 620
Transition, 37, 39, 40, 651, 657, 665, 710
Turns ratio, 190, 241, 306, 341, 378

Unity power factor, 129, 130, 132, 133
Unstable, 519, 521, 524, 532, 534, 546
Utility, 1, 129, 132

Variable, 531
Voltage clamp, 231
Voltage-mode control, 469
Voltage regulation, 1, 13, 14
Volt-second balance, 29

z-domain, 530
z-transform, 530, 530

ZCS, 736, 751, 760, 763
Zero-current switching, 736, 751, 753
Zero, 442, 444, 574, 579, 583
ZOH, 526, 531
Zero-order hold, 526, 531, 569
ZVS, 736, 745, 760, 763
Zero-voltage switching, 736, 745, 763